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PATENT SPECIFICATION

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DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Field-Effect Transistors.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to field-effect transistors, which are also referred to as unipolar transistors.

The field-effect transistors of the invention are especially useful for operation at high frequencies.

A field-effect transistor as used herein includes a charge carrier path or channel of low resistivity semiconductor material and two spaced electrical contacts to the channel. The contacts are referred to as the source and the drain. Such a field-effect transistor includes also a gate electrode adjacent to and electrically separated from the path or channel. When a voltage is applied between the source and the drain, majority charge carriers flow through the path or channel from the source to the drain. The magnitude of the carrier current may be modulated, by modulating the drain-to-source voltage and/or applying a modulating voltage to the gate electrode.

An object of this invention is to provide an improved field-effect transistor having a minimum charge carrier path or channel length as determined by the manufacturing technology and an improved high frequency response.

Accordingly, the present invention provides a field-effect transistor comprising a body of semiconductor material a source adjacent to a surface of said body; a drain adjacent to said surface and spaced from

said source; said source and said drain defining the ends of a charge carrier path extending entirely adjacent to said surface; and a single continuous gate electrode structure adjacent to said surface and extending opposite to at least a portion of said source and a continuous portion of said path, one end of said gate electrode structure being closer physically to said source than the other end of said gate electrode structure is to said drain.

By offsetting the gate electrode structure in this manner, without changing the path (channel) length or the gate length, the capacitance between the drain and the gate electrode is reduced, thereby reducing the coupling between the input and the output of the device. The reduced input-to-output circuit coupling improves the stability characteristic of analogue circuits in which the device is used. In switching circuits, this reduced coupling improves the speed of response. This is achieved at the expense of a higher capacitance between the source and the gate electrode. This has a relatively minor effect on the operating characteristics of the device and may be tuned out by a proper selection of the associated circuit components.

During the operation of a field-effect transistor, one portion of the path or channel effectively appears as a resistance between the source and that region of the path or channel which is gated when a gate voltage is applied. Another portion of the path or channel effectively appears as a resistance between the drain and that region of the path or channel which is gated when a gate voltage is applied. By offsetting the gate electrode toward the source according to this invention, the resistance between the source and the gated region of the path or channel is reduced, while the resistance be-

tween the drain and the gated region of the path or channel is increased.

The reduction of resistance between the source and gated region increases the transconductance of the device, since this resistance is common to the input and output circuits and is degenerative. In addition, the reduced resistance between the source and gated region reduces the input circuit time constant and hence extends the upper frequency limit at which the device is operable. It should be noted that the increase in source-to-gate capacitance can be compensated by external circuit means.

More than one gate electrode may be used. In this application all of the gate electrodes are considered together and are referred to as the gate electrode structure. Unlike previous unipolar transistors where more than one gate electrode is used, the gate electrode structure is continuous with respect to a portion of the path or channel length, so that the resistance in the path or channel between the source and the gate electrode structure is minimized at the expense of the resistance between the drain and the gate electrode structure.

Referring to the accompanying drawings:

FIGURE 1 is a side view partially in section of a first embodiment of a field-effect transistor according to the present invention and having a junction type gate electrode internal to a semiconductor body and shown diagrammatically with a biasing circuit;

FIGURE 2 is an equivalent circuit of the field-effect transistor of FIGURE 1;

FIGURE 3 is a sectional view of a second embodiment of a field-effect transistor according to the invention and having a single insulated gate electrode external to the semiconductor substrate and shown diagrammatically with a biasing circuit; and

FIGURE 4 is a sectional view of a third embodiment of a field-effect transistor according to the invention and having two insulated gate electrodes external to the semiconducting substrate.

Similar reference numerals are used for similar elements in the several FIGURES of the drawings.

Referring particularly to FIGURE 1, a transistor 11 is illustrated having a relatively low resistivity base 13 of N-type semiconductor material. The base 13 is a single crystal wafer having two opposed surfaces 14 and 16. The base 13 may be made from any of the semiconductor materials used to prepare transistors in the semiconductor art. For purpose of illustration, the base 13 is a single crystal body of N-type germanium having a resistivity of approximately 1 ohm-cm. On the surface 14 of the base 13 are located two spaced metal contacts 15 and 17, which function as the source and the drain respectively.

A P-type region 19 which constitutes the gate electrode of the device extends from the opposite surface 16 of the base 13 inwardly toward the surface 14. The interface between the P-type region and the N-type portion 13 is a P-N junction 21, which is spaced a short distance from the surface 14 and is substantially parallel to the surface 14 over a substantial area. The space between the P-N junction 21 and the surface 14 in the region between the source 15 and the drain 17 defines the channel of the device. A gate connection 23 of metal connects to the P-type region 19.

FIGURE 1 also includes a circuit for using the device of FIGURE 1 as an amplifier. The circuit shown is typical of a common-source connection amplifier. The circuit includes a pair of input terminals 29 for applying an input signal to the gate connection 23. One input terminal is grounded. The other input terminal is connected in series to the gate connection 23 together with means for biasing the gate electrode 19 in the reverse direction with respect to the source and drain. As shown, the gate biasing means comprises a variable gate bias resistor 30 and a battery 31 connected at one end to the gate connection 23 and grounded at the other end. A negative bias is applied to the gate electrode 19 through the gate connection 23.

The circuit includes also a pair of output terminals 33 for deriving an output signal from the device 11. One output terminal 33 is connected to the drain 17 and to means for biasing the drain electrode 17 with respect to ground. The drain biasing means comprises a battery 35 connected at one end to ground and at the other end serially with a variable load resistor 37 to the drain electrode 17 and output terminal 33. The source 15 is grounded and the drain 17 is biased positively with respect to the source electrode 15.

It can be seen that the gate electrode, which is defined by the P-N junction 21, is offset toward the source 15 so that it overlaps a substantial portion of the source 15, while there is effectively no overlap of the drain 17. This offset structure is to be compared with a conventional gate structure, which is shown by the dotted lines in FIGURE 1 to indicate the usual position of the P-type gate electrode 19a, the P-N junction 21a, and the gate connection 23a. By offsetting the gate from the position shown by the dotted lines to the position shown by the solid lines, the device may be operated at significantly higher frequencies and exhibits better operating stability than the conventional device.

One explanation for the improvement achieved by off-setting the gate 21 may be made in connection with the equivalent cir-



cuit shown in Figure 2. The equivalent circuit for the unipolar transistor of Figure 1 includes a source capacitance C_{sg} and a source resistance R_{sg} in series between the gate 19 and the source 15, and a drain capacitance C_{dg} and a drain resistance R_{dg} in series between the gate 19 and the drain 17. The equivalent circuit also includes a distributed capacitance C_{cg} between the gate 19 and the gated portion of the channel of the device. The equivalent circuit considers that there are three resistances in series between the source 15 and the drain 17. There is a first resistance R_{so} between the source and the gated portion of the channel; a second resistance R_c of the gated portion of the channel; and a third resistance R_{do} between the drain 17 and the gated portion of the channel.

The equivalent circuit also considers that there are three capacitances associated with the gate of the device. There is a first capacitance C_{sg} between the source and the gate, a second capacitance C_{dg} between the drain and the gate, and a third distributed capacitance C_{cg} between the gate and the channel. Because the second capacitance C_{dg} is an important part of the input capacitance of the device, it is desirable that it be as low as possible; although the other capacitances should also be low. By offsetting the gate 19 as shown in Figure 1, C_{dg} is reduced and therefore the effective input capacitance is reduced by an amount which is a function of the amount of offset. The overall transconductance of the device is improved because the resistance R_{so} is an unbypassed degenerative resistance common to the input and output circuits.

Increases in R_{do} have little effect on the usual operation of the device, since R_{do} is usually small compared with the load resistor, such as the resistor 37 in Figure 1, normally in the circuit. Increases in C_{sg} have little effect on the usual operation of the device, especially because this capacitance can be compensated for by a suitable inductance in the operating circuit.

Offsetting the gate toward the source according to the invention may be used for one or more of the following purposes: (1) to reduce the coupling between the input and output of the device, (2) to increase the operating frequency of the device and its associated circuit, and (3) to improve the transconductance of the device.

Figure 3 illustrates a second embodiment of a field-effect transistor which has an insulated gate external to the base or substrate of the device. The device 41 comprises a high resistivity base 43 of semiconductor material. The base 43 may be either single crystal or may be polycrystalline; and may be any one of the semiconductor materials

used to prepare transistors in the semiconductor art.

The base 43 includes a reacted region comprising a high resistivity layer 45 of converted body material and a low resistivity channel 47 between the bulk of the base 43 and the high resistivity layer 45 of converted body material. For purposes of illustration, the base 43 in Figure 3 is a single crystal body of P-type silicon having a resistivity of approximately 100 ohm-cm and is approximately 10 mils thick. The high resistivity layer 45 is produced by oxidizing a portion of the surface of the base 43. The high resistivity layer 45 is approximately 2,000 Å thick and consists essentially of pure silicon oxide produced by completely oxidizing the silicon of the base 43. The low resistivity channel 47 is produced at the same time as the high resistivity layer 45 and is sometimes referred to as an inversion layer. The channel 47 extends under the entire high resistivity layer 45 and may be described as partially oxidized silicon, which is transitional between the pure silicon of the base 43 and the silicon oxide of the high resistivity layer 45. The channel 47 is believed to have a low resistivity by virtue of attracting free charge carriers thereto which compensate for unbalanced electronic charges in the partially converted semiconductor material of the channel 47.

A gate electrode 49, preferably of a metal such as aluminium is disposed on the high resistivity layer 45 opposite to and spaced from the channel 47. The gate electrode 49 is offset toward a source 51 and away from a drain 53. As illustrated in Figure 1, the gate electrode 49 extends opposite to the channel 47 and then over the source 51.

The source 51 is in the base 43 and connects to one end of the channel 47. Similarly the drain 53 is in the base 43 and connects to the other end of the channel 47. The length of the channel 47, which is the distance between the source 51 and the drain 53, is approximately 0.5 mil. As illustrated, the source 51 and the drain 53 are regions of the base 43 into which N-type impurities have been diffused to render them conducting. Any of the structures which make a suitable connection to the channel 47 may be used as the source 51 and the drain 53.

A source electrode 55 contacts a part of the source 51. A drain electrode 57 contacts a part of the drain 53. The source and drain electrodes 55 and 57 are preferably of a metal, such as aluminium, and may be produced in the same step and of the same material as the gate electrode 49.

Figure 3 also includes a circuit for operating the transistor 41 as an amplifier. The circuit, which is of the common source type, is similar to that illustrated in Figure 1. In one mode of operation, the drain voltage



V_d and drain current I_d are adjusted to the desired values as by adjusting the variable load resistor 37 and the variable gate bias resistor 30. A signal voltage V_g is applied to the input terminals 29. For a device having a channel length of approximately 0.5 mil, the frequency response can extend into the kilomegacycle range. Drain (conventional) current I_d flows from ground through the voltage source 35, through the load resistor 37, the drain electrode 57, through the drain 53, the channel 47, the sources 51, the source electrode 55 to ground. Majority charge carriers flow in the opposite direction in this embodiment. The transistor may be used to translate from a high impedance input to a low impedance output, to amplify the input signal, or both to translate and to amplify.

The transistor illustrated in Figure 3 may be prepared by the following process. A 100 ohm-cm P-type silicon wafer approximately 18 mils thick is chemically polished to a thickness of 10 mils. A uniform layer of phosphorus doped silicon oxide is thermally deposited upon one surface of the wafer by heating for approximately 10 minutes at 75° C. in an atmosphere of argon which has been bubbled through trimethyl-phosphate and tetraethyl-orthosilicate. The deposited oxide is consolidated by heating for approximately 5 minutes at 75° C. in an atmosphere of argon which has bubbled through silane. A photoresist pattern is now deposited upon the consolidated oxide and the oxide etched away leaving the doped consolidated oxide over those areas which are to be the source and drain and removing the doped oxide from the region between source and drain.

The wafer is now heated at approximately 900°C. in oxygen to grow a new silicon oxide layer in the region between source and drain and produce an inversion layer under this layer. Also it simultaneously produces a diffusion of impurities from the doped consolidated oxide into the wafer. This diffusion forms the highly doped source-drain contacts. Then, the wafer is coated with a photoresist and etched to provide access through the oxide layer into the source and drain. Then aluminium metal is evaporated over the entire surface of the wafer. A photoresist is now applied and the aluminium metal is etched away from the surface of the wafer except where the source electrode, the drain electrode and the gate electrode are to be located. It is at this step that the shape of the gate electrode is defined. The mask is offset to define the gate electrode. Finally, the wafer is diced and suitable leads connected to the source, drain and gate electrodes.

Figure 4 illustrates a third embodiment of a planar transistor 41a which is the same as

the transistor illustrated in Figure 3 except that an additional second gate electrode 59 is provided. A unipolar transistor having two (or more) gate electrodes physically spaced along the length of the channel produces, not only the resistances R_{cs}, R_{co} and R_{cd} mentioned above, but also produces additional resistances along the channel opposite to the space between adjacent gate electrodes.

It has been found on analysis that all of the gate electrodes should be considered as a single gate electrode structure. In order to achieve improved operating characteristics in a planar field effect transistor, it is desirable in the practice of this invention to provide a continuous gate electrode structure. By this is meant that the one or more gate electrodes present to the channel a continuous face with no spaces therebetween. To this end, the embodiment of Figure 4 provides a second gate electrode 59 which is insulated from the first gate electrode 49a. Also, the continuous gate electrode structure (comprising the two gate electrodes 49a and 59) is offset toward the source 51a and away from the drain 53a in the manner described with respect to the device of Figure 3.

The circuit included in Figure 4 is similar to the circuit described in Figure 3 except that a second pair of input terminals 63 are provided, together with suitable means 65 for biasing the gate electrode 59.

WHAT WE CLAIM IS:—

1. A field-effect transistor comprising a body of semiconductor material, a source adjacent to a surface of said body; a drain adjacent to said surface and spaced from said source, said source and said drain defining the ends of a charge carrier path extending entirely adjacent to said surface; and a single continuous gate electrode structure adjacent to said surface and extending opposite to at least a portion of said source and a continuous portion of said path, one end of said gate electrode structure being closer physically to said source than the other end of said gate electrode structure is to said drain.

2. A field-effect transistor as claimed in Claim 1, wherein said gate electrode structure comprises a single P-N junction in said body.

3. A field-effect transistor as claimed in Claim 1, wherein said gate electrode structure comprises at least one gate electrode spaced from said path by a thin insulating layer.

4. A field-effect transistor as claimed in Claim 1 or Claim 3, wherein said gate electrode structure comprises a single gate electrode spaced from said path by an insulating layer genetically derived from said body.

5. A field-effect transistor as claimed in Claim 1 or Claim 3 wherein said gate elec-

source

V_d and drain current I_d are adjusted to the desired values as by adjusting the variable load resistor 37 and the variable gate bias resistor 30. A signal voltage V_s is applied to the input terminals 29. For a device having a channel length of approximately 0.5 mil, the frequency response can extend into the kilomegacycle range. Drain (conventional) current I_d flows from ground through the voltage source 35, through the load resistor 37, the drain electrode 57, through the drain 53, the channel 47, the sources 51, the source electrode 55 to ground. Majority charge carriers flow in the opposite direction in this embodiment. The transistor may be used to translate from a high impedance input to a low impedance output, to amplify the input signal, or both to translate and to amplify.

The transistor illustrated in Figure 3 may be prepared by the following process. A 100 ohm-cm P-type silicon wafer approximately 18 mils thick is chemically polished to a thickness of 10 mils. A uniform layer of phosphorus doped silicon oxide is thermally deposited upon one surface of the wafer by heating for approximately 10 minutes at 75° C. in an atmosphere of argon which has been bubbled through trimethyl-phosphate and tetraethyl-orthosilicate. The deposited oxide is consolidated by heating for approximately 5 minutes at 75° C. in an atmosphere of argon which has bubbled through silane. A photoresist pattern is now deposited upon the consolidated oxide and the oxide etched away leaving the doped consolidated oxide over those areas which are to be the source and drain and removing the doped oxide from the region between source and drain.

The wafer is now heated at approximately 900°C. in oxygen to grow a new silicon oxide layer in the region between source and drain and produce an inversion layer under this layer. Also it simultaneously produces a diffusion of impurities from the doped consolidated oxide into the wafer. This diffusion forms the highly doped source-drain contacts. Then, the wafer is coated with a photoresist and etched to provide access through the oxide layer into the source and drain. Then aluminium metal is evaporated over the entire surface of the wafer. A photoresist is now applied and the aluminium metal is etched away from the surface of the wafer except where the source electrode, the drain electrode and the gate electrode are to be located. It is at this step that the shape of the gate electrode is defined. The mask is offset to define the gate electrode. Finally, the wafer is diced and suitable leads connected to the source, drain and gate electrodes.

Figure 4 illustrates a third embodiment of a planar transistor 41a which is the same as

the transistor illustrated in Figure 3 except that an additional second gate electrode 59 is provided. A unipolar transistor having two (or more) gate electrodes physically spaced along the length of the channel produces, not only the resistances R_{cs}, R_{cd} and R_{ds} mentioned above, but also produces additional resistances along the channel opposite to the space between adjacent gate electrodes.

It has been found on analysis that all of the gate electrodes should be considered as a single gate electrode structure. In order to achieve improved operating characteristics in a planar field effect transistor, it is desirable in the practice of this invention to provide a continuous gate electrode structure. By this is meant that the one or more gate electrodes present to the channel a continuous face with no spaces therebetween. To this end, the embodiment of Figure 4 provides a second gate electrode 59 which is insulated from the first gate electrode 49a. Also, the continuous gate electrode structure (comprising the two gate electrodes 49a and 59) is offset toward the source 51a and away from the drain 53a in the manner described with respect to the device of Figure 3.

The circuit included in Figure 4 is similar to the circuit described in Figure 3 except that a second pair of input terminals 63 are provided, together with suitable means 65 for biasing the gate electrode 59.

WHAT WE CLAIM IS:—

1. A field-effect transistor comprising a body of semiconductor material, a source adjacent to a surface of said body; a drain adjacent to said surface and spaced from said source, said source and said drain defining the ends of a charge carrier path extending entirely adjacent to said surface; and a single continuous gate electrode structure adjacent to said surface and extending opposite to at least a portion of said source and a continuous portion of said path, one end of said gate electrode structure being closer physically to said source than the other end of said gate electrode structure is to said drain.

2. A field-effect transistor as claimed in Claim 1, wherein said gate electrode structure comprises a single P-N junction in said body.

3. A field-effect transistor as claimed in Claim 1, wherein said gate electrode structure comprises at least one gate electrode spaced from said path by a thin insulating layer.

4. A field-effect transistor as claimed in Claim 1 or Claim 3, wherein said gate electrode structure comprises a single gate electrode spaced from said path by an insulating layer genetically derived from said body.

5. A field-effect transistor as claimed in Claim 1 or Claim 3 wherein said gate elec-



trode structure comprises two overlapping gate electrodes spaced from said path by a first thin insulating layer genetically derived from said body, and spaced from each other by a second thin insulating body.

6. A field-effect transistor substantially as herein described with reference to and as illustrated in Figure 1 of the accompanying drawings.

7. A field-effect transistor substantially as herein described with reference to and as

illustrated in Figure 3 of the accompanying drawings.

8. A field-effect transistor substantially as herein described with reference to and as illustrated in Figure 4 of the accompanying drawings.

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