

DRAWINGS

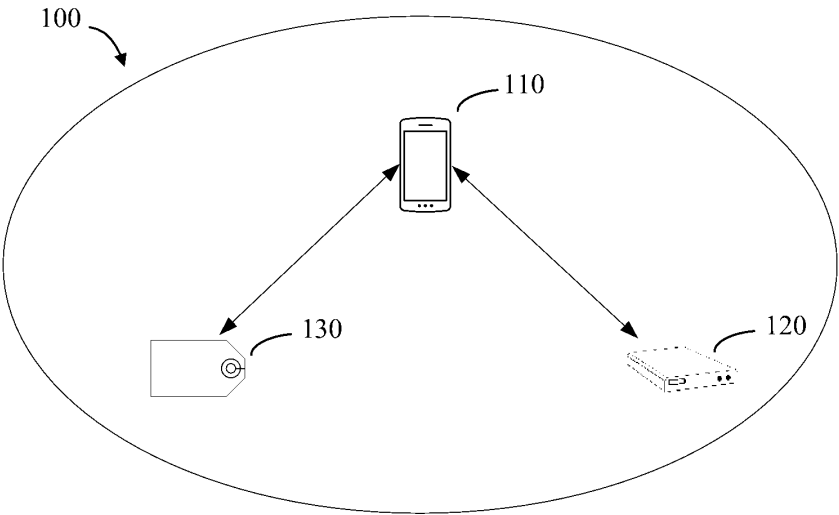


FIG. 1

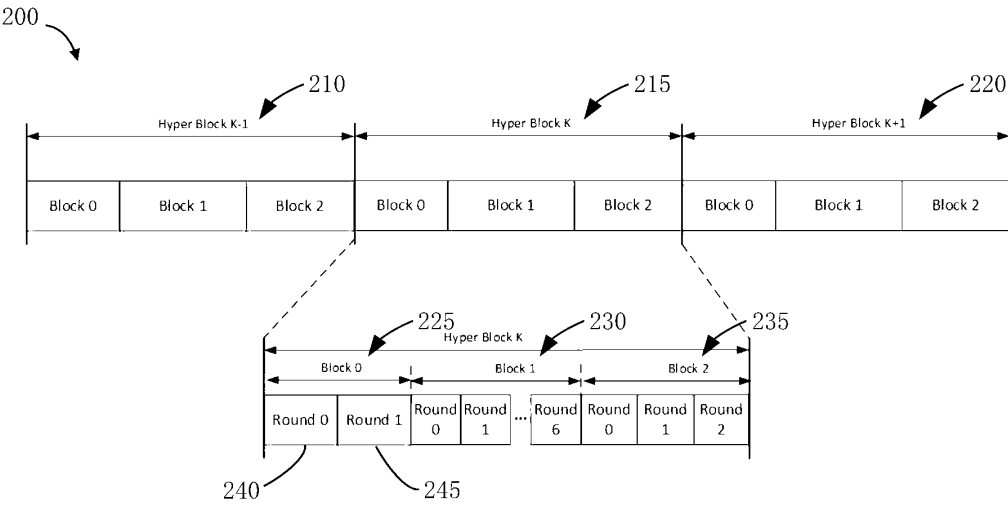


FIG. 2

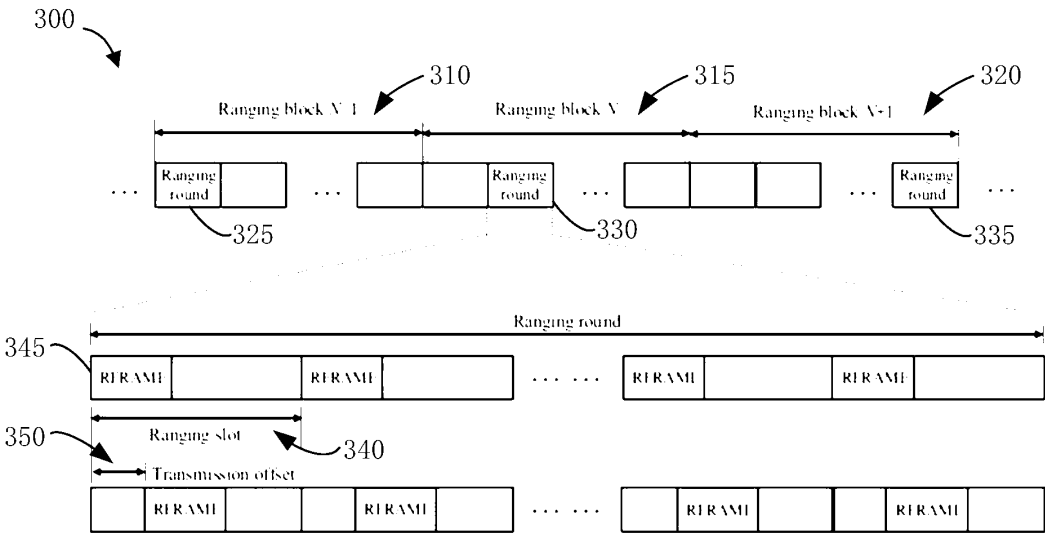


FIG. 3

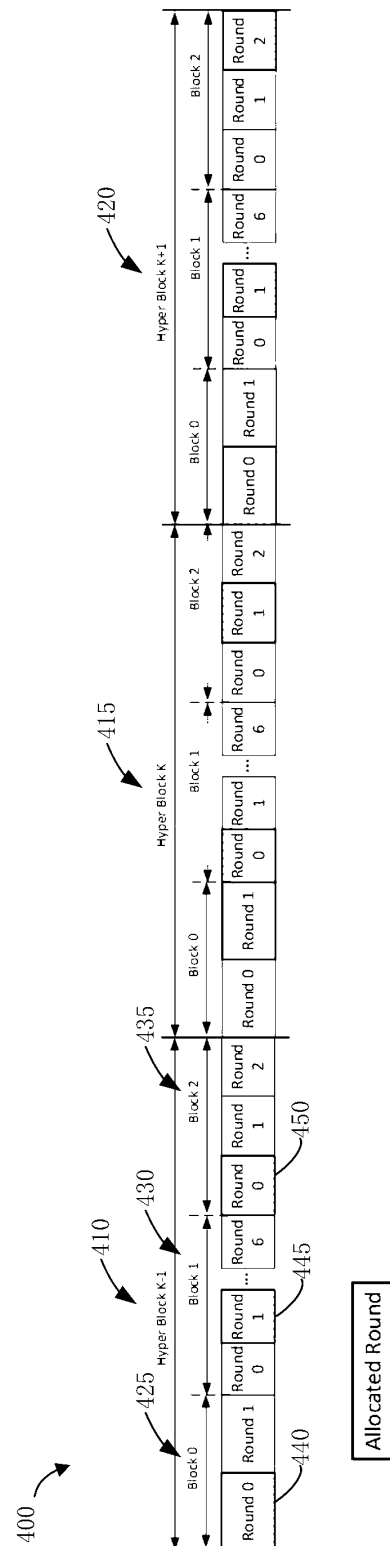


FIG. 4

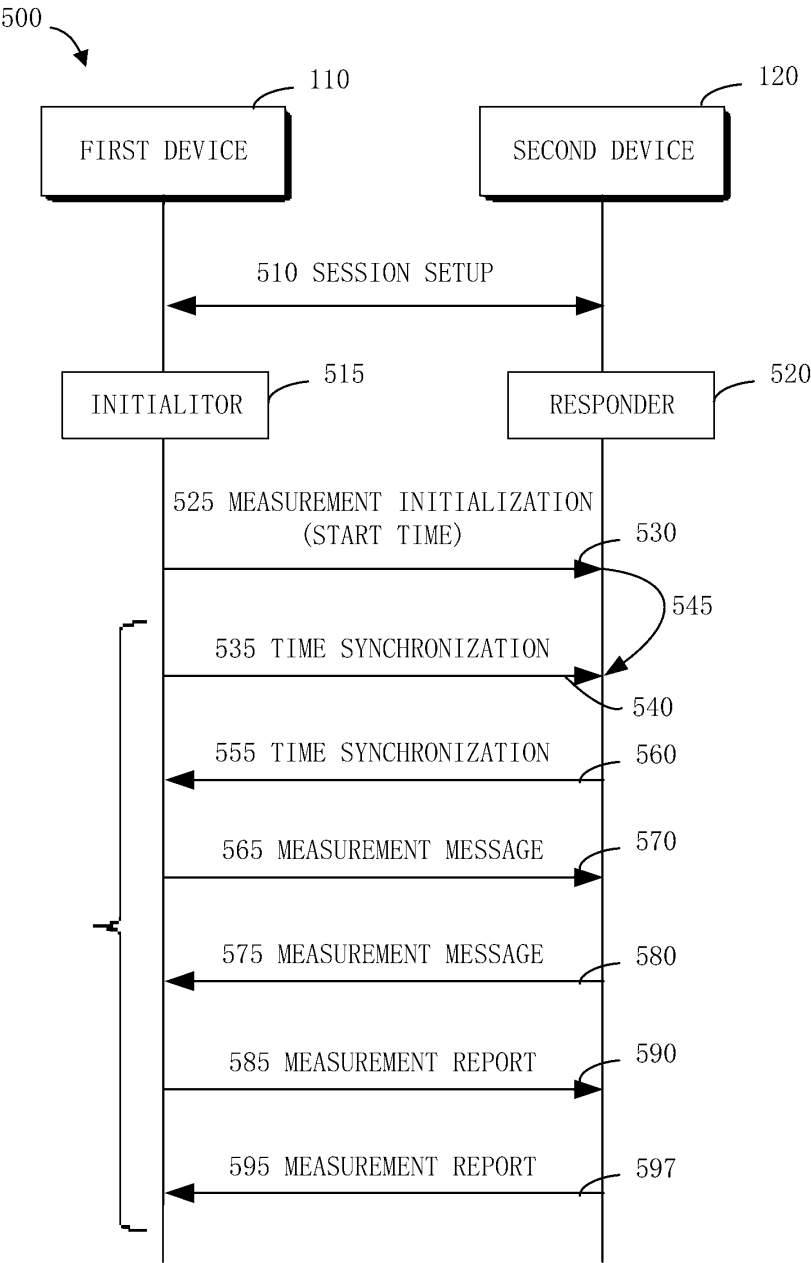


FIG. 5

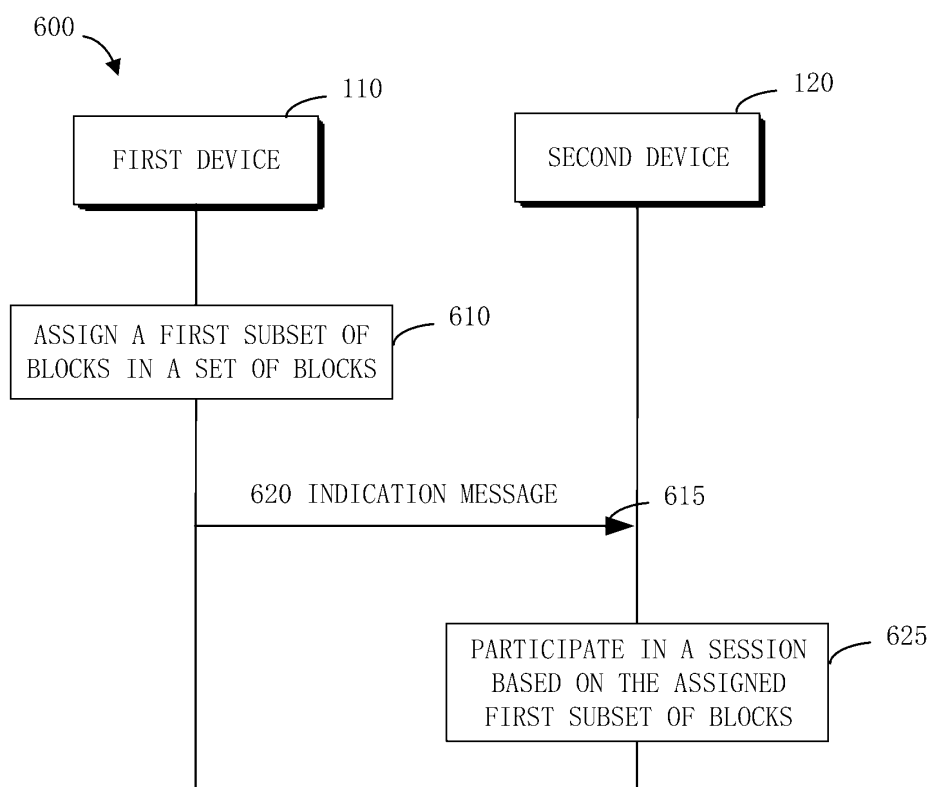


FIG. 6

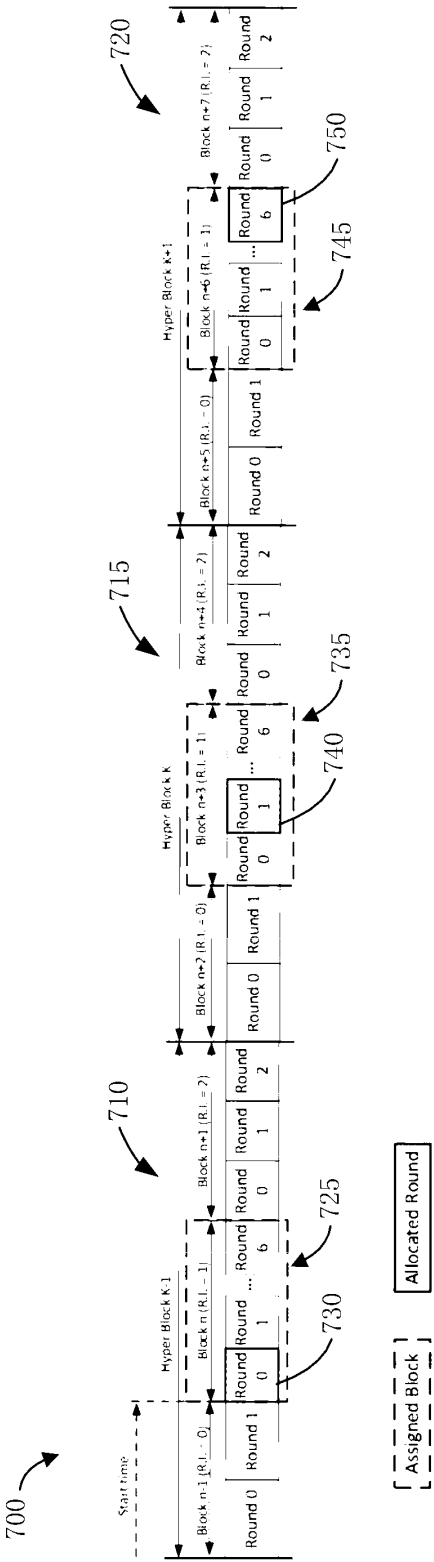


FIG. 7A

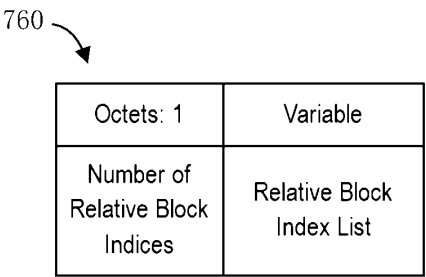


FIG. 7B

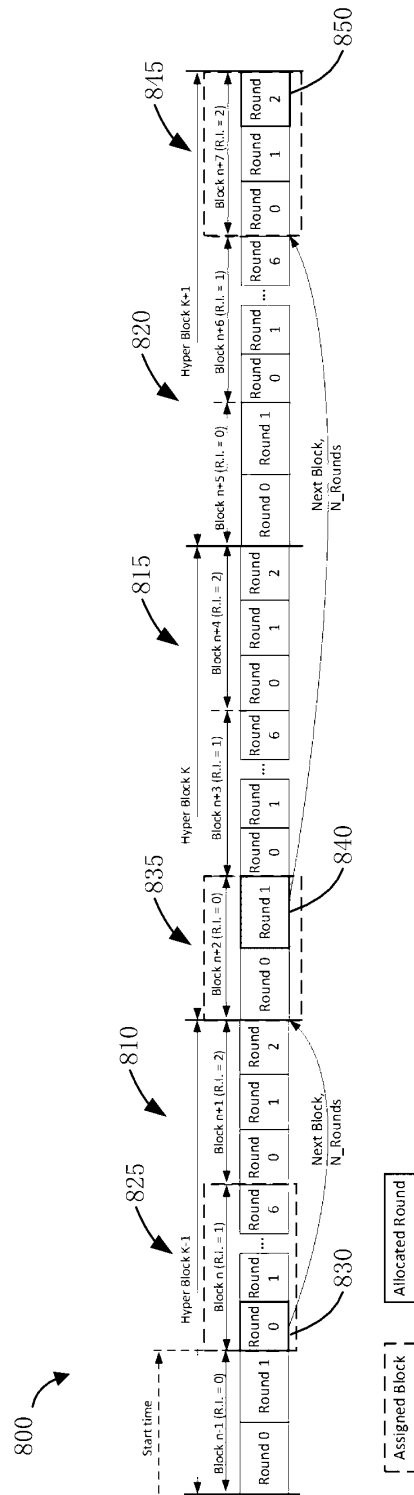


FIG. 8A

860

Octets: 2	0 1	variable	variable	variable		variable	2 4
Frame Control	Sequence Number	Addressing fields	Auxiliary Security Header	IEs		Data Payload	FCS
				Header IEs	Payload IEs		
MHR				MAC Payload			MFR

FIG. 8B

870

Octets: 1	1	Bits: 0	1 - 15	Octets: 2	1
Hyper Block Index	Relative Block Index	Hopping Mode	Round Index	Transmission Offset	Number of Rounds

FIG. 8C

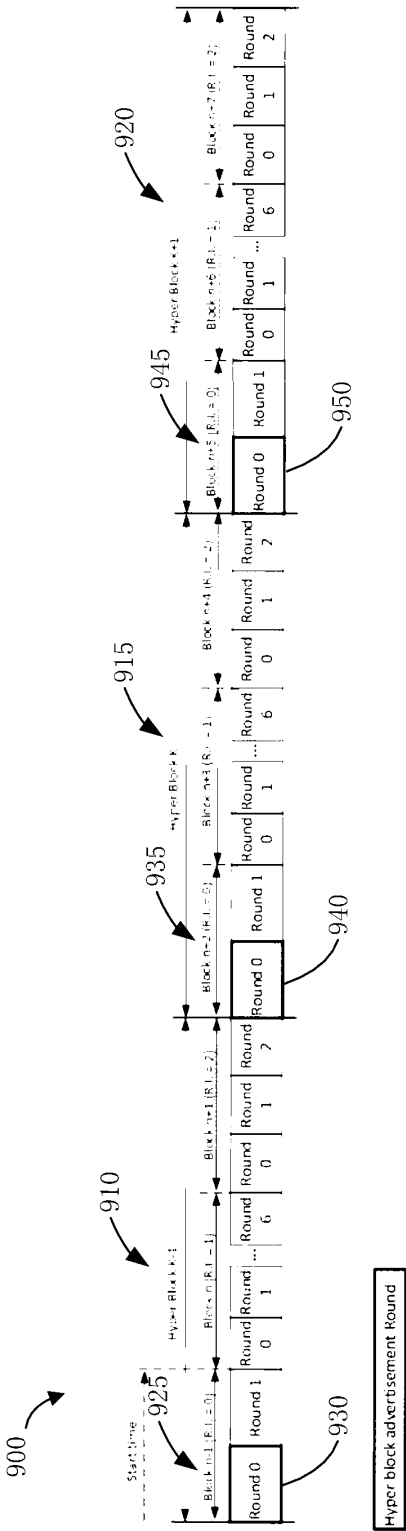


FIG. 9A

960

Octets:2	1	1	Variable
Hyper Block Index	Content Control	Block Description List Length	Block Description List

FIG. 9B

965

Bits: 2	1	1	4
Block Duration Units	Round Duration Presence	Slot Duration Presence	Reserved

FIG. 9C

970

Octets: 1	1/2/3	0/1	0/2	1	Variable
Block Index	Block Duration	Round Duration	Slot Duration	Block Assignment List Length	Block Assignment List

FIG. 9D

980

Bits: 0	1 - 7	Octets: Variable
Address Size	Address List Length	Address List

FIG. 9E

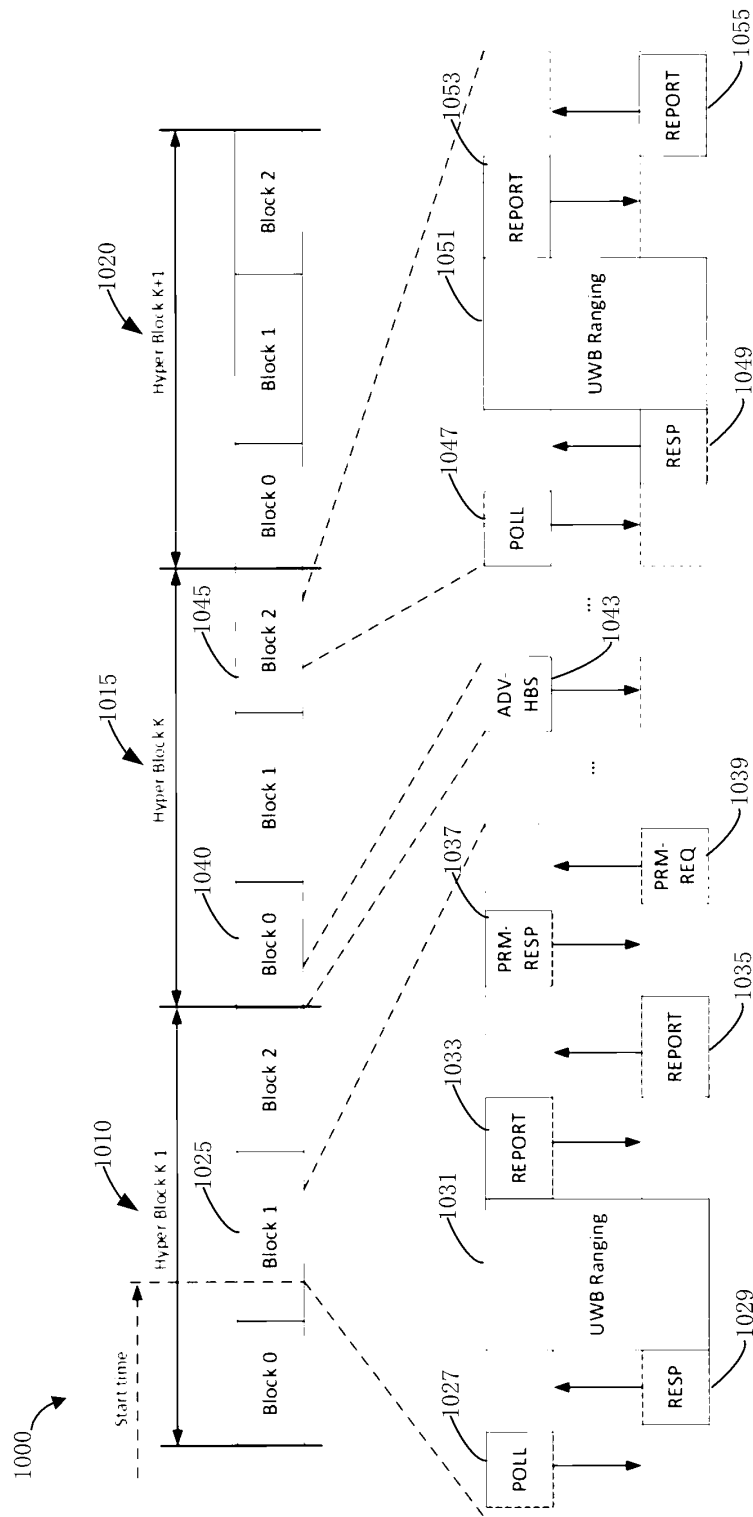


FIG. 10A

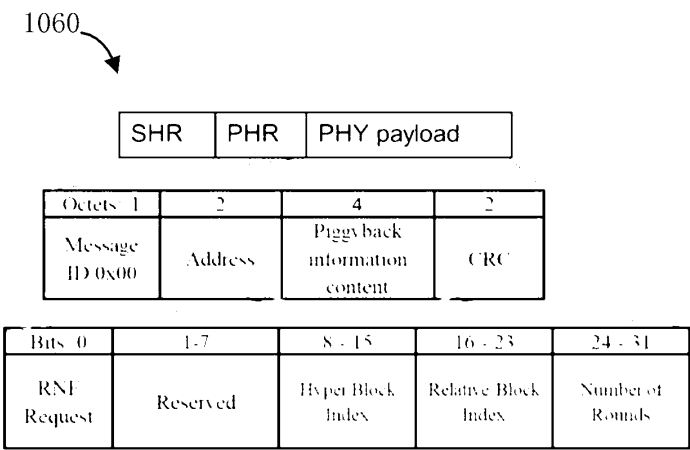


FIG. 10B

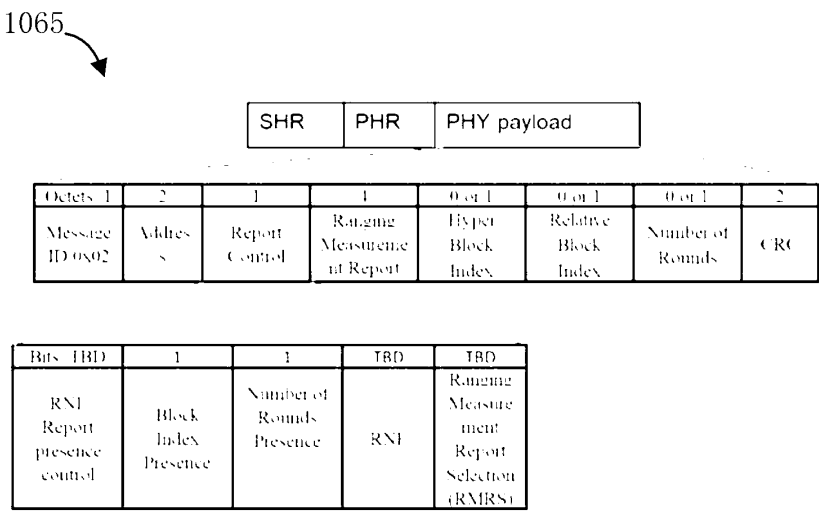


FIG. 10C

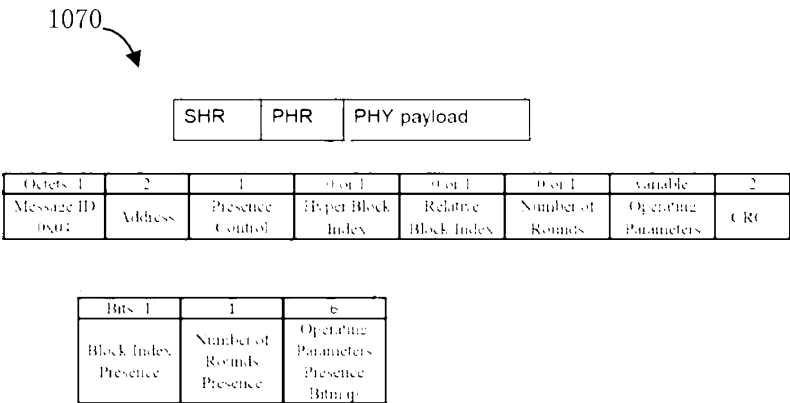


FIG. 10D

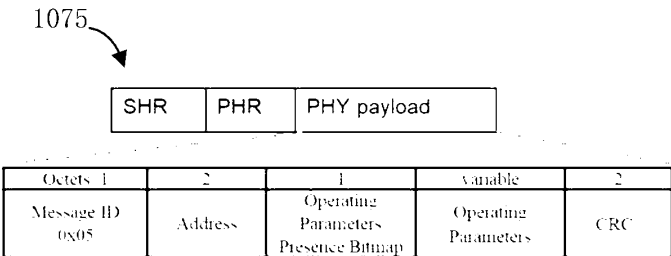


FIG. 10E

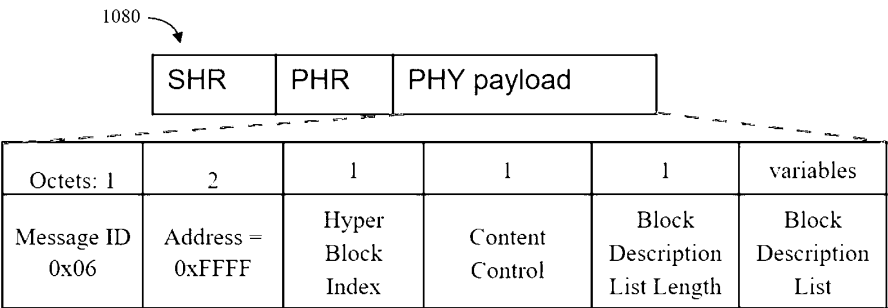


FIG. 10F

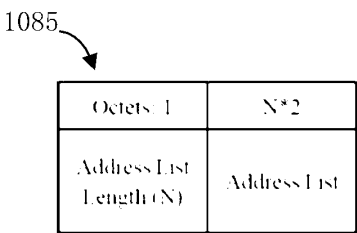


FIG. 10G

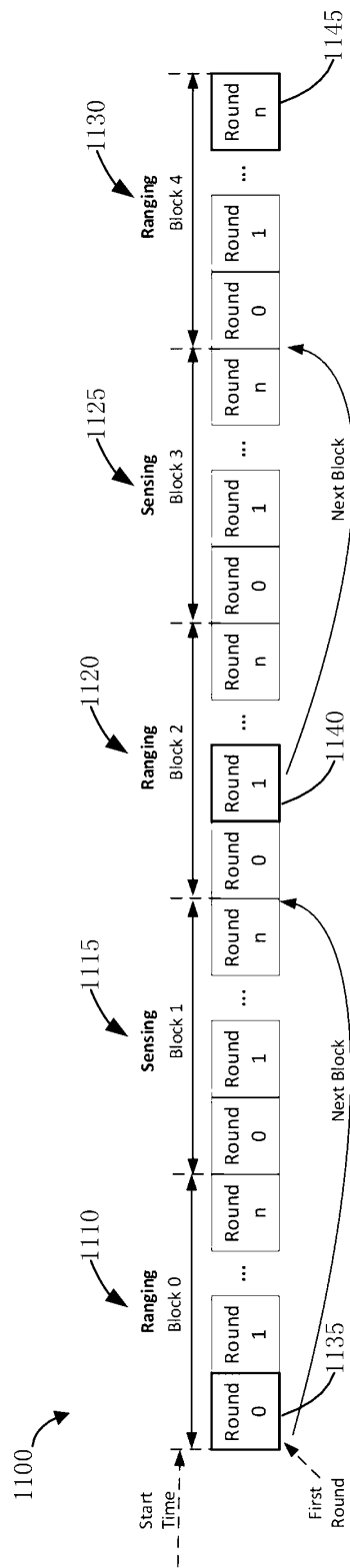


FIG. 11A

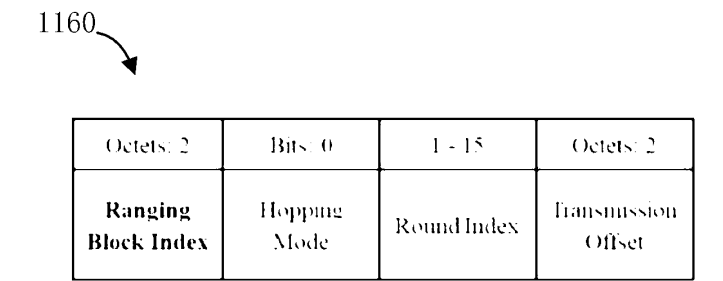


FIG. 11B

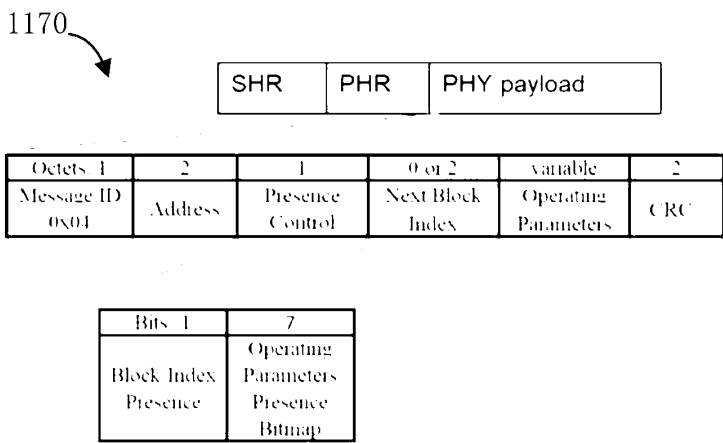


FIG. 11C

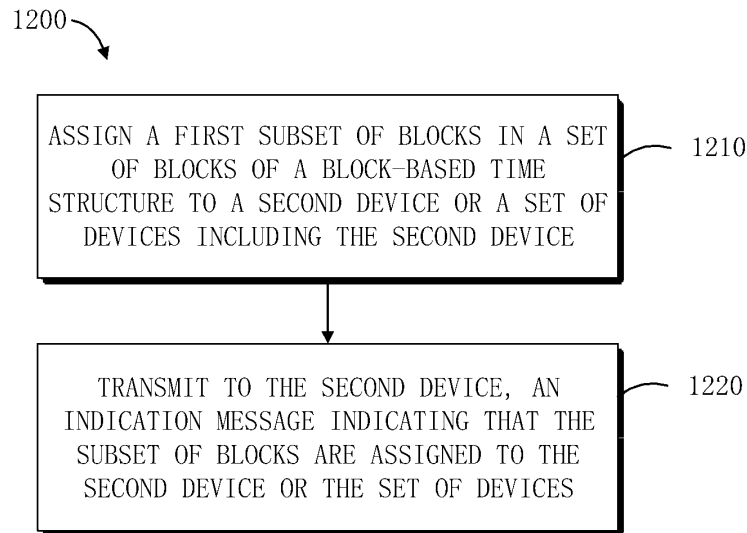


FIG. 12

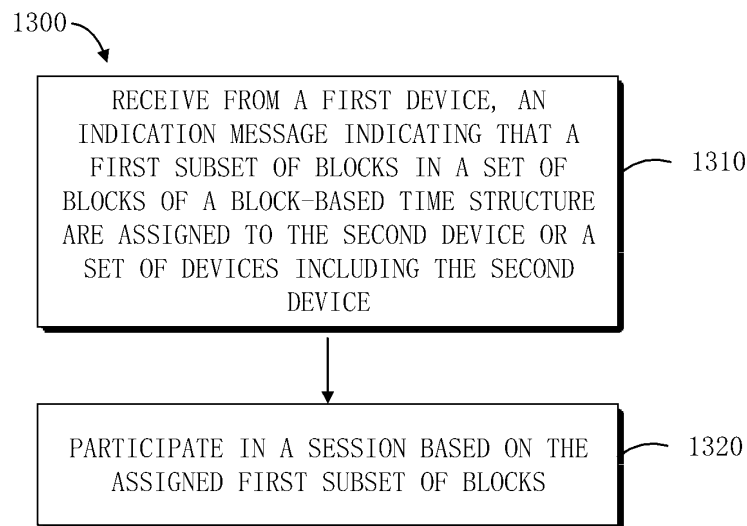


FIG. 13

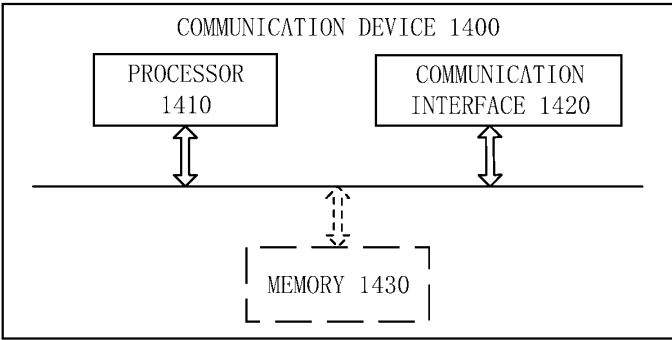


FIG. 14

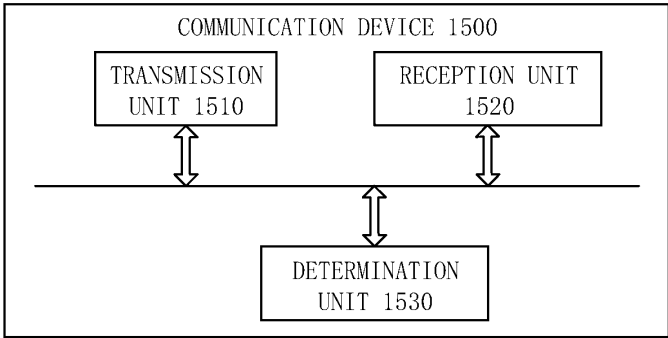


FIG. 15