

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
02 November 2023 (02.11.2023)



(10) International Publication Number
WO 2023/211777 A1

(51) International Patent Classification:

H01L 21/265 (2006.01) *H01L 29/786* (2006.01)
H01L 21/84 (2006.01) *H01L 21/02* (2006.01)
H01L 27/12 (2006.01) *H01L 21/8234* (2006.01)

(21) International Application Number:

PCT/US2023/019395

(22) International Filing Date:

21 April 2023 (21.04.2023)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

63/336,920 29 April 2022 (29.04.2022) US

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(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,
MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,

(54) Title: BACK-GATE EFFECT CONTROL VIA DOPING

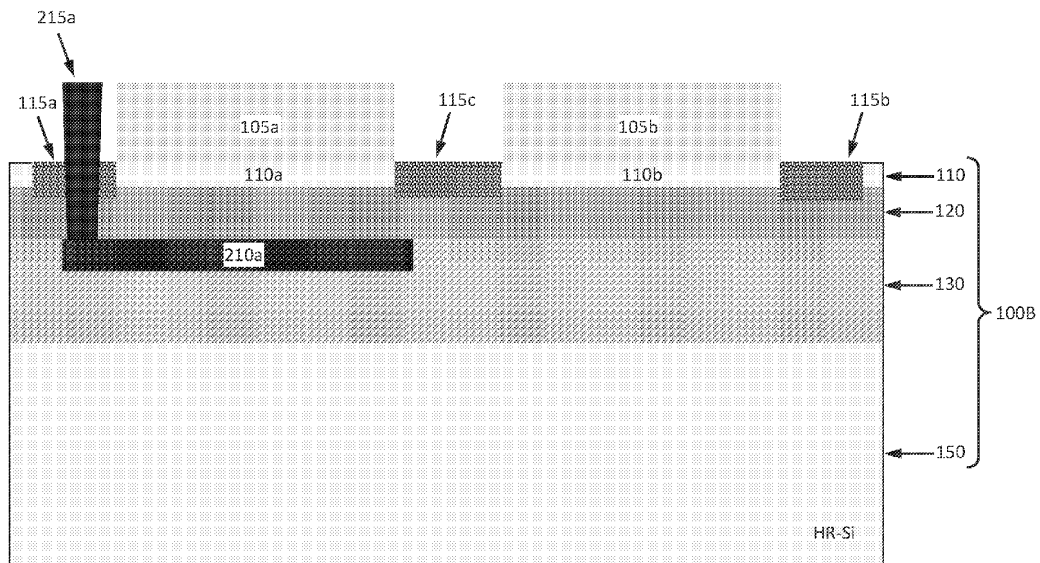


FIG. 2A

(57) Abstract: Methods and structures for mitigating back-gate effects in a radio frequency (RF) silicon-on-insulator (SOI) substrate, RF-SOI, are presented. According to one aspect, a first implant or junction is formed in a region of a trap-rich layer (TRL) of the RF-SOI that is located below a first circuit/device to protect. The first implant or junction is fully contained within the TRL. A planar surface area of the first implant and/or junction fully contains a projection of a planar surface area of the first circuit and/or device. The first implant or junction is biased via a through BOX contact (TBC) that penetrates the BOX layer at a shallow trench isolation region formed in the RF-SOI. According to another aspect, a second implant or junction is formed in a region of the TRL below a second circuit/device. The first and second implants or junctions are disjoint and separated by an undoped region of the TRL.

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NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))