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Devices for signal processing before and after transmission and/or storage with data rate reduction, and systems for transmitting and/or storing signals including such devices.

The present invention relates to an arrangement for processing signals which are grouped in periodic clusters, such as images, and intended to be transmitted and/or stored block-wise via a passband-limited information carrier which implies a reduction in the quantity of information components to be transmitted and/or stored, comprising

(a) a temporal sub-sampling sub-assembly provided to supply in a first transmission and/or storage mode, denoted compensated mode, a first sequence of signals to be transmitted and/or stored having a rate which is twice lower than that of the original signal clusters;

(b) a motion estimation sub-assembly for estimating motion between blocks which belong to consecutive periodical clusters, provided to supply block-wise a motion information to be transmitted and/or stored by replacing those blocks which are cancelled by said temporal sub-sampling;

(c) a recovering sub-assembly with motion compensation.

The invention also relates to a signal transmission and/or storage system comprising a transmission stage and, after transmission and/or storage of the signals transmitted via a passband-limited information carrier which implies a reduction processing of the quantity of information components to be transmitted and/or stored, a receiving and/or read stage for the transmitted and/or stored signals, and in which said transmission stage incorporates such a processing arrangement.

The invention also relates to an arrangement for processing previously transmitted and/or stored signals after a reduction of the quantity of information components to be transmitted and/or stored, effected either in accordance with a first compensated mode and with the aid of a temporal sub-sampling sub-assembly provided to supply a first signal sequence, or in accordance with a second fall-back mode and with the aid of a fall-back processing sub-assembly provided to add to said first sequence a second signal sequence synchronous with the first, the choice of said mode being effected with the transmission of a mode information component and with the aid

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of a decision-taking sub-assembly and on the basis of motion information components, which are also transmitted and/or stored, and a comparison of information components which are associated with either one or the other mode.

The invention further relates to an arrangement for processing previously transmitted and/or stored signals after a reduction of the quantity of information components to be transmitted and/or stored, effected either in accordance with a first compensated mode and with the aid of a temporal sub-sampling sub-assembly provided to supply a first signal sequence, or in accordance with a second fall-back mode and with the aid of a fall-back processing sub-assembly provided to add to said first sequence a second signal sequence synchronous with the first, with a spatial sub-sampling of said sequences, and for effecting the alternate selection of one or the other of these spatially sub-sampled sequences, the choice of said mode being effected with the transmission of a mode information component and with the aid of a decision-taking sub-assembly and on the basis of motion information components which are also transmitted and/or stored, and a comparison of the information components which are associated with either one or the other mode, respectively, with a view to selecting either the output of said motion-compensation subassembly or the output of said fall-back processing sub-assembly.

Finally, the invention relates to a signal transmission and/or storage system comprising a transmission stage and, after transmission and/or storage of the signals transmitted via a passband-limited information carrier which implies a reduction processing of the quantity of information components to be transmitted and/or stored, a receiving and/or read stage for the transmitted and/or stored signals.

This invention has a particularly interesting application in the case in which the signals to be processed include information components which represent animated images and in which a compact disc is used as the carrier of the transmitted and/or stored signals.

The transmission and/or storage of a very large quantity of information components, associated, for example, with images, generally implies a compression of the signals to be transmitted and/or stored, that is to say a reduction, in a predetermined ratio, of their number. The reduction ratio is inter alia determined by the fact that a sufficient quantity of signals must be preserved to avoid that the overall information they carry is not degraded too much, for example by the fact that one must preserve an

acceptable picture quality within the scope of the cited Application.

The majority of the currently known signal coding methods of realising this flow rate reduction is based on orthogonal transforms of the discrete cosine transform type, which allow a flow-rate reduction in a ratio of the order of 10 to 1. For a significant number of applications and, for example when used in storing and processing images on compact disc, this ratio is not sufficient and a complementary reduction processing in a ratio of 2 to 1 was found to be indispensable.

It is therefore an object of the invention to provide a signal processing arrangement which obviates previously found insufficiencies as regards the flow-rate reduction.

To this end the invention relates to a signal processing arrangement of the type defined in the opening paragraph, which is characterized in that it also includes:

(d) a fall-back processing sub-assembly provided to add block-wise to said first signal sequence, at least a second signal sequence which is in synchronism with the first and is supplied in accordance with a second fall-back mode substituting the first compensated mode as a function of the result provided by a decision-taking sub-assembly on the basis of a comparison between the original signals and the signals recovered by said recovering sub-assembly with motion compensation based on transmitted and/or stored blocks and on motion information components.

In this structure, the decision-taking sub-assembly includes, for example, a switch which is controlled by a decision circuit for selecting, in the compensated mode, only the output signals of the temporal sub-sampling sub-assembly, and in the fall-back mode, also the output signals of the fall-back processing sub-assembly.

The communication "HDMAC coding for compatible broadcasting of high definition television signals" presented by F.W.P. Vreeswijk et al. at the "16th International TV Symposium", Montreux (Switzerland), 17-22 June 1989, pp. 37-52, describes an arrangement for processing image signals in blocks intended to be transmitted and/or stored after data compression, particularly comprising three sub-sampling paths at 20 ms, 40 ms and 80 ms, a single path of which has its output signal selected for transmission. This transmission of the output signal of the 20 ms path or of the output signal of the 40 ms path or of the output signal of the 80 ms path effectively results in a decision taken as a function of the result of a comparison between the original signals and signals recovered after a motion estimation and compensation, but is

effected in accordance with a rhythm which is typical of each path, and corresponds to a respective sub-sampling structure adapted to the rates of displacement found in the images (80 ms path: stationary images or images showing slight motion; 40 ms path: images showing moderate motion; 20 ms path: images showing rapid motion). The "compensated mode" can be accepted as the mode of operation of this system when it is the output signal of the 40 ms path (and that only) which is selected (because in this case the transmitted signals are accompanied by motion information components with which those signals that have not been transmitted can be subsequently reconstructed), but on the other hand the modes of operation in which it is the output signal of the 20 ms path or that of the 80 ms path which is selected instead of the output signal of the 40 ms path can in no case be referred to as the "fall-back mode". The selection of one of the three paths is a choice of one out of three comparable modes of operation and the transmission of one of the output signals excludes that of the two others. In the present case, the arrangement has only two sub-sampling paths, but in accordance with the circumstances either only one or both have their output signal selected. This selection of one or two output signals of these paths results in taking a decision on whether the operation of the arrangement proceeds in accordance with a compensated mode, in which only one first signal sequence (at a frequency which is twice lower than that of the original signals before temporal sub-sampling) is transmitted and/or stored, or whether a fall-back mode, in which said first signal sequence is always present, is completed by a second sequence which is synchronous with the first.

In accordance with an advantageous embodiment, the fall-back processing sub-assembly includes a delay circuit producing a delay equal to the period of the original signals, followed by a temporal sub-sampling circuit operating at the same ratio as the ratio of the temporal sub-sampling sub-assembly.

In a further, still more improved embodiment, the fall-back processing sub-assembly also includes a spatial sub-sampling subassembly which comprises, in parallel, a first and a second spatial sub-sampling path in the same ratio as that of the temporal sub-sampling, the spatial sub-sampling matrix of each path being independent of the motion and being fixed but for the temporal resolution of the signals.

In the latter structure, the arrangement is preferably characterized in that:

(A) the spatial sub-sampling sub-assembly comprises, in each path, a spatial filtering circuit followed by a spatial sub-sampling circuit operating at a ratio

1/2, and, at the output of the two paths, a switching circuit provided to select alternately one or the other of the outputs of said spatial sub-sampling circuits at a frequency which is twice lower than that of the original signals;

(B) the decision-taking sub-assembly includes a changeover switch controlled to select, in the compensated mode, the output signals of the temporal sub-sampling sub-assembly or, in the fall-back mode, the output signals of said switching circuit.

In a further embodiment of the fall-back processing subassembly, the arrangement is also characterized in that:

(A) the fall-back processing sub-assembly includes, in parallel with said temporal sub-sampling sub-assembly, a spatial sub-sampling sub-assembly which comprises two parallel-arranged paths the first of which comprises a first spatial sub-sampling circuit and the second comprises, in series, a delay circuit producing a delay of one period of the original signals and a second spatial sub-sampling circuit, the spatial sub-sampling matrix of each path being independent of the motion and being fixed but for the temporal resolution of the signals, and said two parallel paths being preceded, in series, by a spatial filtering circuit and followed by a switching circuit provided to select alternately one or the other of the outputs of the spatial sub-sampling circuits, at a frequency which is twice lower than that of the original signals;

(B) the decision-taking sub-assembly comprises a change-over switch controlled by a decision circuit for selecting, in the compensated mode, the output signals of the temporal sub-sampling sub-assembly and, in the fall-back mode, the output signals of said change-over switch.

In the specific application in which the signals to be transmitted and/or stored are representative of images, the signal processing arrangement is characterized in that the selection in the decision-taking circuit is effected per image block and after interpolation error and fall-back error computations compared for selecting the smallest error.

When this application to image signals is used, the invention can be employed in a particularly advantageous manner when the carrier for the transmitted and/or stored signals is of the compact disc type.

A further object of the invention is to provide a processing arrangement for previously transmitted and/or stored signals, adapted, at the receiving side, to a

signal recovery without loss of information components with respect to the motion contained in the original signals.

To that effect the invention relates, in a first embodiment, to an arrangement which is characterized in that it comprises:

(a) a motion-compensation sub-assembly provided to receive the transmitted and/or stored signals corresponding to the output signals of said temporal sub-sampling sub-assembly;

(b) a change-over switch receiving at a first input the output of the motion-compensation sub-assembly and at a second input the transmitted and/or stored signals corresponding to the output signals of said fall-back processing sub-assembly and supplying from its output, in accordance with said mode information corresponding to the selection of the first or the second mode, either the signals present at said first input or the signals present at said second input, respectively;

(c) a change-over switch for alternately selecting, at a frequency which is twice as high as that of the input signals, either said output of this change-over switch, or the input of said motion-compensation sub-assembly but delayed by a half period of the rate of said input signals of the signal processing arrangement.

The invention also relates, in a variant constituting a second embodiment, to an arrangement which is characterized in that it comprises:

(a) a first sub-sampling and interpolation sub-assembly of the received signals corresponding to the previously transmitted and/or stored signals and constituting the input signals of the arrangement;

(b) a motion-compensation sub-assembly whose input is connected, in accordance with said selection of the first or the second mode, respectively, either directly to the input of said arrangement or to this same input but via said first sub-sampling and interpolation sub-assembly;

(c) a second sub-sampling and interpolation sub-assembly whose input is connected, in accordance with said selection of the first or the second mode, respectively, either to the output of said motion-compensation sub-assembly, or directly to the input of said arrangement;

(d) a change-over switch which supplies from its output or in accordance with said mode information corresponding to the selection of the first or second mode, respectively, either the output of said motion-compensation sub-assembly or the output

of said second sub-sampling and interpolation sub-assembly;

(e) a change-over switch for alternately selecting, at a frequency which is twice as high as that of the input signals, either said output of this change-over switch or the input of said motion-compensation sub-assembly but delayed by a half period of the rate of said input signals of the arrangement.

In the case of this second embodiment, the arrangement is preferably characterized in that the first and second sub-sampling and interpolation sub-assemblies each comprise a spatial sub-sampling circuit and a spatial interpolation circuit, and in that the motion-compensation sub-assembly comprises image memories and an adder, with a view to a motion-compensated interpolation on the basis of the output image of the first of these memories, of the input image of the second of these memories and of the motion information between said input and output images, the delay produced by each of said memories being equal to half the period of the input signals of the processing arrangement.

In one or the other of these structures, the arrangement is advantageously characterized in that the selection at the input of the motion-compensation sub-assembly and the selection at the input of the second sub-sampling and interpolation sub-assembly are effected with the aid of a first and d second change-over switch, respectively, which are controlled in accordance with said mode information.

Particulars and advantages of the invention will now become more apparent in a more detailed manner from the following description which is given, by way of non-limitative example, with reference to the accompanying drawings, in which:

- Fig. 1 shows a first example, in accordance with the invention, of an embodiment of the arrangement for processing signals intended to be transmitted and/or stored, after flow rate reduction;

- Fig. 2 shows, in this arrangement, an embodiment of the recovery sub-assembly with motion compensation and of the decision circuit of the decision-taking sub-assembly;

- Fig. 3 shows, in combination with Fig. 1, a further embodiment of the fall-back processing sub-assembly;

- Figs. 4a to 4c show three examples of transfer characteristics of the filtering circuits of the structure of Fig. 3, adapted to different sub-sampling matrices, respectively, such as those shown in Figs. 5a to 5c;

- Fig. 6 shows another example of the arrangement for processing signals;

- Fig. 7 is an embodiment, in accordance with the invention, of the arrangement for processing previously transmitted and/or stored signals after processing in an arrangement of the type corresponding to the arrangement shown in the associated Figs. 1 and 3, and shown in Figs. 7a, 7b, 7c for three different modes of operation.

In the application described here, the input signals have, for example, a repetition rate of 25 Hz and the processing arrangement for these signals must then supply signals at a rate of 12.5 Hz. This temporal sub-sampling by a factor of 2 is realised in the following manner, which is described in connection with mainly the Figs. 1, and 3.

The signal processing arrangement shown in Fig. 1 includes first of all a temporal sub-sampling sub-assembly provided for supplying, in accordance with a first transmission and/or storage mode referred to as compensated mode, a first signal sequence (to be transmitted and/or stored) of a frequency which is lower than the frequency of the original signals in a predetermined ratio. Here this sub-assembly consists of a temporal sub-sampling circuit 10'a operating at half a ratio. On the other hand the arrangement includes a motion estimation sub-assembly here formed by a motion estimation circuit 20. In this case, the temporal sub-sampling circuit 10'a is a change-over switch which is controlled at half the original repetition rate, that is to say at 12.5 Hz here, and which consequently cancels one signal image out of every two in the sequence of image signals, for example the even images. The motion estimation circuit 20 acts on the non-cancelled images, in this case the odd images. In the example described, it is assumed that the image information components are processed in blocks of 16 x 16 image signals. For each of these blocks, the circuit 20 looks for the direction of the motion so as to subsequently deduce an approximation of this block on the basis of the motion information thus obtained, denoted D, and of the content of two images adjacent to the cancelled image. The motion-information components must also be transmitted and/or stored, by replacing those blocks which are cancelled by the temporal sub-sampling operation. Fig. 1 shows an example of the motion estimation circuit comprising two image memories 21 and 22 and a block correlator 23.

Correlators of this type are already known, for example from the article by J.R. Jain and A.K. Jain, "Displacement measurement and its application in interframe image coding", IEEE Transactions on Communications, vol. COM-29, no.

12, December 1981, pp. 1799 to 1808. The motion estimation by correlation thus proposed has for its effect to determine a displacement vector D for each block of the cancelled image, for example $I_2$, in a sequence of images $I_1$, $I_2$, $I_3$, etc. ....) in such a manner that it is possible to deduce from this knowledge of D an approximation $I_2$ of the cancelled image from the half-sum of the non-cancelled images $I_1$ and $I_3$ surrounding it, in accordance with a relation of the type:

$$\hat{I}_2(X) = (1/2)(I_1(X-D) + I_3(X+D))$$

wherein X is the spatial index of the current pixel, $I_1$, $I_2$, $I_3$, the original images, D the shift (in pixels), and $I_2$ the searched approximation of the intensity of the pixel X of the current block of the cancelled image.

Expressed in other terms, this motion estimation is a search for each block, represented by a current pixel X, a vector D in such a manner that the expression:

$\Sigma\ (DFD(X,D))^2$ for the totality of blocks is minimal. In this expression, DFD, which is an abbreviation of the term "Display Frame Difference", is the approximation error linked with the current block and is equivalent, for this block, to the sum of the square of the approximation errors over all the pixels of the block. Consequently, this approximation error is expressed as:

$$\Sigma\ (I_2(X) - (1/2)(I_3(X+D) + I_1(X-D))^2$$

(blocks)

and for this expression the minimal value is searched. The selected displacement vector is the vector which is associated with this minimal value, after an exhaustive test of all the possible displacement vectors in a search range limited by horizontal and vertical values $D_x$ and $D_y$, respectively.

The signal processing arrangement also includes a fall-back processing sub-assembly which is intended to take over the operation in the compensated mode when the motion estimation sub-assembly is omitted in accordance with a predetermined criterion which will be described in greater detail hereinafter. In a general manner, the normal mode of operation is the motion estimation mode, which will allow a subsequent motion compensation and which will consequently be referred to as the compensated mode, and this normal mode may in certain situations be replaced by a mode referred to as the fall-back mode. This fall-back processing sub-assembly comprises a delay circuit 50, this delay here being equal to the period of the original signals, and a temporal sub-

sampling circuit 10"a operating in the same ratio as the ratio of the circuit 10'a.

The signal processing arrangement also includes a recovery sub-assembly with motion compensation intended to supply, on the basis of a portion of those blocks which, in the original signals, induce the transmission and/or storage in accordance with the compensated mode and motion information components associated with said blocks by replacing the cancelled blocks, the signal blocks such as they will be recovered, on reception, by replacing the non-transmitted blocks, on the basis of the transmitted signal sequences and transmitted motion information components. Here this sub-assembly includes, as shown in Fig. 2, image memories 91a, 91b and 92, and also an adder 93. These elements render it possible to effect a motion-compensated interpolation, by a half-sum of the image $I_1$ (present at the output of the memory 91a while taking into account the displacement vector D selected by the motion estimation circuit 20) and the image $I_3$ (present at the output of the memory 92 while also taking D into account), the addresses in these memories 91a and 92 being shifted, by -D in the memory 91a and by +D in the memory 92. The motion-compensated image resulting from this interpolation is supplied by the adder 93.

Finally, the signal processing arrangement includes a decision-taking sub-assembly, which here comprises a change-over switch 80 a which is controlled by a decision circuit. In the example described here (see Fig. 2), the decision circuit (94 to 103) is more specifically formed in the following way. A subtracter 94, which subtracts the image $I_2$, present at the output of the memory 91b, from the motion-compensated image present at the output of the motion-compensation recovery sub-assembly (that is to say, at the output of the adder 93), and a means 95 for squaring the output of this subtracter 94 which together form an interpolation error computing circuit (94, 95) operating in the motion-compensation mode. This interpolation error is computed for each block. A circuit (96, 97, 98, 99, 100, 101, 102, 103) similarly allows an error computation in the fall-back mode, and to this end includes spatial filtering circuits (96, 97) and (98, 99) of the image $I_3$, each comprising a spatial filter 96 or 98 and a subtracter 97 or 99, thereafter means 100 and 101 for squaring the output signals of said spatial filtering circuits, an adder 102 which produces the half-sum of the output signals of these squaring means 100 and 101, and a comparator 103 comparing the output signals of the squaring means 95 and of the adder 102. This comparator 103 selects that output signal which is the weakest and for each image block supplies a

corresponding mode information: the compensated mode if the output of the squaring means 95 is selected, and the fall-back mode in the opposite case.

The mode of operation of the arrangement shown in Fig. 1 is as follows. In accordance with the first transmission mode (compensated mode), the temporal sub-sampling sub-assembly - in this case the circuit 10'a - supplies a first signal sequence. As the ratio of the temporal sub-sampling is equal to 1/2 in the example described, the frequency of these signals is equal to 12.5 Hz, as has already been described. In accordance with the second transmission mode (fall-back mode) a second signal sequence which is in synchronism with the first signal sequence is also transmitted, namely the output signals of the temporal sub-sampling circuit 10"a. Thus, the normally transmitted signals are the blocks available at the output $S_1$, and the fall-back blocks present at the output $S_2$ are adjacent thereto (when the decision circuit 90 controls closure of the change-over switch 80'a).

In a variant of the embodiment, the fall-back processing sub-assembly also includes a spatial sub-sampling subassembly. The latter, shown in Fig. 3, comprises a first and a second spatial sub-sampling path which is arranged in series with the outputs $S_2$ and $S_1$, respectively. The first path includes a spatial filtering circuit 30'a and a first spatial sub-sampling circuit 40a which operate at a ratio 1/2 (for example a staggered sub-sampling, or rather an orthogonal sub-sampling). The second path includes a spatial filtering circuit 30"a which is identical to the preceding circuit and a second spatial sub-sampling circuit 60a operating at a ratio 1/2, the latter sub-sampling being similar or complementary to the sub-sampling effected by the circuit 40a, that is to say in the case of the cited sampling matrix examples, the staggered sub-sampling or the identical or complementary orthogonal sub-sampling operation.

Examples of filtration effected by the spatial filtering circuits are shown in Figs. 4a to 4c in accordance with the nature of the sampling matrix: if $f_p$ and fo are the horizontal frequencies (pixels) and vertical frequencies (rows), respectively, of the image, Fig. 2a shows the filtering mode effected for the case of a staggered sub-sampling operation such as the one shown in Fig. 5 (the crosses and dots represent the preserved pixels and the cancelled pixels, respectively, during the sub-sampling operation), in Fig. 4b for the case of a vertical orthogonal sub-sampling operation (one row out of two is omitted, as shown in Fig. 5b), and in Fig. 4c for the case of a horizontal orthogonal sub-sampling operation (one pixel out of every two pixels of each

row is omitted, in vertically aligned positions as shown in Fig. 5c).

The spatial sub-sampling sub-assembly also includes, at the output of the two parallel paths, a switch 70a whose output alternately receives either the output of the spatial sub-sampling circuit 40a, or the output of the spatial sub-sampling circuit 60a. Thus, on the basis of samples of two consecutive images, a complete image is available at the frequency of 12.5 Hz at the output of the change-over switch 70, this image being obtained by mixing two previously filtered images.

For the case of this variant shown in Fig. 3, the decision-taking sub-assembly includes a second change-over switch 80''a intended to select, under the control of the decision circuit 90, in the compensated mode, the output signals of the temporal sub-sampling circuit 10'a or, in the fall-back mode, the output signals of the switch 70a. This selection is effected, as previously, block-wise, by considering blocks of 16 x 16 or blocks of 8 x 8 (without these examples being limitative). For each block it is again one of the two modes which subsequently allows an image recovery with a minimal error chosen by the decision circuit.

The embodiment of the fall-back processing sub-assembly corresponding to the combined Figs. 1 and 3 is not the only possible one. Fig. 6 shows a variant of the embodiment of the signal processing arrangement in which this arrangement includes, as in the preceding cases, a temporal sub-sampling sub-assembly, which is here a temporal sub-sampling circuit 10b operating at a ratio of 1/2 (identical to the circuits 10'a and 10''a), a motion estimation sub-assembly 20, a motion-compensation recovery sub-assembly, and a decision-taking sub-assembly, as well as a fall-back processing sub-assembly which, however, is realised in the following manner. This sub-assembly includes a spatial filtering circuit 30b which is intended to limit the passband of the signals, then followed by two parallel-arranged paths, the first of which includes a first spatial sub-sampling circuit 40b sampling at a ratio of 1/2 (for example a staggered sub-sampling or rather an orthogonal sub-sampling), and the second path includes a delay circuit 50b and a second spatial sub-sampling circuit 60b sampling at a ratio 1/2. The delay produced by the circuit 50b is equal to the period of the original signals (here 25 Hz). The spatial sub-sampling realised by the circuit 60b is similar or complementary to the spatial sub-sampling realised by the circuit 40b, that is to say in the case of the sampling matrix examples cited, the staggered sub-sampling or the identical or complementary orthogonal sub-sampling. The fall-back processing sub-

assembly comprises, at the output of the two parallel paths, a switch 70b whose output receives alternately either the output of the spatial sub-sampling circuit 40b, or the output of the spatial sub-sampling circuit 60b. Thus, at the output of the switch 70b, there is available, from the samples of two consecutive images, a complete image at the frequency of 12.5 Hz, obtained by mixing two previously filtered images. The decision-taking sub-assembly, this time includes a change-over switch 80b which is controlled by the decision circuit 90 to select, in the compensated mode, the output signals of the temporal sub-sampling circuit 10b or, in the fall-back mode, the output signals of the switch 70b.

It will here be noted that the invention is not limited to the processing arrangements described, but that it also relates to any transmission and/or signal storage system which on the one hand includes a stage intended to transmit information components which are representative of these signals towards a transmission or storage information carrier for these information components, and on the other hand a stage intended to receive information components thus transmitted and/or to read the information components thus stored: in the case in which this information carrier is of the limited passband type and in which a processing operation to reduce the quantity of information components before transmission and/or storage has proved to be necessary, the invention relates to such a system when its transmission stage includes one of the above-described signal processing arrangements.

Conversely, when the information components have been processed by a signal processing arrangement of the type described in the foregoing, the signals are subsequently recovered at the original time rate. This operation can then be realised by means of a postprocessing operation which will now be described with reference to Fig. 7 for the case in which a spatial sub-sampling has been effected on transmission. The structure of the arrangement in the absence of such a spatial sub-sampling upon transmission can then easily be deduced from this Fig. 7.

The signal processing arrangement shown in Fig. 7 in three distinct situations corresponding to Figs. 7a, 7b and 7c, respectively, and explained hereinafter, receives, in the example described, input images at the frequency of 12.5 Hz (which consequently follow each other every 80 ms) and, at the output of the arrangement, images at the frequency of 25 Hz. The input images are accompanied by motion information components D and information components M relative to the mode (motion-

compensated mode or fall-back mode), these motion and mode information components being also transmitted and/or stored by means of said information carrier (see Fig. 1 or Fig. 6).

The processing arrangement shown in Figs. 7a to 7c then includes, first of all, a motion compensation sub-assembly which comprises image memories 201a, 201b and 202 and an adder 203. This motion compensation sub-assembly is preceded by a change-over switch 110 which directly receives the input images at a first input terminal and these same input images at a second input terminal but via a first sub-sampling and interpolation sub-assembly. This first sub-sampling and interpolation sub-assembly includes a first spatial sub-sampling circuit 211 and a first spatial interpolation circuit 212, which is adapted to the sub-sampling mode employed in the circuit 211. The change-over switch 110 receives for each image block the mode information and, as a function thereof, changes to the position of direct connection to the input (motion compensation mode, denoted C at the corresponding input of the change-over switch 110) or, in contrast, to the opposite position (fall-back mode, denoted R at the corresponding input of the change-over switch 110), to select in this position the output signals of the first sub-sampling and interpolation sub-assembly.

The processing arrangement shown in Figs. 7a to 7c also includes a second sub-sampling and interpolation sub-assembly, which includes a second spatial sub-sampling circuit 221 and a second spatial interpolation circuit 222, which are identical to the circuits 211 and 212, respectively. This second sub-sampling and interpolation sub-assembly (221, 222) is preceded by a change-over switch 120 and is followed by a change-over switch 130. The change-over switch 120 receives at a first input terminal the output signals from the motion compensation sub-assembly, and at a second input terminal directly the input images, and, in accordance with the mode information received, selects either the motion-compensated signals (motion compensation mode, denoted C), or the input images (fall-back mode, denoted R). At a first input terminal the change-over switch 130 also receives the output signals of the motion compensation sub-assembly, and at a second input the output signals of the second sub-sampling and interpolation sub-assembly, and, in accordance with the mode information received, selects either the motion-compensated signals, (motion compensation mode, denoted C), or the output signals of the second sub-sampling and interpolation sub-assembly (fall-back mode, denoted R).

The processing arrangement of Figs. 7a to 7c finally includes a change-over switch 250 which, at a twice higher rate than the input images (at the frequency of 25 Hz in the present case, since the input images here have a frequency of 12.5 Hz), alternately selects the output of the change-over switch 130 or that of the image memory 201b.

The mode of operation of this processing arrangement will now be described for three situations which can be met, with reference to the corresponding Figures 7a to 7c. First it should be remembered that the input images of the arrangement may be constituted by processed image blocks, before transmission and/or storage, either in accordance with the motion compensation mode, or the fall-back mode, or also in accordance with one or the other of these two modes, these three alternatives corresponding to said three situations.

Let it first be assumed (first situation, shown in Fig. 7a) that the input images are exclusively formed by processed image blocks, before transmission and/or storage, in accordance with the motion compensation mode. The information of the corresponding mode then keeps the three change-over switches 110 to 130 in their position C. If, moreover, the sequence of input images is denoted $I_1$, $I_3$, $I_5$, $I_7$, etc. ... and at a considered instant $t_c$ the image $I_1$ (compensated by -D) is available at the output of the image memory 201a, at the same instant the image $I_3$, which appeared 80 ms after $I_1$, is available at the input of the image memory 201b. The change-over switch 250 then selects, in its position denoted IC, the output of the adder 203 of the motion compensation sub-assembly. The image denoted $I_2$ available at this output is the image having a parity opposite to that of the images $I_1$ and $I_3$ and is recovered, between these two images, at 40 ms from each of them, by the half-sum of these images $I_1$ and $I_3$ and takes the direction of the displacement vector D (which was previously selected and applied to said motion compensation subassembly) into account. At the frequency of 25 Hz, that is to say 40 ms later, the change-over switch 250 has changed state and, in its position denoted IT, selects the output of the memory 201b, this output now being $I_3$ since $I_3$ appeared 40 ms earlier at the input of the memory 201b.

The same change-of-state cycle then proceeds, and the change-over switch 250 thereafter selects the image $I_4$ which is the weighted average of $I_3$ and $I_5$ in the direction of the new selected displacement vector, thereafter the image $I_5$, then $I_6$, $I_7$, $I_8$, $I_9$ etc. ... . Finally, at the output of the changeover switch 250 and consequently of

the processing arrangement of Fig. 7a an image sequence of the type $I_1$, $I_2$, $I_3$, $I_4$, $I_5$, $I_6$, $I_7$, etc. ..., is available at a frequency which is twice as high as the frequency of the input images.

Let it now be assumed (second situation, shown in Fig. 7b) that the input images are exclusively formed by processed image blocks, before transmission and/or storage, in accordance with said fall-back mode. The corresponding mode information this time maintains the three change-over switches 110 to 130 in their position R. The spatial sub-sampling circuit 211 sub-samples the determined parity images (for example odd images, that is to say the images $I_1$, $I_3$, $I_5$, etc. ... ) in accordance with the same sampling matrix as that used during the processing operation at the transmission end, thereafter, the spatial interpolation circuit 212 recovers the missing samples. If for an input image $I_3$, the image available at the output of the circuit 212 of the first sub-sampling and interpolation sub-assembly is denoted $I_{3R}$, it will then be found that, now, the image $I_{3R}$ is substituted for the input image $I_3$.

Similarly, the spatial sub-sampling circuit 221 and the spatial interpolation circuit 222 ensure the sub-sampling of the images having an opposite parity (for example the even images $I_2$, $I_4$, $I_6$, etc. ....), in accordance with the same phase of the sampling matrix as that previously employed, and the recovery of the missing samples, respectively. For an input impage $I_3$, this image recovered at the output of the circuit 222 of the second sub-sampling and interpolation sub-assembly is now denoted $I_{2R}$. The change-over switch 250 then selects in its position IC the image designated $I_{2R}$ available at the output of the said second sub-assembly and, in its position IT, the image designated $I_{3R}$, available 40 ms earlier at the output of the first sub-sampling and interpolation sub-assembly and now available at the output of the image memory 201b. This time, an image sequence of the type $I_{1R}$, $I_{2R}$, $I_{3R}$, $I_{4R}$, $I_{5R}$, etc. .... , is available at the output of the processing arrangement of Fig. 7b, always at a frequency which is twice the frequency of the input images.

Let it finally be assumed (third situation shown in Fig. 7c, and in general the most frequently occurring situation) that the input images are recovered simultaneously from image blocks processed at the transmission end in accordance with the motion compensation mode, and image blocks processed at the transmission end in accordance with the fall-back mode. The mode information, corresponding to each of these two modes, then switches the three change-over switches 110, 120, 130,

alternately to their position C or to their position R, according to the processing type to which the image blocks appearing at the input of the processing arrangement were previously submitted: the processing operations effected in this arrangement will then be those processing operations effected in the case of the first or the second situation, as the case may be.

Actually, in the case of the fall-back mode blocks, the first sub-sampling and interpolation sub-assembly (211, 212) consecutively ensures the recovery of the samples of the images of a predetermined parity (odd, for example) and the recovery of the missing samples. The blocks $I_{3R}$ available at the output of said first sub-assembly are then reinserted by the change-over switch 110 into the input image $I_3$, to form the future output image called $I_{3CR}$. Similarly, for the case of fall-back mode blocks, the second sub-sampling and interpolation sub-assembly (221, 222) ensures the recovery of the images of the opposite parity (here the even images), by processing the output signals of the change-over switch 120, which in this third situation, has for its function to insert the compensated blocks $I_2$ (available in the manner already described, at the output of the motion compensation sub-assembly 201a to 203) into the input image $I_3$. The image thus formed at the input of said second sub-assembly is designated $I_2$", and the image at the output is designated $I"_{2R}$. The change-over switch 130 then renders it possible to complete the future output image $I_{2CR}$ by selecting, as a function of the mode information it receives and which controls its position, either the compensated output blocks $I_2$ of the motion compensation sub-assembly, or the interpolated output blocks $I"_{2R}$ of the second sub-sampling and interpolation sub-assembly.

Then, in this third situation the change-over switch 250 can now select either, in its position denoted IC, the output image $I_{2CR}$ of the change-over switch 130, or, in its position IT, the image $I_{3CR}$ available 40 ms earlier at the output of the change-over switch 110 and now present at the output of the image memory 201b. Again, at the output of the processing arrangement of Fig. 7c, a sequence of images of the type $I_{1CR}$, $I_{2CR}$, $I_{3CR}$, $I_{4CR}$, $I_{5CR}$, etc. .... is available again at a frequency which is twice the frequency of the input images.

The arrangement for processing signals after transmission and/or storage described in the foregoing with reference to Fig. 7 corresponds to the arrangement for processing signals before transmission and/or storage described in association with the combined Figs. 1 and 3. In the absence of the spatial sub-sampling on transmission (that

is to say, with only the fall-back processing sub-assembly as shown in Fig. 1) the processing arrangement of Fig. 7 is simplified in the following manner. On the one hand, the two sub-sampling and interpolation sub-assemblies (211, 212) and (221, 222), are omitted, and also the corresponding change-over switches 110 and 120. On the other hand, taking this suppression into account, the signals corresponding to the signals $S_1$ and $S_2$ of Fig. 1 are now, applied to the input of the motion compensating sub-assembly, (common input of the memories 201b and 202) and to the input R of the change-over switch 130, respectively. These modifications which can easily be understood from Fig. 7, are therefore not shown.

It should be noted that the present invention is not limited to the examples described, on the basis of which variants can be proposed without departing from the scope of the invention. Some of these variants have already been mentioned. It will also be noted that the criterion used to determine whether the motion estimation circuit 20 is lacking and must be replaced by the fall-back processing sub-assembly may correspond to a large range of situations. The main criterion which can be maintained is, for example, the fact that the motion is either too fast or not too fast and that the motion estimation circuit then moves outside its operating range. But it is also possible to provide a trigger control in the fall-back mode when the noise becomes too great and results in estimation errors, or when operations are effected in an image zone where the objects have opposite motions and put the motion estimation circuit out of order.

Moreover, it is obvious once again that the invention is not limited to the processing arrangements described hereinbefore, but that it also relates to any transmission and/or signal storage system comprising on the one hand a stage intended to transmit information components representative of these signals to a transmission or storage carrier of these information components, and on the other hand a stage intended to receive the information components thus transmitted and/or to read the information components thus stored: in the case in which this information carrier has a limited passband and in which a processing operation for reducing the quantity of information components before transmission and/or storage proves to be necessary, the invention also relates to such a system when its receiving stage includes one of the signal processing arrangements as described hereinbefore.

# CLAIMS

1. An arrangement for processing signals which are grouped in periodic clusters, such as images, and intended to be transmitted and/or stored block-wise via a passband-limited information carrier, which implies a reduction in the quantity of information components to be transmitted and/or stored, comprising:

(a) a temporal sub-sampling sub-assembly provided to supply in a first transmission and/or storage mode, denoted compensated mode, a first sequence of signals to be transmitted and/or stored, having a rate which is twice lower than that of the original signal clusters;

(b) a motion estimation sub-assembly (20) for estimating motion between blocks which belong to consecutive periodical clusters, provided to supply block-wise a motion information to be transmitted and/or stored by replacing those blocks which are cancelled by said temporal sub-sampling;

(c) a recovering sub-assembly with motion compensation (91a, 91b, 92, 93);

said arrangement being characterized in that it also includes:

(d) a fall-back processing sub-assembly provided to add block-wise to said first signal sequence at least a second signal sequence which is in synchronism with the first and is supplied in accordance with a second fall-back mode, substituting the first compensated mode as a function of the result provided by a decision-taking sub-assembly on the basis of a comparison between the original signals and the signals recovered by said recovering sub-assembly with motion compensation based on transmitted and/or stored blocks and on motion information components.

2. An arrangement as claimed in Claim 1, characterized in that the decision-taking sub-assembly includes a change-over switch (80'a) which is controlled by a decision circuit (94, 95, 96, 97, 98, 99, 100, 101, 102, 103) for selecting, in the compensated mode, only the output signals of the temporal sub-sampling sub-assembly (10'a), and in the fall-back mode, also the output signals of the fall-back processing subassembly.

3. An arrangement as claimed in any one of Claims 1 and 2, characterized in

that the fall-back processing sub-assembly includes a delay circuit (50) producing a delay equal to the period of the original signals, followed by a temporal sub-sampling circuit (10''a) operating at the same ratio as the ratio of the temporal sub-sampling sub-assembly.

4. An arrangement as claimed in any one of the Claims 1 to 3, characterized in that the fall-back processing sub-assembly also includes a spatial sub-sampling sub-assembly which comprises, in parallel, a first (30'a, 40a) and a second spatial sub-sampling path (30''a, 60a) in the same ratio as that of the temporal sub-sampling, the spatial sub-sampling matrix of each path being independent of the motion and being fixed but for the temporal resolution of the signals.

5. An arrangement as claimed in Claim 4, characterized in that:

(A) the spatial sub-sampling sub-assembly comprises, in each path, a spatial filtering circuit (30'a, 30''a) followed by a spatial sub-sampling circuit (40a, 60a) operating at a ratio 1/2, and, at the output of the two paths, a switching circuit (70a) provided to select alternately one or the other of the outputs of said spatial sub-sampling circuits at a frequency which is twice lower than that of the original signals;

(B) the decision-taking sub-assembly includes a changeover switch (80''a) controlled to select, in the compensated mode, the output signals of the temporal sub-sampling sub-assembly (10'a) or, in the fall-back mode, the output signals of said switching circuit (70a).

6. An arrangement as claimed in Claim 5, for the case in which said signals are signals which are representative of images, characterized in that the selection in the decision-taking circuit is effected per image blocks and after interpolation error and fall-back error computations compared for selecting the smallest error.

7. An arrangement as claimed in Claim 6, characterized in that the passband-limited information carrier is of the compact disc type.

8. A signal transmission and/or storage system comprising a transmission stage and, after transmission and/or storage of the signals transmitted via a passband-limited information carrier which implies a reduction processing of the quantity of information components to be transmitted and/or stored, a receiving and/or read stage for the transmitted and/or stored signals, characterized in that said transmission stage includes an arrangement as claimed in any one of Claims 1 to 7.

9. An arrangement for processing previously transmitted and/or stored

signals after a reduction of the quantity of information components to be transmitted and/or stored, effected either in accordance with a first compensated mode and with the aid of a temporal sub-sampling sub-assembly provided to supply a first signal sequence, or in accordance with a second fall-back mode and with the aid of a fall-back processing sub-assembly provided to add to said first sequence a second signal sequence synchronous with the first, the choice of said mode being effected with the transmission of a mode information component with the aid of a decision-taking sub-assembly and on the basis of motion information components which are also transmitted and/or stored, and a comparison of information components which are associated with either one or the other mode, respectively, characterized in that it includes:

(a) a motion compensation sub-assembly (201a, 201b, 202, 203) provided to receive the transmitted and/or stored signals corresponding to the output signals of said temporal sub-sampling sub-assembly;

(b) a change-over switch (130) receiving at a first input the output of the motion-compensation sub-assembly and at a second input the transmitted and/or stored signals corresponding to the output signals of said fall-back processing sub-assembly and supplying from its output, in accordance with said mode information corresponding to the selection of the first or the second mode, either the signals present at said first input or the signals present at said second input, respectively;

(c) a change-over switch (250) for alternately selecting, at a frequency which is twice as high as that of the input signals, either said output of this change-over switch (130), or the input of said motion compensation sub-assembly but delayed by a half period of rate of the said input signals of the signal processing arrangement.

10. An arrangement for processing previously transmitted and/or stored signals after a reduction of the quantity of information components to be transmitted and/or stored, effected either in accordance with a first compensated transmission and/or storage mode and with the aid of a temporal sub-sampling sub-assembly in a predetermined ratio provided to supply a first signal sequence, or in accordance with a second fall-back mode and with the aid of a fall-back processing sub-assembly provided to add a second signal sequence to said first sequence and to effect, after spatial sub-sampling of said sequences, the alternate selection of one or the other of these spatially sub-sampled sequences, the choice of said mode being effected with the transmission of a mode information component with the aid of a decision-taking sub-assembly and on

the basis of motion information components which are also transmitted and/or stored, and a comparison of the information components which are associated with either one or the other mode, respectively, with a view to selecting either the output of said motion compensation sub-assembly or the output of said fall-back processing sub-assembly, characterized in that it comprises:

(a) a first sub-sampling and interpolation sub-assembly (211, 212) of the received signals corresponding to the previously transmitted and/or stored signals and constituting the input signals of the arrangement;

(b) a motion-compensation sub-assembly (201a, 201b, 202, 203) whose input is connected, in accordance with said selection of the first or the second mode, respectively, either directly to the input of said arrangement or to this same input but via said first sub-sampling and interpolation sub-assembly;

(c) a second sub-sampling and interpolation sub-assembly (221, 222) whose input is connected, in accordance with said selection of the first or the second mode, respectively, either to the output of said motion compensation sub-assembly, or directly to the input of said arrangement;

(d) a change-over switch (130) which supplies from its output or in accordance with said mode information corresponding to the selection of the first or second mode, respectively, either the output of said motion-compensation sub-assembly or the output of said second sub-sampling and interpolation sub-assembly;

(e) a change-over switch (250) for alternately selecting, at a frequency which is twice as high as the frequency of the input signals, either said output of this change-over switch (130) or the input of said motion compensation sub-assembly but delayed by a half period of the rate of said input signals of the arrangement.

11. An arrangement as claimed in Claim 10, characterized in that the first and second sub-sampling and interpolation sub-assemblies each comprise a spatial sub-sampling circuit (211, 221) and a spatial interpolation circuit (212, 222), and in that the motion compensation sub-assembly comprises image memories (201a, 201b, 202) and an adder (203), with a view to a motion-compensated interpolation on the basis of the output image of the first of these memories, of the input image of the second of these memories, and of the motion information between said input and output images, the delay produced by each of said memories being equal to half the period of the input signals of the processing arrangement.

12. An arrangement as claimed in one of the Claims 10 and 11, characterized in that the selection at the input of the motion compensation sub-assembly and the selection at the input of the second sub-sampling and interpolation sub-assembly are effected with the aid of a first and a second change-over switch (110, 120), respectively, which are controlled in accordance with said mode information.

13. A signal transmission and/or storage system comprising a transmission stage and, after transmission and/or storage of the signals transmitted via a passband-limited information carrier which implies a reduction processing of the quantity of information components to be transmitted and/or stored, a receiving and/or read stage for the transmitted and/or stored signals, characterized in that said receiving and/or read stage includes a signal processing arrangement as claimed in any one of Claims 9 to 12.