

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC WATCHES

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic watches.
 The main object of the invention is to provide improved highly reliable accurate easily manufactured electronic watches, well suited to manufacture by mass production methods, which shall be of small size and low power consumption. These objects are achieved by using frequency dividing circuits of integrated circuit construction the circuitry of which (to be defined later) is such as to enable a high frequency time standard oscillator to be used and a high ratio of frequency division of the oscillations of said oscillator to be obtained (to derive suitable signal for driving the time indicating means of the watch) from an integrated circuit structure involving a minimum number of active semiconductor elements.

Present day normal practice in electronic wrist watches is to use a time standard oscillator followed by a frequency divider of hybrid or bipolar integrated circuit structure. Such dividers are of relatively high cost, large size and high power consumption and therefore great difficulties have been encountered in producing electronic watches of sufficiently small size, low cost and lower power consumption to present a strong popular appeal. The present invention overcomes these difficulties.

According to this invention an electronic watch comprises a time standard oscillator of relatively high frequency; COS/MOS integrated circuits constituting a binary counter chain composed of dual OR-NAND gates and two inverters, for dividing the output frequency of said oscillator; and time-display means driven by the frequency divided output of said chain.

[Price 25p]

Preferably the watch comprises a binary counter composed of three pairs of N channel MOS transistors, three pairs of P channel MOS transistors and two COS/MOS inverters.

The time standard oscillator is preferably a quartz crystal oscillator, and the time display means of the watch is driven by a pulse motor by the frequency divided output of the divider chain and preferably also the input inverter of the binary counter chain is arranged to be "off" when said divider chain is re-set.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:—

Figure 1(a) is a simplified diagram of a COS/MOS inverter,

Figure 1(b) is a graphical tuning diagram of input and output voltages of the inverter of Figure 1(a),

Table 1 is a timing chart of a binary counter;

Figure 2(a) is a simplified diagram of a COS/MOS OR-NAND gate,

Figure 2(b) is a graphical timing diagram of input and output voltages of the inverter of Figure 2(a),

Figure 3(a) is a simplified diagram of a preferred form of binary counter employed in a watch in accordance with this invention,

Figure 3(b) is a graphical timing diagram of waveforms occurring with the counter of Figure 3(a), and

Figure 4 is a block diagram of a preferred form of watch in accordance with this invention.

Figure 1(a) shows a COS/MOS inverter. An input voltage at I turns the P channel MOST "on" and the N channel MOST "off" or vice versa as will be apparent from Figure 1(b). In Figures 1(a) and 1(b) V_{DD} represents voltage from a cell (not shown) and V_{SS} represents ground or zero voltage. Therefore, the inverter takes very little power when in its normal state. A COS/MOS

integrated circuit composed of such inverters similarly requires very little power. In the case of such a circuit used for frequency division, the change of logic is as follows:—

$$5 \quad Q_n = \overline{(\bar{P}_{n-1} + \phi_n) \cdot (\bar{Q}_{n-1} + \bar{\phi}_n)} \dots\dots\dots(1)$$

$$P_n = \overline{(\bar{P}_{n-1} + \phi_n) \cdot (Q_{n-1} + \bar{\phi}_n)} \dots\dots\dots(2)$$

where $\phi_n, \bar{\phi}_n$ refer to clock pulses at the time $t=\pi$ and Q_n, P_n are output logic pulses at $t=\eta$. If P_{n-1} is (a), the change will be as shown in Table 1. As will be apparent the clock frequency ϕ is divided by 2.

Figure 2(a) is an example of an OR-NAND gate composed of COS/MOS transistors referenced 1a, 1b, 2a, 2b, 3a, 3b and 4a, 4b. The signal (Q) at terminal Q is related to the signals A, B, C, and D at terminals A, B, C and D respectively so as substantially to satisfy the equation

$$Q = (A + B) \cdot (C + D).$$

Figure 2(b) is a timing chart of input and output voltages. An OR-NAND gate also consumes little power in its normal state. In

Figure 2(a) the equation $Q = (A + B) \cdot (C + D)$ applies.

Figure 3(a) shows a preferred form of binary counter for a watch in accordance with the invention. I_1 and I_3 are inverters. As will be seen, the counter is composed of OR-

NAND gates, with $\phi, \bar{\phi}$ the input terminals,

and $Q, \bar{Q}$ the output terminals. These output terminals provide signals which are used as clock signals to drive the next counter stage (not shown). Figure 3(b) is a timing chart of voltage in the binary counter which is composed of a minimum number of MOSTs. For a quartz crystal wrist watch in which the attainment of minimum size and minimum power consumption are of paramount importance, the use of a counter as shown in Figure 3 is of great practical advantage.

Figure 4 is a block diagram of a quartz crystal wrist watch in accordance with this invention and having a chain of binary counters $F_1 \dots F_m \dots F_n$ as illustrated by Figure 3. Referring to Figure 4, 1 represents the time standard quartz crystal oscillator of the watch. It operates at a high frequency of the order of several kc/s up to several tens of kc/s. The clock signal for the 1st binary counter stage F_1 derived from the output of the oscillator 1 by means of a NAND gate I_1 and inverter I_2 . When the binary counter

chain is reset, NAND gate I_1 turns "off" to reduce power consumption. An inverter I_3 is used to re-set a predetermined number of the later stages of the binary counter chain when the switch SW is closed. Block 2 represents a pulse motor and associated gearing driving the hands or other time indicating means of the watch.

Because of the use of a COS/MOS binary counter consisting of a minimum number of MOSTs, and because of the small size in which such a counter can be made, as well as its low power consumption, it is possible to use a time standard oscillator of high frequency, followed by a divider chain of high division ratio and therefore to obtain a reliable accurate wrist watch of remarkably small size.

WHAT WE CLAIM IS:—

1. An electronic watch comprising a time standard oscillator of relatively high frequency; COS/MOS integrated circuits constituting a binary counter chain composed of dual OR-NAND gates and two inverters, for dividing the output frequency of said oscillator; and time display means driven by the frequency divided output of said chain.

2. A watch as claimed in claim 1 and comprising a binary counter composed of three pairs of N channel MOS transistors, three pairs of P channel MOS transistors and two COS/MOS inverters.

3. A watch as claimed in claim 1 and comprising an OR-NAND gate composed of a pair of 1st P channel MOS transistors (1a, 1b) with their sources connected to a positive supply terminal of a cell; a pair of 2nd P channel MOS transistors (2a, 2b) with their sources connected separately to the drains of said 1st P channel MOS transistors and their drains connected to one another, a pair of 3rd N channel MOS transistors (3a, 3b) with their drains connected to the drains of the said 2nd P channel transistors and their sources connected to one another, and a pair of 4th N channel MOS transistors (4a, 4b) with their drains connected to the sources of the said 3rd N channel transistors and their sources grounded, the input terminals of said OR-NAND gate being connected in common with those of the pair (2a, 3b) the pair (1a, 3a), the pair (1b, 4b) and the pair (2b, 4a), the output terminal being constituted by the drains of the pairs (3a, 3b, 2a, 2b) connected in common.

4. An electronic watch comprising binary counters composed of dual OR-NAND gates as set forth in claim 3, wherein a pair (1a, 1b) of the 1st P channel MOS transistors are used in common and a pair (4a, 4b) of the 4th N channel MOS transistor are also used in common, the input terminals being consti-

integrated circuit composed of such inverters similarly requires very little power. In the case of such a circuit used for frequency division, the change of logic is as follows:—

$$5 \quad Q_n = \overline{(\bar{P}_{n-1} + \phi_n) \cdot (\bar{Q}_{n-1} + \bar{\phi}_n)} \text{-----}(1)$$

$$P_n = \overline{(\bar{P}_{n-1} + \phi_n) \cdot (Q_{n-1} + \bar{\phi}_n)} \text{-----}(2)$$

where $\phi_n, \bar{\phi}_n$ refer to clock pulses at the time $t=\pi$ and Q_n, P_n are output logic pulses at $t=\eta$. If P_{n-1} is (a), the change will be as shown in Table 1. As will be apparent the clock frequency ϕ is divided by 2.

Figure 2(a) is an example of an OR-NAND gate composed of COS/MOS transistors referenced 1a, 1b, 2a, 2b, 3a, 3b and 4a, 4b. The signal (Q) at terminal Q is related to the signals A, B, C, and D at terminals A, B, C and D respectively so as substantially to satisfy the equation

$$Q = (A+B) \cdot (C+D).$$

Figure 2(b) is a timing chart of input and output voltages. An OR-NAND gate also consumes little power in its normal state. In

Figure 2(a) the equation $Q = (A+B) \cdot (C+D)$ applies.

Figure 3(a) shows a preferred form of binary counter for a watch in accordance with the invention. I_1 and I_2 are inverters. As will be seen, the counter is composed of OR-

NAND gates, with $\phi, \bar{\phi}$ the input terminals,

and $Q, \bar{Q}$ the output terminals. These output terminals provide signals which are used as clock signals to drive the next counter stage (not shown). Figure 3(b) is a timing chart of voltage in the binary counter which is composed of a minimum number of MOSTs. For a quartz crystal wrist watch in which the attainment of minimum size and minimum power consumption are of paramount importance, the use of a counter as shown in Figure 3 is of great practical advantage.

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chain is reset, NAND gate I_1 turns "off" to reduce power consumption. An inverter I_3 is used to re-set a predetermined number of the later stages of the binary counter chain when the switch SW is closed. Block 2 represents a pulse motor and associated gearing driving the hands or other time indicating means of the watch.

Because of the use of a COS/MOS binary counter consisting of a minimum number of MOSTs, and because of the small size in which such a counter can be made, as well as its low power consumption, it is possible to use a time standard oscillator of high frequency, followed by a divider chain of high division ratio and therefore to obtain a reliable accurate wrist watch of remarkably small size.

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2. A watch as claimed in claim 1 and comprising a binary counter composed of three pairs of N channel MOS transistors, three pairs of P channel MOS transistors and two COS/MOS inverters.

3. A watch as claimed in claim 1 and comprising an OR-NAND gate composed of a pair of 1st P channel MOS transistors (1a, 1b) with their sources connected to a positive supply terminal of a cell; a pair of 2nd P channel MOS transistors (2a, 2b) with their sources connected separately to the drains of said 1st P channel MOS transistors and their drains connected to one another, a pair of 3rd N channel MOS transistors (3a, 3b) with their drains connected to the drains of the said 2nd P channel transistors and their sources connected to one another, and a pair of 4th N channel MOS transistors (4a, 4b) with their drains connected to the sources of the said 3rd N channel transistors and their sources grounded, the input terminals of said OR-NAND gate being connected in common with those of the pair (2a, 3b) the pair (1a, 3a), the pair (1b, 4b) and the pair (2b, 4a), the output terminal being constituted by the drains of the pairs (3a, 3b, 2a, 2b) connected in common.

4. An electronic watch comprising binary counters composed of dual OR-NAND gates as set forth in claim 3, wherein a pair (1a, 1b) of the 1st P channel MOS transistors are used in common and a pair (4a, 4b) of the 4th N channel MOS transistor are also used in common, the input terminals being consti-



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5 uted by the input terminals of the pair (1a, 2a) connected in common and the input terminals of the pair (2b, 4a) connected in common, the output terminal of one OR-NAND gate being connected to both input terminals of the pair (1b, 4b) through an inverter, and the input terminal of the pair (2a, 3b) of one OR-NAND gate being connected to the output terminal of the other OR-NAND gate and further connected to the input terminals of the pair (2a, 3b) of the other OR-NAND gate through an inverter.

10 5. An electronic watch as claimed in any of the preceding claims wherein the time standard oscillator is a quartz crystal oscillator, and the time display means of the watch

is driven by a pulse motor driven by the frequency divided output of the divider chain.

6. An electronic watch as claimed in any of the preceding claims wherein the input inverter of the binary counter chain is arranged to be "off" when said divider chain is reset. 20

7. Electronic watch substantially as herein described with reference to the accompanying drawings. 25

J. MILLER & CO.,
Agents for the Applicants,
Chartered Patent Agents,
262 High Holborn,
London, W.C.1.

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