What Is Claimed Is:

1. A semiconductor device, comprising:

a substrate having first and second regions;

gate electrodes spaced apart from each other and stacked in a first direction perpendicular to an upper surface of the substrate on the first region, extending in a second direction perpendicular to the first direction by different lengths on the second region, and including at least one ground select gate electrode, memory cell gate electrodes, and at least one string select gate electrode stacked in order from the substrate;

first separation regions penetrating through the gate electrodes and extending in the second direction in the first and second regions, and spaced apart from each other in a third direction perpendicular to the first and second directions;

second separation regions penetrating through the gate electrodes and extending in the second direction between the first separation regions, and spaced apart from each other in the second direction on the second region;

a lower separation region penetrating through the at least one ground select gate electrode between the second separation regions and separating the at least one ground select gate electrode along with the second separation regions;

a substrate insulating layer disposed in the substrate between the first separation regions and the second separation regions in the second region;

channel structures penetrating through the gate electrodes and extending perpendicularly to the substrate in the first region; and

a first dummy channel structure penetrating through the gate electrodes and the substrate insulating layer and extending perpendicularly to the substrate on an external side of the lower separation region in the third direction,

wherein the substrate insulating layer is disposed between the lower separation region and the first separation regions and between the second separation regions and the first separation regions not to overlap the lower separation region on a plane.

2. The semiconductor device of claim 1, wherein the first dummy channel structure has a first width in the second direction and has a second width greater than the first width in the third direction.

3. The semiconductor device of claim 2, wherein each of the channel structures has a first maximum width, and the first maximum width is less than the second width of the first dummy channel structure.

4. The semiconductor device of claim 3, wherein the first maximum width is within a range of 50 nm to 150 nm approximately, and the second width is within a range of 120 nm to 220 nm approximately.

5. The semiconductor device of any one of claims 1 to 4, further comprising:

second dummy channel structures penetrating through the gate electrodes and the substrate insulating layer and forming columns and rows in the second region,

wherein the first dummy channel structure is disposed between the second dummy channel structures adjacent to each other in the second direction.

6. The semiconductor device of claim 5, wherein each of the second dummy channel structures has a size and a shape different from a size and a shape of the first dummy channel structure.

7. The semiconductor device of claim 5 or claim 6, wherein the first dummy channel structure is surrounded by four second dummy channel structures.

8. The semiconductor device of any one of claims 5 to 7, wherein the second dummy channel structures are disposed along ends of the gate electrodes.

9. The semiconductor device of claim 1, further comprising:

third separation regions penetrating through the gate electrodes and extending in the second direction between the first separation regions and the second separation regions, and spaced apart from each other in the second direction with spacing regions therebetween in the second region.

10. The semiconductor device of claim 9,

wherein the substrate insulating layer is disposed on the substrate in a lower portion of a first spacing region of the spacing regions most adjacent to the first region, and

wherein the semiconductor device further includes a third dummy channel structure penetrating through the gate electrodes and the substrate insulating layer and extending perpendicularly to the substrate in the first spacing region.

11. The semiconductor device of claim 10, wherein the third dummy channel structure has a maximum diameter less than a maximum diameter of the first dummy channel structure.

12. The semiconductor device of claim 10 or claim 11, wherein the substrate insulating layer is spaced apart from spacing regions other than the first spacing region to not overlap the spacing regions.

13. The semiconductor device of claim 1,

wherein the gate electrodes provide pad regions as the gate electrodes in a lower region extend further than the gate electrode in an upper region in the second region, and

wherein the semiconductor device further includes contact plugs connected to the gate electrodes in the pad regions.

14. The semiconductor device of claim 13, wherein the first dummy channel structure is disposed on a first side of the lower separation region in the third direction, and one of the contact plugs is disposed on a second side of the lower separation region in the third direction.

15. A semiconductor device, comprising:

a substrate having a conductive region and an insulating region;

gate electrodes including at least one ground select gate electrode and memory cell gate electrodes, wherein the memory cell gate electrodes include sub-gate electrodes spaced apart from each other and stacked in a first direction perpendicular to an upper surface of the substrate and extending in a second direction perpendicular to the first direction and gate connectors connecting the sub-gate electrodes disposed on the same level;

channel structures penetrating through the gate electrodes and extending in the conductive region of the substrate;

a first dummy channel structure penetrating through the gate electrodes and extending in the insulating region of the substrate and disposed adjacent to at least one side of the gate connectors in a third direction perpendicular to the first and second directions;

first separation regions penetrating through the gate electrodes and extending in the second direction in the conductive region and the insulating region, and spaced apart from each other in the third direction;

second separation regions penetrating through the gate electrodes and extending in the second direction between the first separation regions, and spaced apart from each other in the second direction on the insulating region;

a lower separation region penetrating through the at least one ground select gate electrode between the second separation regions and separating the at least one ground select gate electrode along with the second separation regions; and

a substrate insulating layer disposed in the substrate between the first separation regions and the second separation regions in the insulating region,

wherein the substrate insulating layer is disposed between the lower separation region and the first separation regions and between the second separation regions and the first separation regions not to overlap the lower separation region on a plane.

16. The semiconductor device of claim 16, wherein each of the channel structures has a first height in the first direction, and the first dummy channel structure has a second height, and

a lower end of the first dummy channel structure is disposed on a level lower than lower ends of the channel structures, such that the second height is greater than the first height.

17. A semiconductor device, comprising:

a substrate having first and second regions;

gate electrodes spaced apart from each other and stacked in a first direction perpendicular to an upper surface of the substrate in the first region, and extending in a second direction perpendicular to the first direction by different lengths and providing pad regions in the second region;

penetration separation regions including first separation regions penetrating through the gate electrodes and extending in the second direction in the first and second regions, and spaced apart from each other in a third direction perpendicular to the first and second directions; and second separation regions penetrating through the gate electrodes and extending in the second direction between the first separation regions, and spaced apart from each other in the second direction on the second region;

a lower separation region penetrating through at least one gate electrode including a lowermost gate electrode between the second separation regions;

a substrate insulating layer disposed in a portion of the substrate between the first separation regions and the second separation regions in the second region;

channel structures penetrating through the gate electrodes and extending

perpendicularly to the substrate in the first region; and

dummy channel structures penetrating through the gate electrodes and at least portions of the substrate insulating layer and extending perpendicularly to the substrate in the second region, and including a first dummy channel structure disposed adjacent to the lower separation region around the lower separation region and second dummy channel structures disposed in a regular pattern in the pad regions of the gate electrodes,

wherein the substrate insulating layer is disposed between the lower separation region and the first separation regions and between the second separation regions and the first separation regions not to overlap the lower separation region on a plane.

18. The semiconductor device of claim 17, wherein the first dummy channel structure is disposed on each of both sides of the lower separation region in the third direction.

19. The semiconductor device of claim 17 or claim 18,

wherein each of the channel structures and the dummy channel structures include an epitaxial layer disposed in lower portions thereof, and

wherein the epitaxial layer of the channel structures has a first thickness, and the epitaxial layer of the dummy channel structures has a second thickness less than the first thickness.