Abstract

A low elasticity layer (20) having an opening in an electrode arranging area where element electrodes are disposed is provided on a main surface of a semiconductor substrate (10). On the low elasticity layer (20), lands (32) serving as external electrodes are disposed, and pads (30) on the element electrodes, the lands (32) and metal wires (31) for connecting them are integrally formed as a metal wiring pattern (33). A solder resist film (50) having an opening for exposing a part of each land (32) is formed, and a metal ball (40) is provided on the land (32) in the opening. The low elasticity layer (20) absorbs thermal stress and the like caused in heating or cooling the semiconductor device, so as to prevent disconnection of the metal wires (31).