

WHAT IS CLAIMED IS:

1. A multi-chip package comprising:

a printed circuit board; and

a plurality of memory chips stacked on the printed circuit board and including a master memory chip and a plurality of slave memory chips, each of the plurality of memory chips including an impedance control (ZQ) pad and a plurality of data input/output (DQ) pads,

wherein the multi-chip package is configured to receive a ZQ calibration command once from an external of the multi-chip package,

wherein the master memory chip is configured to receive the ZQ calibration command and to perform a first ZQ calibration operation with respect to a ZQ pad of the master memory chip by using a ZQ resistor connected to a ZQ terminal of the multi-chip package and control termination resistance values of the DQ pads of the master memory chip on the basis of a result of the first ZQ calibration operation, and

based on the ZQ calibration command received by the master memory chip, each slave memory chip from among the plurality of slave memory chips is configured to perform second ZQ calibration operations with respect to DQ pads of first to m^{th} slave memory chips from among the plurality of slave memory chips by using termination resistance values of first to m^{th} DQ pads from among the plurality of DQ pads of the master memory chip on the basis of a ZQ calibration option set between the first to m^{th} DQ pads of the master memory chip and DQ pads of the first to m^{th} slave memory chips, m being an integer greater than 1, and the ZQ calibration option being a one-to-one correspondence for performing the second ZQ calibration operations between the first to m^{th} DQ pads of the master memory chip and the DQ pads of the first to m^{th} slave memory chips.

2. The multi-chip package of claim 1, wherein
the plurality of slave memory chips are configured to perform the second ZQ calibration operations simultaneously.
3. The multi-chip package of claim 2, wherein
wherein the plurality of slave memory chips are configured such that a time for completing the second ZQ calibration operations performed by the plurality of slave memory chips is shorter than two times a time for completing the second ZQ calibration operation performed by one slave memory chip.
4. The multi-chip package of any one of the previous claims , wherein
the ZQ pad of each slave memory chip from among the plurality of slave memory chips is connected to a source voltage line or a ground voltage line.
5. The multi-chip package of any one of the previous claims, wherein
the first to mth DQ pads of the master memory chip are respectively connected to first to mth DQ pads of each of the first to mth slave memory chips.
6. The multi-chip package of any one of the previous claims, wherein
the ZQ calibration option is stored in a register of the master memory chip.
7. The multi-chip package of any one of claims 1 to 5, wherein
the ZQ calibration option is stored in a register of each of the plurality of memory chips.

8. The multi-chip package of any one of claims 1 to 5, wherein each of the plurality of memory chips includes a ZQ engine connected to the ZQ pad, and

the ZQ engine included in each of the plurality of memory chips comprises:

a master/slave determiner circuit configured to detect a voltage level of the ZQ pad and compare the detected voltage level of the ZQ pad with a source voltage level or a ground voltage level to determine whether a corresponding memory chip is the master memory chip or one of the plurality of slave memory chips;

a first comparator configured to compare the voltage level of the ZQ pad with a reference voltage level in response to the master/slave determiner circuit determining that the corresponding memory chip is the master memory chip;

a second comparator;

a multiplexer configured to provide, as a first input, an output of the first comparator in the master memory chip and provide, as a second input, an output of a third comparator of each of DQ drivers connected to the DQ pads in the plurality of slave memory chips;

first pull-up circuitry configured to perform a pull-up calibration operation that includes generating a pull-up calibration code on the basis of an output of the multiplexer;

second pull-up circuitry of which an impedance is controllable to be equal to an impedance of the first pull-up circuitry on the basis of the pull-up calibration code,

the second comparator being configured to compare the reference voltage level with a voltage level of a connection node between the second pull-up circuitry and first pull-down circuitry; and

the first pull-down circuitry configured to perform a pull-down calibration

operation of generating a pull-down calibration code on the basis of an output of the second comparator.

9. The multi-chip package of claim 8, wherein
the ZQ calibration option is stored in the master/slave determiner circuit.

10. The multi-chip package of claim 8, wherein each of the DQ drivers
comprises:

third pull-up circuitry configured to control a pull-up termination resistance
of each of the DQ pads based on the pull-up calibration code;

second pull-down circuitry configured to control a pull-down termination
resistance based on the pull-down calibration code; and

the third comparator configured to compare a voltage level of each of the DQ
pads with the reference voltage level.

11. The multi-chip package of any one of the previous claims, wherein,
the plurality of memory chips of the multi-chip package includes 2^n memory
chips, and the plurality of memory chips are configured to perform the ZQ calibration
operation on m DQ pads,

wherein n is an integer greater than 1 and m is an integer less than or equal
to $2^n - 1$, wherein $m \leq 2^n - 1$.

12. The multi-chip package of any one of claims 1 to 10, wherein,
when the plurality of memory chips including m DQ pads are stacked in the
multi-chip package, the number of stacked memory chips is equal to n , wherein n is
an integer greater than 1 and less than or equal to $m + 1$, wherein $n \leq m + 1$, and where

m is an integer greater than 1.

13. The multi-chip package of any one of claims 1 to 10, wherein,
when n memory chips including m DQ pads are stacked in the multi-chip package, the ZQ calibration operation is performed "i" times in the multi-chip package, where m is an integer greater than 1, wherein $n > m + 1$, and wherein $i = [(n - 1) / m] + 1$.

14. The multi-chip package of any one of the previous claims, wherein
each of the plurality of memory chips comprises one of a NAND non-volatile memory device, a VNAND non-volatile memory device, and a non-volatile memory device having a cell over peri (COP) structure.