SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims priority to Korean Patent Application No. 10-2022-0031415, filed on 14 March 2022, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The inventive concepts relate to semiconductor devices and/or methods of fabricating the same, and more particularly, to semiconductor devices including buried gate lines and/or methods of fabricating the same.

BACKGROUND

[0003] Due to characteristics such as miniaturization, multifunctionality, and low manufacturing cost, a semiconductor device is in the spotlight as an important element in an electronics industry. The semiconductor devices may be classified into a semiconductor memory device for storing logic data, a semiconductor logic device for processing logic data, and a hybrid semiconductor device including a memory element and a logic element.

[0004] Recently, in accordance with high speed and low power consumption of an electronic device, a semiconductor device embedded therein is also required to have high operating speed and low operating voltage. To satisfy these required characteristics, the semiconductor device becomes more highly integrated. As the semiconductor device is highly integrated, reliability of the semiconductor device may deteriorate. However, as the electronic industry is highly developed, the demand for high reliability of the semiconductor

device is increasing. Accordingly, many studies are being conducted to improve the reliability of the semiconductor device.

SUMMARY

[0005] Some example embodiments of the inventive concepts provide a semiconductor device having improved electrical characteristics and a method for manufacturing the same.

[0006] According to some example embodiments of the present inventive concepts, a method of fabricating a semiconductor device may include forming a device isolation layer defining active regions on a substrate, and forming gate lines intersecting the active regions and buried in the substrate, the forming of the gate lines may include forming a trench intersecting the active regions in the substrate, forming a conductive layer filling the trench, and performing a heat treatment process on the conductive layer, the conductive layer may include a nitride of a first metal, and nitrogen atoms in the conductive layer may be diffused toward an outer surface and a lower surface of the conductive layer by the heat treatment process.

[0007] According to some example embodiments of the present inventive concepts, a method of fabricating a semiconductor device may include forming a device isolation layer defining active regions on a substrate, forming trenches intersecting the active regions, forming a conductive layer filling a lower portion of each of the trenches, the conductive layer including a nitride of a first metal, forming a first interface layer adjacent to an outer surface and a lower surface of the conductive layer, the first interface layer including a nitride of the first metal, and forming a capping layer filling an upper portion of each of the trenches, a nitrogen concentration in the first interface layer may be higher than a nitrogen concentration in the conductive layer.

[0008] According to some example embodiments of the present inventive concepts, a semiconductor device may include a device isolation layer defining active regions of a substrate, and gate lines intersecting the active regions and buried in a trench of the substrate, each of the gate lines may include an interface layer covering sidewalls and a bottom surface of the trench, a conductive layer filling a remainder of the trench on the interface layer, and a capping layer filling an upper portion of the trench on the interface layer and the conductive layer, each of the conductive layer and the interface layer may include a nitride of a first metal, and a nitrogen concentration in the interface layer may be higher than a nitrogen concentration in the conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The drawings described herein are for illustrative purposes only of selected embodiments and not all possible implementations, and are not intended to limit the scope of the present disclosure.

[0010] FIG. 1 is a cross-sectional view for explaining a semiconductor device according to some example embodiments of the present inventive concepts.

[0011] FIGS. 2A and 2B are cross-sections for explaining a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along lines I-I' and II-II' of FIG. 1, respectively.

[0012] FIGS. 3A and 3B are cross-sections for explaining a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along lines I-I' and II-II' of FIG. 1, respectively.

[0013] FIG. 4 is a cross-sectional view for explaining a semiconductor device according to some example embodiments of the present inventive concepts.

[0014] FIGS. 5A to 10A are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line I-I' of FIG. 1.

[0015] FIGS. 5B to 10B are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line II-II' of FIG. 1.

[0016] FIG. 8C is an enlarged view of area "A" of FIG. 8A.

[0017] FIGS. 11A to 13A are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line I-I' of FIG. 1.

[0018] FIGS. 11B to 13B are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line II-II' of FIG. 1.

DETAILED DESCRIPTION

[0019] A semiconductor device according to the inventive concepts will be described with reference to the drawings.

[0020] FIG. 1 is a cross-sectional view for explaining a semiconductor device according to some example embodiment of the present inventive concepts. FIGS. 2A and 2B are cross-sections for explaining a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along lines I-I' and II-II' of FIG. 1, respectively.

[0021] Referring to FIGS. 1, 2A, and 2B, a substrate 100 may be provided. The substrate 100 may include a semiconductor substrate. For example, the semiconductor substrate

may be a silicon (Si) substrate, a germanium (Ge) substrate, or a silicon-germanium (Si-Ge) substrate.

[0022] A first direction "X" and a second direction "Y" may be parallel to an upper surface of the substrate 100 and perpendicular to each other. A third direction "S" may be a direction parallel to the upper surface of the substrate 100 and intersecting both the first direction "X" and the second direction "Y". A fourth direction "Z" may be a direction perpendicular to all of the first to third directions "X", "Y", and "S". The cross section of FIG. 2A shows a "Z"-"S" section, and the section of FIG. 2B shows a "Z"-"Y" section.

[0023] A device isolation layer 110 may be disposed on the substrate 100 to define active regions 105. The active regions 105 may have a bar shape when viewed in a plan view. Here, the active regions 105 may have long axes in the third direction "S", respectively.

[0024] A plurality of gate lines 200 may be disposed in the substrate 100 to intersect the active regions 105 when viewed in a plan view. The gate lines 200 may be word lines. The gate lines 200 may extend in the second direction "Y" and may be disposed in parallel with one another in the first direction "X". The gate lines 200 may be buried gate lines buried in the substrate 100. The gate lines 200 may be disposed in trenches 120 of the substrate 100 extending to cross the active regions 105. Each of the gate lines 200 may partially fill each of the trenches 120. Here, an upper surface of each of the gate lines 200 may be located at a level lower than an upper surface of the substrate 100. Each of the gate lines 200 may include a conductive layer 222 and an interface layer 224. The conductive layer 222 and the interface layer 224 may constitute a conductive part 220 of each of the gate lines 200. Hereinafter, the configuration of the gate lines 200 will be described with respect to one gate line 200.

[0025] The conductive layer 222 may be disposed in the trench 120 of the substrate 100. The conductive layer 222 may partially fill the trench 120. The conductive layer 222 may

include a low-resistance (low-R) material. The conductive layer 222 may include a nitride of a first metal having conductivity. For example, the first metal may include molybdenum (Mo). The conductive layer 222 may lower a resistance of the gate lines 200.

[0026] The interface layer 224 may conformally cover the trench 120 of the substrate 100. The interface layer 224 may cover sidewalls and a bottom surface of the trench 120. The interface layer 224 may be interposed between the sidewalls and bottom surfaces of the trench 120 and the conductive layer 222. That is, the interface layer 224 may separate the conductive layer 222 from the sidewalls and bottom surfaces of the trench 120, and the conductive layer 222 in the trench 120 may fill the inside of the interface layer 224. Depending on a shape of the trench 120 and a shape of the conductive layer 222, a cross-section of the interface layer 224 may have a U-shape. For example, the interface layer 224 may conformally cover a lower surface and an outer surface of the conductive layer 222. The interface layer 224 may be in contact with the lower surface and the outer surface of the conductive layer 222. The uppermost end of the interface layer 224 and the uppermost end of the conductive layer 222 may be formed at the same level. That is, an upper surface 224a of the interface layer 224 may be coplanar with an upper surface 222a of the conductive layer 222. The upper surface 224a of the interface layer 224 and the upper surface 222a of the conductive layer 222 may be formed at a level lower than the upper surface of the substrate 100. Although not shown, the upper surface 222a of the conductive layer 222 may be provided at a higher level than the upper surface 224a of the interface layer 224. That is, an upper portion of the conductive layer 222 may protrude onto the upper surface 224a of the interface layer 224. A thickness of the interface layer 224 may be 5Å to 30Å. However, the inventive concepts are not limited thereto, and the interface layer 224 may be provided to have a thickness of 30Å or more if necessary.

[0027] The interface layer 224 may be a liner layer provided for lowering a flat band voltage of the gate lines 200. In the present specification, the flat band voltage refers to a gate voltage that causes an electric filed to become zero as an energy band becomes flat regardless of a position on a surface of a material layer. For example, a flat band voltage at a surface of the interface layer 224 may be lower than a flat band voltage at a surface of the conductive layer 222. In detail, when nitrogen (N) is injected into the molybdenum (Mo) material layer, a flat band voltage of a material layer may be lowered. That is, the interface layer 224 may be provided on the surface of the conductive layer 222, and thus the flat band voltage of the gate lines 200 may be lowered.

[0028] The interface layer 224 may include the same material as the conductive layer 222. In the present specification, the two layers including the same material may mean that the two layers consist of the same elements as each other and a composition ratio of the elements of the two layers is the same as or different from each other. The interface layer 224 may include the conductive nitride of the first metal. The first metal may include molybdenum (Mo). Here, a composition ratio of the interface layer 224 may be different from a composition ratio of the conductive layer 222. For example, a concentration of nitrogen (N) in the interface layer 224 may be greater than a concentration of nitrogen (N) in the conductive layer 222. For example, a concentration of molybdenum (Mo) in the interface layer 224 may be less than a concentration of molybdenum (Mo) in the conductive layer 222. In other words, in the conductive part 220 formed of the nitride of the first metal, the interface layer 224 may be a nitrogen-rich region, and the conductive layer 222 may be a molybdenum-rich region.

[0029] The concentration of nitrogen (N) in the interface layer 224 may decrease toward the conductive layer 222. However, the inventive concepts are not limited thereto, and the concentration of nitrogen (N) in the interface layer 224 may be substantially uniform.

[0030] The interface layer 224 and the conductive layer 222 may include the same material and may have different composition ratio from each other. Accordingly, an interfacial resistance between the interface layer 224 and the conductive layer 222 may be small. For example, there may be less lattice mismatch, which is a factor increasing the interfacial resistance, at an interface between the interface layer 224 and the conductive layer 222.

[0031] In addition, the interface layer 224 may lower the flat band voltage of each of the gate lines 200, which may mean that a work function of each of the gate lines 200 is low. For example, the flat band voltage may correspond to a difference between the work function of each of the gate lines 200 and a work function of the substrate 100. That is, the work function of each of the gate lines 200 may be reduced by the interface layer 224, and a threshold voltage of the semiconductor device may be lowered.

[0032] Furthermore, the interface layer 224 may be provided on the sidewalls of the gate lines 200, from a top of each of the gate lines 200 to first and second impurity implantation regions SD1 and SD2 to be described later. A gate induced drain leakage current (GIDL current) may be reduced.

[0033] According to some embodiments of the inventive concepts, the threshold voltage of the semiconductor device may be low while the interfacial resistance between the constituent layers 222 and 224 in each of the gate lines 200 is small. Accordingly, electrical characteristics of the semiconductor device may be improved.

[0034] Referring to FIGS. 1, 2A, and 2B, gate insulating patterns 210 may be interposed between the gate lines 200 and the active regions 105, respectively, and may be interposed between the gate lines 200 and the device isolation layer 110. The gate insulating patterns 210 may cover the sidewalls and bottom surfaces of the trenches 120. That is, the gate insulating patterns 210 may separate the gate lines 200 from the substrate 100. The gate

insulating patterns 210 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0035] First capping patterns 230 may be disposed on the gate lines 200, respectively. The first capping patterns 230 may be in contact with the upper surface 222a of the conductive layer 222 and the upper surface 224a of the interface layer 224. Upper surfaces of the first capping patterns 230 may be coplanar with the upper surface of the substrate 100. The gate insulating patterns 210 may extend between the first capping patterns 230 and the active regions 105 or between the first capping patterns 230 and the device isolation layer 110, respectively. Here, the gate insulating patterns 210 interposed between the first capping patterns 230 and the active regions 105 may act as a buffer which relieves stress between the active regions 105 and the first capping patterns 230. Contrary to that shown in FIG. 2A, lower surfaces of the first capping patterns 230 may be in contact with the upper surfaces of the gate insulating patterns 210 and both side surfaces of the first capping patterns 230 may be in contact with the active regions 105 or the device isolation layer 110. The first capping patterns 230 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0036] The first impurity implantation region SD1 and the second impurity implantation region SD2 may be respectively disposed in the active regions 105 adjacent to both sides of each of the gate lines 200. The first impurity implantation region SD1 and the second impurity implantation region SD2 may extend inward from the surface of the substrate 100. A conductivity type of the first and second impurity implantation regions SD1 and SD2 may be different from a conductivity type of the substrate 100. For example, when the substrate 100 is P-type, the first and second impurity implanted regions SD1 and SD2 may be N-type. The first and second impurity implantation regions SD1 and SD2 may correspond to a source region or a drain region, respectively.

[0037] Subsequently, first pads 310 connected to the first impurity implantation region SD1 may be disposed on the substrate 100, and second pads 320 connected to the second impurity implantation region SD2 may be disposed on the substrate 100. The first pads 310 and the second pads 320 may include a conductive material such as polysilicon doped with impurities or metal.

[0038] A first interlayer insulating layer 400 may be disposed on the first and second pads 310 and 320. The first interlayer insulating layer 400 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0039] Bit lines 510 may be disposed on the first interlayer insulating layer 400. The bit lines 510 may be provided in a second interlayer insulating layer 550 on the first interlayer insulating layer 400. The second interlayer insulating layer 550 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON). The bit lines 510 may pass through the first interlayer insulating layer 400 to be connected to direct contacts 520 connected to the first pads 310, respectively. The bit lines 510 and the direct contacts 520 may include any one of a doped semiconductor material, a conductive metal nitride, a metal, and a metal-semiconductor compound. For example, the doped semiconductor material may include doped silicon (doped-Si) or doped germanium (doped-Ge). For example, the conductive metal nitride may include titanium nitride (TiN) or tantalum nitride (TaN). For example, the metal may include tungsten (W), titanium (Ti), or tantalum (Ta). For example, the metal-semiconductor compound may include tungsten silicide (WSi_2), cobalt silicide (CoSi), or titanium silicide (TiSi).

[0040] Second capping patterns 530 may be disposed on the bit lines 510, respectively, and both sidewalls of each of the bit lines 510 may be covered with insulating spacers 540. The second capping patterns 530 and the insulating spacers 540 may include any one of silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0041] Buried contacts 610 passing through the first and second interlayer insulating layers 400 and 550 and connected to the second pads 320, respectively, may be disposed on the substrate 100. The buried contacts 610 may include a conductive material such as doped silicon or metal.

[0042] A data storage element connected to the buried contacts 610 may be disposed on the second interlayer insulating layer 550. For example, the data storage element may be a capacitor CA. The capacitor CA may include first electrodes 620, a second electrode 640, and a dielectric layer 630 interposed between the first electrodes 620 and the second electrode 640. Each of the first electrodes 620 may have a cylindrical shape with a closed bottom. The second electrode 640 may be a common electrode that commonly covers the first electrodes 620. The first electrodes 620 and the second electrode 640 may include silicon doped with impurities, a metal, or a metal compound.

[0043] A support layer 700 may be disposed between the second electrode 640 and the second interlayer insulating layer 550. The support layer 700 may be disposed on an outer wall of the first electrode 620 to prevent the first electrode 620 from collapsing. The support layer 700 may include an insulating material. The dielectric layer 630 may extend in one direction and may be interposed between the support layer 700 and the second electrode 640.

[0044] FIGS. 3A and 3B are cross-sections for explaining a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along lines I-I' and II-II' of FIG. 1, respectively. In the following embodiments, components described in the embodiments of FIGS. 1, 2A, and 2B use the same reference numerals, and descriptions thereof are omitted or briefly described for convenience of description. That is, differences between the embodiments of FIGS. 1, 2A, and 2B and the following embodiments will be mainly described.

[0045] Referring to FIGS. 1, 3A, and 3B, a plurality of gate lines 200 may be disposed in a substrate 100 to intersect active regions 105 when viewed in a plan view. The gate lines 200 may be buried gate lines buried in the substrate 100. The gate lines 200 may be disposed in trenches 120 of the substrate 100 extending to cross the active regions 105, respectively. The gate lines 200 may include a conductive layer 222 and interface layers 224 and 226. The conductive layer 222 and the interface layers 224 and 226 may constitute the conductive part 220 of each of the gate lines 200. Hereinafter, the configuration of the gate lines 200 will be described with respect to one gate line 200.

[0046] The conductive layer 222 may be disposed in the trench 120 of the substrate 100. The conductive layer 222 may partially fill the trench 120. The conductive layer 222 may include a nitride of a first metal having conductivity. For example, the first metal may include molybdenum (Mo).

[0047] The interface layers 224 and 226 may include a first interface layer 224 and a second interface layer 226.

[0048] The first interface layer 224 may be substantially the same as or similar to the interface layer 224 described with reference to FIGS. 1, 2A, and 2B. The first interface layer 224 may conformally cover the trench 120 of the substrate 100. The first interface layer 224 may cover sidewalls and a bottom surface of the trench 120. The first interface layer 224 may be interposed between the sidewalls and bottom surfaces of the trench 120 and the conductive layer 222. Depending on a shape of the trench 120 and a shape of the conductive layer 222, the cross-section of the first interface layer 224 may have a U-shape. An upper surface 224a of the first interface layer 224 may be coplanar with an upper surface 222a of the conductive layer 222.

[0049] The second interface layer 226 may be disposed on the conductive layer 222 and the first interface layer 224. The second interface layer 226 may cover the upper surface

222a of the conductive layer 222 and the upper surface 224a of the first interface layer 224. The second interface layer 226 may extend from the upper surface 224a of the first interface layer 224 to the upper surface 222a of the conductive layer 222 to cover a top of the conductive layer 222. That is, the first interface layer 224 may cover the side surface of the conductive layer 222, and the second interface layer 226 may cover the upper surface 222a of the conductive layer 222. The upper surface 222a of the conductive layer 222 may not be exposed by the second interface layer 226. The second interface layer 226 may be in contact with the upper surface 224a of the first interface layer 224, and the second interface layer 226 and the first interface layer 224 may be connected to each other. Accordingly, the conductive layer 222 may be surrounded by the first interface layer 224 and the second interface layer 226.

[0050] The first interface layer 224 and the second interface layer 226 may include the same material as the conductive layer 222. The first interface layer 224 and the second interface layer 226 may include the conductive nitride of the first metal. For example, the first metal may include molybdenum (Mo). Here, a composition ratio of the first interface layer 224 and a composition ratio of the second interface layer 226 may be different from a composition ratio of the conductive layer 222. For example, a concentration of nitrogen (N) in the first interface layer 224 and a concentration of nitrogen (N) in the second interface layer 226 may be greater than a concentration of nitrogen (N) in the conductive layer 222. For example, a concentration of molybdenum (Mo) in the first interface layer 224 and a concentration of molybdenum (Mo) in the second interface layer 226 may be less than a concentration of molybdenum (Mo) in the conductive layer 222. In other words, in a conductive part 220 formed of the nitride of the first metal, the first interface layer 224 and the second interface layer 226 may be a nitrogen-rich region, and the conductive layer 222 may be a molybdenum-rich region. The concentration of nitrogen (N) in the first

interface layer 224 and the second interface layer 226 may decrease toward the conductive layer 222. However, the inventive concepts are not limited thereto, and the concentration of nitrogen (N) in the first interface layer 224 and the second interface layer 226 may be substantially uniform.

[0051] When the first interface layer 224 and the second interface layer 226 are formed of the same material and have the same composition ratio as each other, the first interface layer 224 and the second interface layer 226 have a structure connected to each other, and an interface between the first interface layer 224 and the second interface layer 226 may not appear visually. That is, the first interface layer 224 and the second interface layer 226 may be integrally formed. Alternatively, depending on the composition ratio of the first interface layer 224 and the second interface layer 226, the interface between the first interface layer 224 and the second interface layer 226 may appear visually.

[0052] The first interface layer 224 and the second interface layer 226 may lower a flat band voltage of each of the gate lines 200, which means that a work function of each of the gate lines 200 is low. The second interface layer 226 having a low work function may cover the entire upper portion of the conductive part 220, and accordingly, the work function of the upper portion of each of the gate lines 200 may be further lowered. That is, a gate induced leakage drain (GIDL) current generated from upper portions of the gate lines 200 to impurity implantation regions SD1 and SD2 may be reduced.

[0053] Gate insulating patterns 210 may be interposed between the gate lines 200 and the active regions 105, and may also be interposed between the gate lines 200 and the device isolation layer 110. The gate insulating patterns 210 may separate the gate lines 200 from the substrate 100, respectively.

[0054] First capping patterns 230 may be disposed on the gate lines 200. The first capping patterns 230 may be in contact with the upper surface of the second interface layer 226.

Upper surfaces of the first capping patterns 230 may be coplanar with the upper surface of the substrate 100. The gate insulating patterns 210 may extend between the first capping patterns 230 and the active regions 105 or between the first capping patterns 230 and the device isolation layer 110, respectively. Contrary to that shown in FIG 3A, lower surfaces of the first capping patterns 230 may be in contact with the upper surfaces of the gate insulating patterns 210 and the upper surface of the second interface layer 226, and both side surfaces of each of the first capping patterns 230 may be in contact with the active regions 105 or the device isolation layer 110. The first capping patterns 230 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0055] FIG. 4 is a cross-sectional view for explaining a semiconductor device according to some example embodiments of the present inventive concepts.

[0056] Referring to FIG. 4, a substrate 100 may be provided. The substrate 100 may have a first region R1 and a second region R2. The first region R1 and the second region R2 may be regions on the substrate 100 on which transistors are provided. For example, the transistors provided on the first region R1 and the second region R2 may have the same or similar structure and may have different electrical characteristics. This will be described in more detail along with the description of gate lines 200 later.

[0057] A device isolation layer 110 may be disposed on the substrate 100 to define active regions 105. Each of the active regions 105 may have a bar shape when viewed in a plan view.

[0058] A plurality of gate lines 200 may be disposed in the substrate 100 to intersect the active regions 105 when viewed in a plan view. The gate lines 200 may extend in a second direction “Y” and may be disposed in parallel in a first direction “X”. The gate lines 200 may be buried gate lines buried in the substrate 100. The gate lines 200 may be disposed in trenches 120 of the substrate 100 extending to cross the active regions 105.

The gate lines 200 on the first region R1 may include a first conductive layer 222 and a first interface layer 224. The first conductive layer 222 and the first interface layer 224 may constitute a first conductive part 220. The gate lines 200 on the second region R2 may include a second conductive layer 222' and a third interface layer 224'. The second conductive layer 222' and the third interface layer 224' may constitute a second conductive part 220'.

[0059] The configuration of the first conductive part 220 may be substantially the same as or similar to the configuration of the conductive part 220 described with reference to FIGS. 2A and 2B. For example, the first conductive layer 222 may be disposed in the trench 120 of the substrate 100 on the first region R1. The first conductive layer 222 may partially fill the trench 120. The first conductive layer 222 may include a nitride of a first metal having conductivity. For example, the first metal may include molybdenum (Mo). The first interface layer 224 may be interposed between sidewalls and bottom surfaces of the trench 120 in the first region R1 and the first conductive layer 222. The first interface layer 224 may conformally cover a lower surface and an outer surface of the first conductive layer 222. The uppermost end of the first interface layer 224 and the uppermost end of the first conductive layer 222 may be formed at the same level. An upper surface of the first interface layer 224 and an upper surface of the first conductive layer 222 may be formed at a level lower than an upper surface of the substrate 100. The first interface layer 224 may include the same material as the first conductive layer 222. The first interface layer 224 may include the conductive nitride of the first metal. A composition ratio of the first interface layer 224 may be different from a composition ratio of the first conductive layer 222. For example, a concentration of nitrogen (N) in the first interface layer 224 may be greater than a concentration of nitrogen (N) in the first conductive layer 222. For example,

a concentration of molybdenum (Mo) in the first interface layer 224 may be less than a concentration of molybdenum (Mo) in the first conductive layer 222.

[0060] A configuration of the second conductive part 220’ may be similar to the configuration of the first conductive part 220. For example, the second conductive layer 222’ may be disposed in the trench 120 of the substrate 100 on the second region R2. The second conductive layer 222' may partially fill the trench 120. The second conductive layer 222’ may include a nitride of the first metal having conductivity. For example, the first metal may include molybdenum (Mo). The third interface layer 224’ may be interposed between the sidewalls and bottom surfaces of the trench 120 in the second region R2 and the second conductive layer 222’. The third interface layer 224’ may conformally cover a lower surface and an outer surface of the second conductive layer 222’. The uppermost end of the third interface layer 224’ and the uppermost end of the second conductive layer 222’ may be formed at the same level. An upper surface of the third interface layer 224’ and an upper surface of the second conductive layer 222’ may be formed at a level lower than the upper surface of the substrate 100. The third interface layer 224’ may include the same material as the second conductive layer 222’. The third interface layer 224’ may include the conductive nitride of the first metal. A composition ratio of the third interface layer 224’ may be different from a composition ratio of the second conductive layer 222’. For example, a concentration of nitrogen (N) in the third interface layer 224’ may be greater than a concentration of nitrogen (N) in the second conductive layer 222’. For example, a concentration of molybdenum (Mo) in the third interface layer 224’ may be less than a concentration of molybdenum (Mo) in the second conductive layer 222’.

[0061] A thickness of the first interface layer 224 and a thickness of the third interface layer 224’ may be different from each other. For example, the thickness of the first

interface layer 224 may be greater than the thickness of the third interface layer 224'. The thickness of the first interface layer 224 and the thickness of the third interface layer 224' may be 5Å to 30Å, respectively.

[0062] The first interface layer 224 and the third interface layer 224' may be liner layers provided for lowering a flat band voltage of each of the gate lines 200. Because the thickness of the first interface layer 224 and the thickness of the third interface layer 224' are different from each other, work functions of the gate lines 200 on the first region R1 and work functions of the gate lines 220 on the second region R2 may be different from each other. That is, transistors having different threshold voltages may be provided on the first region R1 and the second region R2, respectively.

[0063] Alternatively, the thickness of the first interface layer 224 and the thickness of the third interface layer 224' may be the same. Here, the nitrogen concentration in the first interface layer 224 and the nitrogen concentration in the third interface layer 224' may be different from each other. For example, the nitrogen concentration in the first interface layer 224 may be greater than the nitrogen concentration in the third interface layer 224'. Accordingly, the work functions of the gate lines 200 in the first region R1 may be smaller than the work functions of the gate lines 200 in the second region R2. That is, transistors having different threshold voltages may be provided on the first region R1 and the second region R2, respectively.

[0064] FIGS. 5A to 10A are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line I-I' of FIG. 1. FIGS. 5B to 10B are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond

to cross-sections taken along line II-II' of FIG. 1. FIG. 8C is an enlarged view of area "A" of FIG. 8A.

[0065] Referring to FIGS. 1, 5A, and 5B, a device isolation layer 110 defining active regions 105 may be formed on a substrate 100. For example, the device isolation layer 110 may be formed using a shallow trench isolation (STI) method. The device isolation layer 110 may include silicon oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON). The device isolation layer 110 may be formed to extend into the substrate 100.

[0066] Second impurity implantation regions SD2 may be formed in the active regions 105 of the substrate 100. The second impurity implantation regions SD2 may be formed by an ion implantation process. For example, the second impurity implantation regions SD2 may be regions doped with an N-type dopant.

[0067] Referring to FIGS. 1, 6A, and 6B, mask patterns MP may be formed on the substrate 100. The mask patterns MP may be formed to have openings defining regions in which gate lines 200 (refer to FIGS. 2A and 2B) to be described below are disposed. The mask patterns MP may be a hard mask pattern such as silicon nitride (SiN) or a photo resist pattern. Line-shaped trenches 120 extending in a second direction "Y" may be formed by etching the substrate 100 and the device isolation layer 110, using the mask patterns MP as an etching mask. Bottom surfaces of the trenches 120 may expose the device isolation layer 110 and the active regions 105.

[0068] Subsequently, gate insulating patterns 210 may be formed in the trenches 120, respectively. The gate insulating patterns 210 may be formed by a thermal oxidation process, atomic layer deposition (ALD), or chemical vapor deposition (CVD). For example, the gate insulating patterns 210 may be formed of silicon oxide (SiO_2) formed on the exposed surface of the substrate 100 by a thermal oxidation process. Here, the gate insulating patterns 210 may be formed on sidewalls and bottom surfaces of the trenches 120.

Here, the gate insulating patterns 210 may conformally cover the inside of the trenches 120 (i.e., sidewalls and bottom surfaces of the trenches 120). Alternatively, the gate insulating patterns 210 may include silicon oxide (SiO_2), silicon nitride (SiN), silicon oxynitride (SiON), or high dielectric material which is formed by a LPCVD process, a PECVD process, a UHV-CVD process, or an ALD process. Here, the gate insulating patterns 210 may conformally cover the inside of the trenches 120 and the mask patterns MP.

[0069] Referring to FIGS. 1, 7A, and 7B, a preliminary conductive layer 240 may be formed on the substrate 100. In detail, the preliminary conductive layer 240 may be formed by depositing a conductive material on the entire surface of the substrate 100. Here, the conductive material may fill the trenches 120. In detail, the preliminary conductive layer 240 may be formed using a first precursor material including molybdenum (Mo) and a second precursor material including nitrogen. For example, the first precursor material may include $Mo_xO_yCl_z$, and the second precursor material may include ammonia (NH_3). The first precursor material and the second precursor material may react to form $Mo_aO_bN_c$, N_d, H_2O, and HCl. The deposition process of the conductive material may be performed at a temperature of 550 degrees or more. As the process temperature of the deposition process increases, “b” and “c” of $Mo_aO_bN_c$ may decrease, and “d” of Nd may increase. When the process temperature of the deposition process is lower than 550 degrees, a nitrogen concentration in the preliminary conductive layer 240 may be low, and the preliminary interface layer 242 having a high nitrogen concentration may not be formed in a process to be described later. The depositing of the conductive material may be performed using various deposition processes, such as a chemical vapor deposition (CVD) process or atomic layer deposition (ALD). The conductive material may include a low resistance (low-R) material. The conductive material may include a nitride of a first metal

having conductivity. For example, the conductive material may include molybdenum (Mo).

[0070] Referring to FIGS. 1 and 8A to 8C, a preliminary interface layer 242 may be formed by performing a first process. For example, the preliminary interface layer 242 may be formed by diffusing nitrogen atoms in the preliminary conductive layer 240 into a part of the preliminary conductive layer 240. Here, the part of the preliminary conductive layer 240 means a part adjacent to outer surfaces of the preliminary conductive layer 240. For example, the part may be a part of the preliminary conductive layer 240 adjacent to an interface between the preliminary conductive layer 240 and the gate insulating patterns 210. That is, the preliminary interface layer 242 may be interposed between the preliminary conductive layer 240 and the trenches 120 or the preliminary conductive layer 240 and the gate insulating patterns 210. A thickness of the preliminary interface layer 242 may be 5Å to 30Å.

[0071] To describe the first process in more detail, the nitrogen atoms of the preliminary conductive layer 240 may be diffused into the outer portion of the preliminary conductive layer 240 along an arrow AF of FIG. 8C by the first process. The outer portion of the preliminary conductive layer 240 having an increased nitrogen concentration may constitute the preliminary interface layer 242. A nitrogen concentration inside the preliminary conductive layer 240 may be lowered. Accordingly, the nitrogen concentration of the preliminary interface layer 242 may be higher than the nitrogen concentration of the preliminary conductive layer 240. Along the diffusion direction AF of the nitrogen atoms, the nitrogen concentration in the preliminary conductive layer 240 may decrease from the outer surface and lower surfaces of the preliminary conductive layer 240 toward the inside of the preliminary conductive layer 240. Alternatively, the nitrogen concentration in the

preliminary conductive layer 240 may be substantially uniform in the preliminary conductive layer 240. The first process may include a heat treatment process. That is, the nitrogen atoms in the preliminary conductive layer 240 may be diffused by heat HT provided from the outside. The heat treatment process may include a rapid thermal annealing (RTA) process.

[0072] Referring to FIGS. 1, 9A, and 9B, an etch back process may be performed on the preliminary conductive layer 240 and the preliminary interface layer 242. For example, a conductive layer 222 and an interface layer 224 may be formed by etching the preliminary conductive layer 240 and the preliminary interface layer 242. During the etching process, the conductive layer 222 and the interface layer 224 may be etched together. For example, the conductive layer 222 and the interface layer 224 may be formed of the same material, and an etchant for etching the conductive layer 222 and the interface layer 224 may be the same. The etching process may be continued until the conductive layer 222 and the interface layer 224 remain in the trenches 120 to a desired thickness. Here, an upper surface of the interface layer 224 may be formed to be at the same level as an upper surface of the conductive layer 222. Alternatively, the upper surface of the interface layer 224 and the upper surface of the conductive layer 222 may be disposed at different heights depending on difference in etch rates between the conductive layer 222 and the interface layer 224. For example, the upper surface of the interface layer 224 may be disposed at a level lower than the upper surface of the conductive layer 222.

[0073] Thereafter, the mask patterns MP may be removed. As the mask patterns MP are removed, the upper surfaces of the device isolation layer 110 and the active regions 105 may be exposed.

[0074] Referring to FIGS. 1, 10A, and 10B, first capping patterns 230 may be formed in the trenches 120. For example, the first capping patterns 230 may be formed by forming a

capping layer on the entire surface of the substrate 100 and then performing a planarization process or the like. The first capping patterns 230 may include any one of oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0075] An ion implantation process may be performed on the substrate 100, and thus a first impurity implantation region SD1 may be formed in regions between two adjacent gate lines 200. The first impurity implantation region SD1 may be doped with the same N-type impurity as the second impurity implantation region SD2. The first impurity implantation region SD1 may extend deeper into the substrate 100 than the second impurity implantation region SD2.

[0076] Referring back to FIGS. 1, 2A, and 2B, a polysilicon layer doped with impurities, a silicon single crystal layer doped with impurities, or a conductive layer may be formed on the substrate 100 and may be patterned, thereby forming a first pads 310 and second pads 320. The first pads 310 may be connected to the first impurity implantation region SD1, and the second pads 320 may be connected to the second impurity implantation region SD2, respectively. When the first pads 310 and the second pads 320 include a polysilicon layer doped with impurities or a silicon single crystal layer, the first pads 310 and the second pads 320 may be doped with the same type of impurities as those of the first and second impurity implanted regions SD1 and SD2.

[0077] A first interlayer insulating layer 400 may be formed on the first and second pads 310 and 320. The first interlayer insulating layer 400 may be formed using a chemical vapor deposition (CVD) process or the like. The first interlayer insulating layer 400 may include oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON). The first interlayer insulating layer 400 may be partially patterned to form contact holes defining regions in which direct contacts 520 are to be formed. A conductive material filling the contact holes may be coated on the first interlayer insulating layer 400, and a capping layer

may be formed thereon. For example, the conductive material may include a conductive material such as a metal or a doped semiconductor. For example, the capping layer may include any one of oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON). A bit line 510 and second capping patterns 530 disposed thereon may be formed by patterning the capping layer and the conductive material. Direct contacts 520 may be formed in the contact holes. Insulating spacers 540 covering sidewalls of the bit line 510 may be formed by conformally depositing an insulating spacer layer on the first interlayer insulating layer 400 and performing anisotropic etching. The insulating spacers 540 may include any one of oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0078] A second interlayer insulating layer 550 may be formed on the first interlayer insulating layer 400 and may perform a planarization process to expose upper surfaces of the second capping patterns 530. Thereafter, buried contacts 610 connected to the second pads 320 may be formed through the second interlayer insulating layer 550 and the first interlayer insulating layer 400. The buried contacts 610 may include a conductive material such as doped silicon or metal. A support layer 700 may be formed on the second interlayer insulating layer 550. The support layer 700 may include any one of oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON). The support layer 700 may be formed using various deposition processes, such as a chemical vapor deposition (CVD) process or atomic layer deposition (ALD). A first electrode 620 connected to the buried contacts 610 may be formed through the support layer 700. The first electrode 620 may be formed in a cylindrical shape with a closed bottom. A dielectric layer 630 covering the first electrode 620 may be formed, and a second electrode 640 commonly covering the first electrode 620, and thus a capacitor CA may be formed. The first electrode 620 and the second electrode 640 may include silicon doped with impurities, a metal, or a metal compound. Therefore, the semiconductor device described with reference to FIGS. 2A and 2B may be formed.

[0079] FIGS. 11A to 13A are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line I-I' of FIG. 1. FIGS. 11B to 13B are cross-sections for explaining a method of fabricating a semiconductor device according to some example embodiments of the present inventive concepts, and correspond to cross-sections taken along line II-II' of FIG. 1.

[0080] Referring to FIGS. 1, 11A, and 11B, an etch back process may be performed on a preliminary conductive layer 240 in a resultant of FIG. 7. For example, a conductive layer 222 may be formed by etching the preliminary conductive layer 240. The etching process may continue until the conductive layer 222 remains in the trenches 120 to a desired thickness. After the etching process, an upper surface of the conductive layer 222 may be positioned at a level lower than an upper surface of a substrate 100.

[0081] Referring to FIGS. 1, 12A, and 12B, a first interface layer 224 and a second interface layer 226 may be formed by performing a second process. For example, the first interface layer 224 and the second interface layer 226 may be formed by diffusing nitrogen atoms in the conductive layer 222 into a part of the conductive layer 222. Here, the part of the conductive layer 222 means a part adjacent to outer surfaces of the conductive layer 222. For example, the part may be a part of the conductive layer 222 adjacent to an interface between the conductive layer 222 and gate insulating patterns 210 and a part adjacent to the upper surface of the conductive layer 222. In detail, the first interface layer 224 may be interposed between the conductive layer 222 and trenches 120 or the conductive layer 222 and the gate insulating patterns 210, and the second interface layer 226 may be formed adjacent to the upper surface of the conductive layer 222. A thickness of the first interface layer 224 and a thickness of the second interface layer 226 may be 5Å to 30Å.

[0082] To describe the second process in more detail, nitrogen atoms of the conductive layer 222 may be diffused to an outer portion of the conductive layer 222 along an arrow AF by the second process. The outer portion of the conductive layer 222 having an increased nitrogen concentration may be formed to form the first interface layer 224 and the second interface layer 226. The nitrogen concentration inside the conductive layer 222 may be lowered. Accordingly, a nitrogen concentration of the first interface layer 224 and the second interface layer 226 may be higher than a nitrogen concentration of the conductive layer 222. Along the diffusion direction AF of the nitrogen atoms, the nitrogen concentration in the first interface layer 224 and the second interface layer 226 may be decrease from the outer surface, lower surface, and upper surface of the conductive layer 222 toward the inside of the conductive layer 222. Alternatively, the nitrogen concentration in the conductive layer 222 may be substantially uniform in the conductive layer 222. The second process may include a heat treatment process. That is, the nitrogen atoms in the conductive layer 222 may be diffused by heat HT provided from the outside. The heat treatment process may include a rapid thermal annealing (RTA) process.

[0083] Referring to FIGS. 1, 13A, and 13B, first capping patterns 230 may be formed in the trenches 120. For example, the first capping patterns 230 may be formed by forming a capping layer on the entire surface of the substrate 100 and then performing a planarization process or the like. The first capping pattern 230 may be formed on the second interface layer 226. The first capping patterns 230 may include any one of oxide (SiO_2), silicon nitride (SiN), or silicon oxynitride (SiON).

[0084] An ion implantation process on the substrate 100 may be performed, and thus a first impurity implantation region SD1 may be formed in regions between two adjacent gate lines 200. The first impurity implantation region SD1 may be doped with the same N-type impurity as the second impurity implantation region SD2. The first impurity implantation

region SD1 may extend deeper into the substrate 100 than the second impurity implantation region SD2.

[0085] Thereafter, the process described with reference to FIGS. 1, 2A, and 2B may be performed. For example, first pads 310 and second pads 320 may be formed on the substrate 100. The first pads 310 may be connected to the first impurity implantation region SD1, and the second pads 320 may be connected to the second impurity implantation region SD2. A first interlayer insulating layer 400 may be formed on the first and second pads 310 and 320. A direct contact 520 may be formed in the first interlayer insulating layer 400. A bit line 510 and second capping patterns 530 disposed thereon may be formed on the first interlayer insulating layer 400. Insulation spacers 540 covering sidewalls of the bit line 510 may be formed on the first interlayer insulating layer 400. A second interlayer insulating layer 550 may be formed on the first interlayer insulating layer 400, and a planarization process may be performed to expose upper surfaces of the second capping patterns 530. Thereafter, buried contacts 610 connected to the second pads 320 may be formed through the second interlayer insulating layer 550 and the first interlayer insulating layer 400. A support layer 700 may be formed on the second interlayer insulating layer 550. A first electrode 620 connected to the buried contacts 610 may be formed through the support layer 700. A dielectric layer 630 conformally covering the first electrode 620 may be formed, and a second electrode 640 commonly covering the first electrode 620 may be formed, thereby forming a capacitor CA. Accordingly, the semiconductor device described with reference to FIGS. 3A and 3B may be formed.

[0086] According to the semiconductor device according to the example embodiments of the inventive concepts, the interface layer may be provided on the surface of the conductive layer, and thus the flat band voltage of the gate lines may be lowered. That is, the work

function of the gate lines may be reduced by the interface layer, and the threshold voltage of the semiconductor device may be lowered.

[0087] Furthermore, the interface layer may be provided on the sidewalls of the gate lines, and thus the leakage current generated from the upper portions of the gate lines to the impurity implantation regions may be reduced.

[0088] In addition, the interface layer and the conductive layer may include the same material as each other, include a different composition ratio from each other, and thus the interfacial resistance between the interface layer and the conductive layer may be small.

[0089] The threshold voltage of the semiconductor device may be low while the interfacial resistance between the constituent layers in the gate lines is small. Accordingly, the electrical characteristics of the semiconductor device may be improved.

[0090] In the semiconductor device according to the example embodiments of the inventive concepts, the interface layers in the regions in which the transistors are provided may have different configurations, and the work functions of the gate lines in each of the regions may be different from one another. That is, the transistors having different threshold voltages may be provided on each of the regions.

[0091] While example embodiments of the inventive concepts have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the attached claims.

WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, the method comprising:

forming a device isolation layer defining active regions on a substrate; and

forming gate lines intersecting the active regions and buried in the substrate,

wherein the forming of the gate lines includes:

forming a trench intersecting the active regions in the substrate;

forming a conductive layer filling the trench; and

performing a heat treatment process on the conductive layer,

wherein the conductive layer includes a nitride of a first metal, and

wherein nitrogen atoms in the conductive layer are diffused toward an outer surface and a lower surface of the conductive layer by the heat treatment process.

2. The method of claim 1, wherein, after the heat treatment process, a concentration of nitrogen atoms in the conductive layer decreases from the outer surface and the lower surface of the conductive layer toward an inside of the conductive layer.

3. The method of claim 1 or claim 2, wherein a part of the conductive layer in which the nitrogen atoms are diffused forms a first interface layer,

wherein the first interface layer includes the nitride of the first metal, and

wherein a nitrogen concentration in the first interface layer is higher than a nitrogen concentration in the conductive layer.

4. The method of claim 3, wherein the first interface layer is formed adjacent to the outer surface and the lower surface of the conductive layer.

5. The method of claim 3 or claim 4, wherein, after the heat treatment process, other part of the conductive layer in which the nitrogen atoms are diffused forms a second interface layer, and

wherein the second interface layer is formed adjacent to an upper surface of the conductive layer.

6. The method of any one of claims 3 to 5, wherein a flat band voltage of a material constituting the first interface layer is lower than a flat band voltage of a material constituting the conductive layer.

7. The method of any one of claims 3 to 6, wherein a thickness of the first interface layer is from 5Å to 30Å.

8. The method of claim 3 or claim 4, further comprising etching the first interface layer and the conductive layer,

wherein an upper surface of the first interface layer and an upper surface of the conductive layer are formed to be positioned at the same plane.

9. The method of any one of claims 1 to 8, wherein the forming of the conductive layer includes reacting a first precursor material including the first metal and a second precursor material including nitrogen, and

wherein the forming of the conductive layer is performed at a process temperature of 550 degrees or more.

10. The method of any one of claims 1 to 9, wherein the first metal includes molybdenum (Mo).

11. The method of any one of claims 1 to 10, further comprising forming a capping layer on the gate lines.

12. The method of any one of claims 1 to 11, further comprising forming a gate insulating pattern on a sidewall and a bottom surface of the trench before the forming of the conductive layer.

13. A method of fabricating a semiconductor device, the method comprising:

forming a device isolation layer defining active regions on a substrate;

forming trenches intersecting the active regions;

forming a conductive layer filling a lower portion of each of the trenches, the conductive layer including a nitride of a first metal;

forming a first interface layer adjacent to an outer surface and a lower surface of the conductive layer, the first interface layer including the nitride of the first metal; and

forming a capping layer filling an upper portion of each of the trenches,

wherein a nitrogen concentration in the first interface layer is higher than a nitrogen concentration in the conductive layer.

14. The method of claim 13, wherein the forming of the first interface layer includes:

performing a heat treatment process on the conductive layer; and

diffusing nitrogen atoms in the conductive layer toward the outer surface and the lower surface of the conductive layer through the heat treatment process, to form the first interface layer.

15. The method of claim 14, wherein a part of the nitrogen atoms in the conductive layer are diffused toward an upper surface of the conductive layer through the heat treatment, to form a second interface layer.

16. The method of any one of claims 13 to 15, wherein the forming of the conductive layer includes reacting a first precursor material including the first metal and a second precursor material including nitrogen, and

wherein the forming of the conductive layer is performed at a process temperature of 550 degrees or more.

17. The method of any one of claims 13 to 16, wherein a concentration of nitrogen atoms in the first interface layer decreases toward the conductive layer.

18. The method of claim 13 or claim 14, further comprising etching the first interface layer and the conductive layer,

wherein an upper surface of the first interface layer and an upper surface of the conductive layer are formed to be provided at the same plane.

19. The method of any one of claims 13 to 18, wherein a thickness of the first interface layer is from 5Å to 30Å.

20. The method of any one of claims 13 to 19, wherein the first metal includes molybdenum (Mo).