

ABSTRACT

A clock recovery circuit has at least two comparators that detect timings at which a digitally modulated signal crosses different levels, and generate level crossing signals at these timings. A classifying circuit classifies sequences of these level crossing signals and issues corresponding classification signals. A timing control circuit generates timing pulses from certain combinations of the level crossing signals and classification signals. A digital phase-locked loop outputs a clock signal synchronized to these timing pulses.

This Sheet Has Been Replaced

