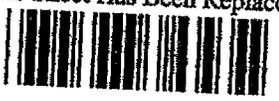
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A DRIVER

The invention relates to a driver, particularly to an LCD driver with no variable level output for achieving a variable voltage level driving of an LCD.

Certain liquid crystal displays (LCDs) driven by different levels will generally have different responses. For example:

(i) Grey levels — contrast can be varied according to input voltage levels;

(ii) colour — some LCDs can appear in different colours according to input voltage levels;

(iii) other properties — such as response time, etc. Most drivers for such different voltage level provision for LCDs only output a preset voltage level so that a particular driven pixel of the LCD is either ON or OFF. Special drivers are needed to output different voltage levels according to input date; these are known as drivers with grey level outputs.

Such provision of different circuits is expensive, as each circuit is itself expensive, and a selection of various circuits has to be provided.

It is an object of the invention to seek to mitigate this disadvantage.

According to the invention, there is provided a driver for a liquid crystal display (LCD), comprising fixed preset drive voltage levels and means for varying an ON:OFF ratio over a number of cycles, whereby effectively to present variable driving voltage levels for driving an LCD.

Using the invention it is possible to provide a driver for an LCD without a variable output voltage which is nevertheless being used to drive an LCD

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requiring variable driving voltage levels.

The means may comprise a circuit inserted between a controller output of the driver and an input of a column driver of the LCD. Suitably, the column driver may comprise a serial input column driver.

Suitably, the driver may include a decoder for data, a frame controller for the LCD and a data selector adapted to receive input from the decoder and data controller and having a multi-level routing circuit for outputting to the column driver.

The data selector may comprise up to $\varkappa$ levels and may be adapted to operate over N cycles where $N = \varkappa$.

Alternatively, the data selector may comprise $\varkappa$ different levels and may be adapted to operate over N levels of response, where N is less than $\varkappa$.

In one embodiment of driver, one complete cycle may last $\varkappa$ frames. The value $\varkappa$ may be 16.

It will be understood that the effective output voltage applied to an LCD pixel may be p/p+q, where p is the number of times the pixel is driven ON and q the number of times the pixel is driven OFF.

It will be understood too that the invention in another aspect extends to an LCD including a driver as hereinbefore defined.

Voltage waveforms driving multiplexed displays are usually pre-determined multi-level waveforms. In the specification, the term "voltage level" refers to the

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effective voltage levels of such complex waveforms, not levels in a multi-level waveform. Sometimes this is also known as the root-mean-square (RMS) voltage as an LCD is believed to respond to RMS value of driving voltage.

It will be understood that if a pixel of a monochrome LCD is driven alternately ON and OFF fast enough, the pixel appears to be somewhere between full ON and full OFF, the exact response depending on the characteristic of the LCD in use. Its response is as though an effective voltage of the value of half the full ON value has been applied to the pixel. Therefore assuming the full ON voltage is 1 and the OFF voltage is *o*, if the pixel is driven with 1 *o* 1 *o* 1 *o* .... for example, the average voltage is 0.25. The pixel will appear even dimmer and so on. Thus a driver with fixed preset drive levels can vary the ON vs OFF ratio over a number of cycles effectively to present a driving voltage equivalent to $T_{ON}/(T_{ON} + T_{OFF})$ of the full-ON driving voltage level.

If the particular LCD displays different colour when driven with different effective voltages, the above driving signals will cause different colours to appear. If there are other properties of LCD which depends on voltage levels, they too can be varied using a driver embodying the invention.

A driver embodying the invention is hereinafter described, by way of example, with reference to the accompanying drawings.

Fig. 1 is a block diagram of a prior art driver for driving an LCD;

Fig. 2 is a block diagram of a driver for driving an LCD according to the invention;

Fig. 3 is an enlarged block diagram of a circuit of the invention;

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Fig. 4 shows a turning relationship of signals for driving a 64 (column) X 16 (row) dot matrix display; and

Fig. 5 shows how a frame signal (FRM) from the controller causes outputs to be stepped through each frame.

Referring to the drawings, a driver 1 for a liquid crystal display (LCD) comprises fixed preset voltage levels 2, and means 3 for varying an ON:OFF ratio over a number of cycles whereby effectively to present variable driving voltage levels 4 for driving an LCD (not shown).

An example of how to drive a 64 (column) X 16 (row) dot matrix display is illustrated in Fig. 1. The arrangement is applicable to any dot-matrix displays of different resolutions. The controller can either be a dedicated LCD controller or it can be a general purpose system designed to control an LCD. The controller accepts commands and displays data from the host system via the interface bus. Typical interface signals are: data bus (D0 - D7, 8-bit data bus shown) of appropriate width, enable signal (E) serving to indicate to the controller that it owns the interface bus, read/write (R/W), reset (RES), command or data input (A0). Typical commands are numbers of ways of multiplex, number of segments, frame speed, clear entire display, etc. The controller upon receiving the commands will configure itself accordingly. It will also place any data input into the display RAM ready to be output to the column drivers via its output data bus. The minimum amount of SRAM in the example is 64 x 16 bits. For simplicity in the example, the RAM is organised as 16 rows of 64 bit each, corresponding to the display pixels, and "1" will mean ON and "0" will mean OFF.

In Fig. 1, typical output signals of the controller are the output data bus,

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consisting of a 4-bit bus (DO*o* - DO3), start of frame signal (FRM), row advance signal (CL1), valid data for display (CL2) and phase of driving voltage (M). This last signal signifies to the row and column drivers to use alternate positive and negative phases of driving waveform to eliminate DC components. A frame is completed when every pixel of a display has been driven once.

All operations can use FRM as the start. FRM and CL1 will signify start of first row. The row driver will output ON (select) signal to row 1 and OFF (non-select) signal to other rows. Subsequent CL1 will advance the driving to subsequent rows. For instance, second CL1 will cause row 2 to be driven ON and other rows OFF, etc.

FRM, CL1 and CL2 will cause the data bits DO*o* to DO3 to be latched onto the first 4 locations of the data register of the column driver. Subsequent CL2 will cause subsequent DO*o* to DO3 to be latched to the second 4 locations of the data register. Usually, shift registers are used such that earlier latched data are shifted left, say, by 4 bits and the latest data are latched to the last 4 bits. After 16 such CL2 signals as in this example, all 64 bits of data for one row of display are in the data register in their proper locations. The next CL1 signal will cause this row of data to be latched by the display register to drive the row of selected display. The data register is ready to accept the next row of data, 4 bits at a time, from the controller. The timing relationship of the signals M, FRM, CL1 and CL2 are illustrated in Fig. 4. Shifting and latching of data by the column driver from the controller is not limited to 4 bits. In fact, it can be from 1 bit to any number of bits. Here 4 bits is used as an example, Fig. 1.

In Fig. 1, after 16 CL1 signals, all the bit data in the RAM will have been transferred to the column drivers, 16 rows of 64 bits, to drive the display. The operation starts again with the next set of FRM, CL1 and CL2 signals.

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Referring now to Fig 2, there is shown how an LCD controller and drivers not ordinarily used for variable effective voltage level outputs can be used to drive an LCD to produce responses as though variable effective voltage level drives are present. Specifically, the controller and drivers can only output voltages either to drive a pixel ON or OFF. A driver embodying the invention will cater for cases when the pixel is required to be driven with effective voltage levels between and including ON and OFF. The phenomenon described above is used. The circuit 3 is inserted between the controller output and the column driver input. The circuit receives the data signifying the desired voltage levels to drive the pixel from the controller and transform these data to a series of outputs. These outputs are presented to the column driver one per frame such that over (p+q) frames the pixel is driven p times ON and q times OFF. The response of the pixel over (p + q) frames will approximate as though an effective voltage of [p/(p+q)] times the ON voltage had been applied to the pixel. The frame signal, FRM, from the controller serves to cause the outputs to be stepped through after each frame. This is illustrated in Fig. 5.

Using as an example 4 bits to specify the output voltage levels, the size of RAM is increased to 16 rows of 256 bit per row. Now, instead of each bit of data in the display RAM signifying that a pixel is ON or OFF, every 4 bits of data will signify from OFF to full ON in 16 levels depending on the bit patterns. Thus pattern *oooo* means full OFF, *ooo*1 means driving the LCD at 1/16 of the full ON voltage level, and so on. Other coding methods or no coding are also possible. The controller is programmed to expect 16 line of 256 display format. It will output a CL1 signal after outputting every 256 bit of data, and a FRM signal every 16 lines. The LCD display being driven is still 16 lines of 64 bits. Using a monochrome LCD, only the contrast ratio is changed when driven by different effective voltages. The driver can drive other properties of an LCD responding to different effective voltage levels. An example of this is colour

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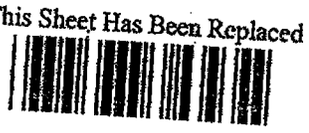


LCD, namely if an LCD changes colour when driven by different effective voltage levels.

The circuit 3 is inserted between the controller and the column driver to effect an effective variable driving voltage level. The circuit 3 (CIRC) will intercept the 4 bit data output by the controller each CL2 strobe. Each such 4-bit data will be interpreted as signifying voltage levels to be applied to the LCD pixel. Assuming no coding is used in the 4 bit data, namely the pixel is driven ON or OFF in accordance with bit patterns being "1" or "*o*". The CIRC 3 will sequentially output DO*o*, DO1, DO2 or DO3 to the column driver at each frame. Initially, during the whole of the first frame, DO*o*is routed to the column driver 4. This can be achieved by usual circuits such as a 4-to-1 multiplexer or any other signal routing circuits. Therefore, bits OO, 04, 08 ..., 10, 14... in RAM are fed to the column driver 4 during this frame. This lasts until a new FRM signal is received. Then, DO1 will be output to the column driver 4, namely, bits 01, 05, 09,... 11, 16, 19... in RAM are fed to the column driver 4. DO2 and DO3 will be used in sequence after each FRM signal. Then, the cycle repeats. If the 4 bits (OO, 01, 02, & 03 for the first pixel for instance) for the pixel is *oooo*, then the pixel will be driven OFF in all 4 frames. If the bits are 1*o*1*o*, say, then the pixel will be driven ON in two of the frames and OFF in the other two frames and thus will appear half ON. If the 4 bits are 1111, then the pixel is driven full ON in all 4 frames and will appear full ON. The cycle lasts over 4 frames. The levels can be from 0, 1/4, 1/2, 3/4 and 1.

The column driver 4 in the embodiment is a serial input type, namely, accepting 1 bit data each CL2 strobe, instead of 4-bit data as described above. There are many column drivers of this type available. There is no need to include a divided by 4 circuit after using a 1 bit input column driver.

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Considering the 4 bit data to be binary coded, a total of 16 levels can be represented and a decoder 5 can be inserted before the now 16-to-1 signal routing circuit. The decoder 5 will accept the 4 bit input at each CL2 strobe and present 16 outputs to the signal routing circuit. If the 4 bit inputs are *oooo*, then all 16 outputs can be *o*'s. If the 4 bit inputs are *ooo*1, then only one of the 16 outputs will be 1 with all others being *o*. If the 4 bit inputs are *oo*1*o*, then two of the 16 outputs will be 1's with the others being *o*, and so on. A 4 bit pattern of all 1's will cause all 16 outputs to be 1's and the pixel is driven ON in every frame. The exact decoder circuit required will depend on the coding on the 4 bit input data. One complete cycle will now last 16 frames. This is illustrated in Fig. 3. It should be noted that, although the example in Fig. 3 uses 4 bit data to implement a 16 to 1 demultiplexor, N bit data can be used to implement a 2^N to 1 demultiplexor, where N is any integer. N is not limited to 4 bits.

It will be understood that there are many different combinations possible. For example, there may be 4 bits to represent 16 levels and only n levels ($n \leq 16$) may be used and the cycle may last over n frames only. One possible, (although by no means the only) application of this variation is when the LCD response is non-linear. 16 different levels are then needed to effect only n levels of response as some adjacent levels would produce only an insignificant variation in output properties such as grey levels or colours.

A driver as hereinbefore described with reference to the accompanying drawings thus provides a way drivers without variable output voltage levels can be used to drive an LCD requiring variable voltage levels. Thus the driver can drive a dot matrix driving arrangement from fixed output voltage levels, thereby achieving a relatively inexpensive, flexible driver.

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* C L M S *

CLAIMS

1. A driver for a liquid crystal display (LCD) comprising fixed preset drive voltage levels and means for varying an ON:OFF ratio over a number of cycles, whereby effectively to present variable driving voltage levels for driving an LCD.

2. A driver according to Claim 1, the means comprising a circuit inserted between a controller output of the driver and an input of a column driver of the LCD.

3. A driver according to Claim 2, the column driver comprising a serial input column driver.

4. A driver according to Claim 2 or Claim 3, the circuit comprising a decoder for data, a frame controller for the LCD, and a data selector adapted to receive input from the decoder and data controller and having a multi-level routing circuit for outputting to the column driver.

5. A driver according to Claim 4, the data selector comprising up to $\varkappa$ levels and being adapted to operate over n cycles where $n = \varkappa$.

6. A driver according to Claim 4, the data selector comprising $\varkappa$ different levels and being adapted to operate over n levels of response where n is less than $\varkappa$.

7. A driver according to Claim 5 or Claim 6, one complete cycle lasting $\varkappa$ frames.

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8. A driver according to any of Claims 2 to 7, the effective output voltage applied to an LCD pixel being p/p+q, when p is the number of times the pixel is driven ON and q the number of times the pixel is driven OFF.

9. An LCD, including a driver according to any preceding claim.