Claims

1. Method comprising the following steps:

   providing a Silicon-On-Insulator, SOI, stack comprising a substrate layer, a first oxide layer on the substrate layer and a silicon layer on the first oxide layer (BOX layer);

   forming at least one first region of the SOI stack wherein the silicon layer is thinned by thermally oxidizing a part of the silicon layer; and

   forming at least one second region of the SOI stack wherein the first oxide layer (BOX layer) is thinned by annealing.

2. The method according to claim 1, wherein the steps of annealing and thermal oxidizing are performed in the same process chamber.

3. The method according to claim 2, wherein the annealing and thermal oxidizing are performed in a single continuous process step wherein the composition of the atmosphere in the process chamber and the temperature are modified according to anneal and oxidation conditions.

4. The method according to one of the preceding claims, wherein the at least one first region and the at least one second region at least partially overlap each other.

5. The method according to one of the preceding claims, further comprising forming at least one shallow trench isolation in the SOI stack after performing the anneal and/or the oxidation to define a first and a second device area.

6. The method according to one of the preceding claims, further comprising:

forming a second oxide layer on the silicon layer and a first mask layer on the second oxide layer;

patterning the second oxide layer and the first mask layer to expose a first part of the silicon layer; and

thermally oxidizing the exposed silicon layer to form a silicon oxide layer on the previously exposed silicon layer and a first thinned silicon layer.

7. The method according to claim 6, further comprising forming a second mask layer on a part of the silicon oxide layer and thermally oxidizing a part of the first thinned silicon layer located beneath the part of the silicon oxide layer that is not covered by the second mask layer thereby forming another silicon oxide layer and a second thinned silicon layer.

8. The method according to claim 6, further comprising subsequently forming a shallow trench isolation between a first device area comprising the part of the silicon layer not previously exposed by the patterned second oxide layer and first mask layer and a second device area comprising the first thinned silicon layer.

9. The method according to claim 7, further comprising subsequently forming a first shallow trench isolation between a first device area comprising the part of the silicon layer not previously exposed by the patterned second oxide layer and first mask layer and a second device area comprising the first thinned silicon layer and forming a second shallow trench isolation between the second device area and a third device area comprising the second thinned silicon layer.

10. The method according to claim 6, further comprising removing the silicon oxide layer from the first thinned silicon layer and subjecting the resulting structure to an anneal process, in particular, in an anneal ambient comprising Ar and/or N_2,

thereby partially dissolving the part of the first oxide layer beneath the first thinned silicon layer in order to obtain a first thinned silicon oxide layer.

11. The method according to claim 7, further comprising removing the other silicon oxide layer from the second thinned silicon oxide layer and subjecting the resulting structure to an anneal process, in particular, in an anneal ambient comprising Ar and/or N_2, thereby partially dissolving the part of the first oxide layer beneath the second thinned silicon layer in order to obtain a second thinned silicon oxide layer.

12. The method according to one of the claims 1 to 6, further comprising:

forming a second oxide layer on the silicon layer and a mask layer on the second oxide layer;

patterning the second oxide layer and the mask layer to expose a first part of the silicon layer; and

subjecting the resulting structure to an anneal process thereby partially dissolving the part of the first silicon oxide layer beneath the exposed first part of the silicon layer in order to obtain a first thinned silicon oxide layer.

13. The method according to claim 12, further comprising

forming a third oxide layer and another mask layer on the exposed first part of the silicon layer;

patterning the third oxide layer and the other mask layer to expose a second part of the silicon layer; and

subjecting the resulting structure to another anneal process thereby partially dissolving the part of the first thinned silicon oxide layer beneath the exposed

second part of the silicon layer in order to obtain a second thinned silicon oxide layer.

14. The method according to claim 12, further comprising subsequently removing the patterned second oxide layer and mask layer and subsequently forming a further oxide layer and a nitride layer over the silicon layer and forming a shallow trench isolation between a first device area comprising the part of the silicon layer that was previously covered by the patterned second oxide layer and mask layer and a second device area comprising the previously exposed first part of the silicon layer and comprising the first thinned silicon oxide layer.

15. The method according to claim 12, 13 or 14, further comprising thermally oxidizing the exposed first part of the silicon layer, in particular, in an oxygen atmosphere, in particular, comprising O_2/H_2 or $O_2/H_2/HCl$ or O_2/HCl without or with dilution in N_2 or Ar or He ambient at a temperature of 800 °C to 1100 °C, thereby obtaining a thinned silicon layer.

Claims

1. Method for the manufacture of a multi-layer structure comprising the following steps:

providing a Silicon-On-Insulator, SOI, stack comprising a substrate layer, a first oxide layer on the substrate layer and a silicon layer on the first oxide layer (BOX layer);

forming at least one first region of the SOI stack wherein the silicon layer is thinned by thermally oxidizing a part of the silicon layer; and

forming at least one second region of the SOI stack wherein the first oxide layer (BOX layer) is thinned by annealing at a temperature of 900 °C to 1250 °C thereby partially dissolving the first oxide layer.

2. The method according to claim 1, wherein the steps of annealing and thermal oxidizing are performed in the same process chamber.

3. The method according to claim 2, wherein the annealing and thermal oxidizing are performed in a single continuous process step wherein the composition of the atmosphere in the process chamber and the temperature are modified according to anneal and oxidation conditions.

4. The method according to one of the preceding claims, wherein the at least one first region and the at least one second region at least partially overlap each other.

5. The method according to one of the claims 1 to 3, further comprising forming at least one shallow trench isolation in the SOI stack after performing the anneal or the oxidation to define a first and a second device area.

6. The method according to one of the claims 1 to 3, further comprising forming at least one shallow trench isolation in the SOI stack after performing the anneal and the oxidation to define a first and a second device area.

7. The method according to one of the claims 1 to 3, further comprising:

forming a second oxide layer on the silicon layer and a first mask layer on the second oxide layer;

patterning the second oxide layer and the first mask layer to expose a first part of the silicon layer; and

thermally oxidizing the exposed silicon layer to form a silicon oxide layer on the previously exposed silicon layer and a first thinned silicon layer.

8. The method according to claim 7, further comprising forming a second mask layer on a part of the silicon oxide layer and thermally oxidizing a part of the first thinned silicon layer located beneath the part of the silicon oxide layer that is not covered by the second mask layer thereby forming another silicon oxide layer and a second thinned silicon layer.

9. The method according to claim 7, further comprising subsequently forming a shallow trench isolation between a first device area comprising the part of the silicon layer not previously exposed by the patterned second oxide layer and first mask layer and a second device area comprising the first thinned silicon layer.

10. The method according to claim 8, further comprising subsequently forming a first shallow trench isolation between a first device area comprising the part of the silicon layer not previously exposed by the patterned second oxide layer and first mask layer and a second device area comprising the first thinned silicon layer and forming a second shallow trench isolation between the second

device area and a third device area comprising the second thinned silicon layer.

11. The method according to claim 7, further comprising removing the silicon oxide layer from the first thinned silicon layer and performing an anneal process, in an anneal ambient comprising Ar or N_2, thereby partially dissolving the part of the first oxide layer beneath the first thinned silicon layer in order to obtain a first thinned silicon oxide layer.

12. The method according to claim 8, further comprising removing the other silicon oxide layer from the second thinned silicon oxide layer and performing an anneal process, in particular, in an anneal ambient comprising Ar or N_2, thereby partially dissolving the part of the first oxide layer beneath the second thinned silicon layer in order to obtain a second thinned silicon oxide layer.

13. The method according to one of the claims 1 to 3, further comprising:

forming a second oxide layer on the silicon layer and a mask layer on the second oxide layer;

patterning the second oxide layer and the mask layer to expose a first part of the silicon layer; and

performing an anneal process thereby partially dissolving the part of the first silicon oxide layer beneath the exposed first part of the silicon layer in order to obtain a first thinned silicon oxide layer.

14. The method according to claim 13, further comprising

forming a third oxide layer and another mask layer on the exposed first part of the silicon layer;

patterning the third oxide layer and the other mask layer to expose a second part of the silicon layer; and

performing another anneal process thereby partially dissolving the part of the first thinned silicon oxide layer beneath the exposed second part of the silicon layer in order to obtain a second thinned silicon oxide layer.

15. The method according to claim 13, further comprising subsequently removing the patterned second oxide layer and mask layer and subsequently forming a further oxide layer and a nitride layer over the silicon layer and forming a shallow trench isolation between a first device area comprising the part of the silicon layer that was previously covered by the patterned second oxide layer and mask layer and a second device area comprising the previously exposed first part of the silicon layer and comprising the first thinned silicon oxide layer.

16. The method according to claim 13 , , further comprising thermally oxidizing the exposed first part of the silicon layer at a temperature of 800 °C to 1100 °C, thereby obtaining a thinned silicon layer.

17. The method according to claim 16, wherein the thermal oxidation is performed in an oxygen atmosphere comprising O_2/H_2 or $O_2/H_2/HCl$ or O_2/HCl.