

1 **VAN DER WAALS CAPACITOR AND QUBIT USING SAME**

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5 **[0001]** This invention was made with Government support. The Government has certain rights in the invention.

FIELD

10 **[0002]** One or more aspects of embodiments according to the present disclosure relate to capacitors, and more particularly to a capacitor for use in a quantum bit (qubit).

BACKGROUND

15 **[0003]** A transmission line shunted plasma oscillation qubit (transmon qubit) may be fabricated with one or two Jacobsen junctions and a capacitor connected in parallel with one or both Jacobsen junctions. In such a system, performance may be enhanced if the capacitor has relatively low loss. A capacitor design in which the electric field lines pass through (i) a substrate to air interface, (ii) a metal to air interface, or (iii) a substrate to metal interface may however exhibit significant loss as a result of imperfections or impurities at the interfaces.

20 **[0004]** It is with respect to this general technical environment that aspects of the present disclosure are related.

SUMMARY

25 **[0005]** According to an embodiment of the present disclosure, there is provided a capacitor, including: a first conductive layer; an insulating layer, on the first conductive layer; and a second conductive layer on the insulating layer, the first conductive layer being composed of one or more layers of a first van der Waals material, the insulating layer being composed of one or more layers of a second van der Waals material, and the second conductive layer being composed of one or more layers of a third van der
30 Waals material.

35 **[0006]** In some embodiments, the capacitor further includes: an insulating lower layer, under the first conductive layer; and an insulating upper layer, on the second conductive layer, wherein: the insulating lower layer being composed of one or more layers of a first van der Waals material, and the insulating upper layer being composed of one or more layers of a first van der Waals material.

[0007] In some embodiments, the capacitor further includes: a first layer of graphene, between the first conductive layer and the insulating layer; and a second layer of graphene, between the insulating layer and the second conductive layer.

- 1 **[0008]** In some embodiments, the first conductive layer is a superconducting layer and the second conductive layer is a superconducting layer.
- [0009]** In some embodiments, the first van der Waals material is a material selected from the group consisting of NbSe₂, MoTe₂, WTe₂, TaS₂, BSCCO, graphene, and combinations thereof.
- 5 **[0010]** In some embodiments, the third van der Waals material is the same material as the first van der Waals material.
- [0011]** In some embodiments, the second van der Waals material is a material selected from the group consisting of BN, WSe₂, MoS₂, MoSe₂, WS₂, MoTe₂, PtS₂, PtSe₂, PtTe₂, HfS₂, HfSe₂, ReS₂, ReSe₂, SnS₃, SnSe₂, ZrS₂, ZrSe₂, silicene, germanene, black phosphorus, and combinations thereof.
- 10 **[0012]** In some embodiments, the capacitor further includes: a first electrode, in contact with the first conductive layer, and a second electrode, in contact with the second conductive layer.
- 15 **[0013]** In some embodiments, the first electrode is composed of a superconducting material.
- [0014]** In some embodiments, the first electrode is composed of a material selected from the group consisting of aluminum, niobium, niobium nitride, niobium titanium nitride, titanium nitride, and molybdenum rhenium.
- 20 **[0015]** According to an embodiment of the present disclosure, there is provided a quantum bit, including: a capacitor according to claim 1, and a Josephson junction, connected to the capacitor.
- [0016]** In some embodiments, the quantum bit further includes: an insulating lower layer, under the first conductive layer; and an insulating upper layer, on the second conductive layer, wherein: the insulating lower layer being composed of one or more layers of a first van der Waals material, and the insulating upper layer being composed of one or more layers of a first van der Waals material.
- 25 **[0017]** In some embodiments, the quantum bit further includes: a first layer of graphene, between the first conductive layer and the insulating layer; and a second layer of graphene, between the insulating layer and the second conductive layer.
- 30 **[0018]** In some embodiments, the first conductive layer is a superconducting layer and the second conductive layer is a superconducting layer.
- [0019]** In some embodiments, the first van der Waals material is a material selected from the group consisting of NbSe₂, MoTe₂, WTe₂, TaS₂, BSCCO, graphene, and combinations thereof.
- 35 **[0020]** In some embodiments, the third van der Waals material is the same material as the first van der Waals material.

- 1 **[0021]** In some embodiments, the second van der Waals material is a material selected from the group consisting of BN, WSe₂, MoS₂, MoSe₂, WS₂, MoTe₂, PtS₂, PtSe₂, PtTe₂, HfS₂, HfSe₂, ReS₂, ReSe₂, SnS₃, SnSe₂, ZrS₂, ZrSe₂, silicene, germanene, black phosphorus, and combinations thereof.
- 5 **[0022]** In some embodiments, the quantum bit further includes: a first electrode, in contact with the first conductive layer, and a second electrode, in contact with the second conductive layer.
- [0023]** In some embodiments, the first electrode is composed of a superconducting material.
- 10 **[0024]** In some embodiments, the first electrode is composed of a material selected from the group consisting of aluminum, niobium, niobium nitride, niobium titanium nitride, titanium nitride, and molybdenum rhenium.

BRIEF DESCRIPTION OF THE DRAWINGS

- 15 **[0025]** Features, aspects, and embodiments are described in conjunction with the attached drawings, in which:
- [0026]** FIG. 1 is a schematic drawing of a qubit, according to an embodiment of the present disclosure;
- [0027]** FIG. 2 is a schematic drawing of a capacitor, according to an embodiment of the present disclosure;
- 20 **[0028]** FIG. 3 is a schematic drawing of a capacitor, according to an embodiment of the present disclosure;
- [0029]** FIG. 4A is a schematic drawing of test coupon, according to an embodiment of the present disclosure;
- 25 **[0030]** FIG. 4B is a schematic drawing of test coupon, according to an embodiment of the present disclosure;
- [0031]** FIG. 4C is a schematic drawing of test coupon, according to an embodiment of the present disclosure;
- [0032]** FIG. 4D is a schematic drawing of test coupon, according to an embodiment of the present disclosure;
- 30 **[0033]** FIG. 5 is a schematic diagram of a qubit, according to an embodiment of the present disclosure;
- [0034]** FIG. 6 is a schematic drawing of a capacitor, according to an embodiment of the present disclosure;
- 35 **[0035]** FIG. 7A is a photograph of a qubit circuit, according to an embodiment of the present disclosure; and
- [0036]** FIG. 7B is an enlarged view of a portion of FIG. 7A.

1 **DETAILED DESCRIPTION**

5 **[0037]** The detailed description set forth below in connection with the appended drawings is intended as a description of exemplary embodiments of a van der Waals capacitor and a qubit constructed with such a capacitor provided in accordance with the present disclosure and is not intended to represent the only forms in which some embodiments may be constructed or utilized. The description sets forth the features of the present disclosure in connection with the illustrated embodiments. It is to be understood, however, that the same or equivalent functions and structures may be accomplished by different embodiments that are also intended to be encompassed within the scope of the disclosure. As denoted elsewhere herein, like element numbers are intended to indicate like elements or features.

10 **[0038]** FIG. 1 shows a quantum bit, or “qubit”, in some embodiments. The quantum bit may be characterized by two quantum mechanical states, separated by an energy difference. A Josephson junction 105 is connected between a first metal (e.g. superconducting metal) pad 110 and a second metal (e.g. superconducting metal) pad 115. In operation, the first metal pad 110 and the second metal pad 115 form a capacitor connected in parallel with the Josephson junction 105. The structure may be fabricated on a substrate 120. Exemplary electric field lines 125, between a first charge on the first metal pad 110 and a second charge on the second metal pad 115, are shown. These field lines may cross (i) a substrate to air interface, (ii) a metal to air interface, and (iii) a substrate to metal interface, at one or more points. At these interfaces, impurities or other imperfections may give rise to two-level systems having respective energy differences similar to that of the qubit; these two-level systems may interact with the qubit, resulting in loss and a degradation in performance.

25 **[0039]** In some embodiments, a capacitor is instead formed as a stack of layers of van der Waals materials, as illustrated in FIG. 2. The capacitor includes a first conductive layer 205 on a substrate 210, an insulating layer 215, on the first conductive layer 205, and a second conductive layer 220 on the insulating layer 215. The first conductive layer 205 may be composed of one or more layers of a first van der Waals material, the insulating layer 215 may be composed of one or more layers of a second van der Waals material, and the second conductive layer 220 may be composed of one or more layers of a third van der Waals material. The third van der Waals material may be the same material as the first van der Waals material. Exemplary electric field lines 225 are shown. Except for fringing fields (not shown) each line of electric field extends directly from the second conductive layer 220 to the first conductive layer 205, passing through (i) a first interface between the second conductive layer 220 and the insulating layer 215 and (ii) a second interface between the first conductive layer 205 and the insulating layer 215. These interfaces may be significantly cleaner than the

1 substrate to air interface, the metal to air interface, and the substrate to metal interface
of the embodiment of FIG. 1. Although other interfaces (e.g., an air to substrate
interface) are present in the embodiment of FIG. 2, the coupling of the capacitor to
these interfaces may be relatively weak because only fringing fields may interact with
5 these interfaces. Moreover, the capacitor of the embodiment of FIG. 2 may be
significantly smaller (e.g., up to a factor of 1000 smaller) than the structure of FIG. 1.

[0040] The first conductive layer 205 and the second conductive layer 220 may be
superconducting layers, e.g., at sufficiently low temperature, current density, and
magnetic field, each of the first conductive layer 205 and the second conductive layer
10 220 may be in a superconducting state.

[0041] FIG. 3 shows a capacitor, in some embodiments. As in the embodiment of
FIG. 2, the capacitor includes a first conductive layer 305, an insulating layer 310 on
the first conductive layer 305, and a second conductive layer 315 on the insulating
layer 310. The capacitor of the embodiment of FIG. 3 further includes an insulating
15 lower layer 320 between the substrate (not shown) and the first conductive layer 305,
and an insulating upper layer 325 on the second conductive layer 315. The substrate
may be a wafer of high-purity silicon (e.g., flow-zone silicon). In the embodiment of
FIG. 3, the capacitor further includes a first electrode 330 and a second electrode 335,
each of which may be a superconducting (e.g. aluminum) electrode. As used herein,
20 a material or structure may be said to be “superconducting” if, at sufficiently low
temperature, current density, and magnetic field it will be in, or it will transition to,
a superconducting state. As used herein, this term (“superconducting”) also applies to
the structure or material when it is not in a superconducting state. As such, aluminum,
or an aluminum electrode, may be referred to as “superconducting”, even when it is at
25 at room temperature (and not in a superconducting state).

[0042] In some embodiments, the capacitor further includes a lower layer of
graphene 340, between the first conductive layer 305 and the insulating layer 310, and
an upper layer of graphene 345 between the insulating layer 310 and the second
conductive layer 315. The lower layer of graphene 340 and the upper layer of
30 graphene 345 may be superconducting layers as a result of being proximitized to the
first conductive layer 305 and to the second conductive layer 315 respectively. In some
embodiments, the lower layer of graphene 340 and the upper layer of graphene 345
are absent.

[0043] As in the embodiment of FIG. 2, each of (i) the first conductive layer 305,
35 the insulating layer 310, and the second conductive layer 315 may be composed of a
van der Waals material. For example, each of the first conductive layer 305 and the
second conductive layer 315 may be composed of niobium selenide (NbSe_2),
molybdenum telluride (MoTe_2), tungsten telluride (WTe_2), tantalum sulfide (TaS_2),

1 bismuth strontium calcium copper oxide (BSCCO), combinations (e.g., alloys) of these materials, or one of various thicknesses and twist angles of graphene. The insulating layer 310 may be composed of boron nitride (BN), tungsten selenide (WSe₂), molybdenum sulfide (MoS₂), MoSe₂, WS₂, MoTe₂, PtS₂, PtSe₂, PtTe₂, HfS₂, HfSe₂,
5 ReS₂, ReSe₂, SnS₃, SnSe₂, ZrS₂, ZrSe₂, silicene, germanene, or black phosphorus. In other embodiments, other suitable conducting (e.g., superconducting) or insulating materials may be used, respectively. In some embodiments, the insulating layer 310 includes fewer than 100 monolayers; the low thickness of this layer may result in a high capacitance per unit area of the capacitor. In some embodiments the insulating
10 layer 310 includes fewer than 10 (e.g., as few as one or two) monolayers; the thickness may be selected to be the smallest thickness for which the tunneling effect is negligible or acceptably small. In some embodiments, the insulating lower layer 320 and the insulating upper layer 325 may also be composed of a van der Waals material (e.g., BN, WSe₂, MoSe₂, or MoS₂).

15 **[0044]** FIGs. 4A – 4D show a portion of a process for fabricating electrodes in contact with a conducting layer. FIGs. 4A – 4D show, for ease of illustration, the process of forming electrodes 415 on a layer of niobium selenide 405 on a test coupon which initially includes only the layer of niobium selenide 405 on the substrate 410; in some embodiments an analogous process may be used to form electrodes that are in
20 contact with the first conductive layer 305 and with the second conductive layer 315 of a capacitor (e.g., the capacitor of FIG. 3 or the capacitor of FIG. 6 (discussed in further detail below)). A layer of niobium selenide 405 (e.g., niobium diselenide, NbSe₂) is deposited (e.g., on a substrate 410, as shown in FIG. 4A). The test coupon is then moved to an evaporating chamber for the forming of electrodes; during the
25 process of moving the test coupon, the outer surface of the layer of niobium selenide 405 may (as shown in FIG. 4B) become oxidized (e.g. covered with an oxide coating 412, shown in FIGs. 4B – 4D as a stippled surface) result of exposure to atmospheric oxygen. Ion milling may then be used, as shown in FIG. 4C, to remove a portion of the layer of niobium selenide 405, exposing unoxidized niobium selenide 405, and
30 electrodes 415 may be formed on the exposed unoxidized niobium selenide 405 as shown in FIG. 4D. FIG. 4D is a cutaway view showing the unoxidized niobium selenide below the layer of oxide, and in contact with the electrodes 415.

[0045] FIG. 5 shows a tunable frequency transmon qubit, which includes (i) a superconducting quantum interference device (SQUID) 505 including two Josephson
35 junctions 510 connected in a loop, and (ii) a capacitor 515 (e.g., the capacitor of FIG. 3 or the capacitor of FIG. 6 (discussed in further detail below)), connected in parallel with the SQUID 505. In some embodiments, a fixed frequency transmon qubit (having,

1 instead of the SQUID 505, a single Josephson junction 510, connected in parallel with the capacitor 515) may be constructed in an analogous manner.

5 **[0046]** FIG. 6 is a schematic drawing of a capacitor 515, in some embodiments. The capacitor 515 includes (like the capacitor of the embodiment of FIG. 3) a first conductive layer 305, an insulating layer 310, on the first conductive layer 305, and a second conductive layer 315 on the insulating layer 310. The capacitor further includes a first electrode 330 and a second electrode 335, in contact with the first conductive layer 305 and the second conductive layer 315, respectively. The capacitor of the embodiment of FIG. 6 lacks the insulating lower layer 320, the insulating upper layer 325, the lower layer of graphene 340, and the upper layer of graphene 345 that are shown for the capacitor of the embodiment of FIG. 3.

10 **[0047]** FIGs. 7A is a photograph of a reduction to practice, in one embodiment, of a qubit including a capacitor according to embodiments described herein. FIG. 7B is an enlarged view of a portion (labeled "7B") of FIG. 7A. The circuit may be fabricated on a silicon (e.g., float-zone silicon) substrate, or wafer. FIG. 7A shows three external connections to the qubit, which is illustrated in FIG. 7B. A first wire bond pad 705 is terminated to ground at a point adjacent to the qubit. A bias current supplied through the first wire bond pad 705 may be employed to produce a magnetic field at the qubit, to control the critical current of the SQUID loop of the qubit, and to control the frequency of the qubit. A second wire bond pad 710 may be capacitively coupled to the SQUID. Control pulses may be sent to the qubit via the second wire bond pad 710 to control the state of the qubit (e.g., to rotate the state of the qubit in the Bloch sphere). The third connection illustrated in FIG. 7A is a microwave resonator 715, which may be employed to read out the qubit. The microwave resonator 715 and the connections to the first wire bond pad 705 and to the second wire bond pad 710 may each be constructed as a coplanar microwave waveguide.

20 **[0048]** FIG. 7B shows, as mentioned above, an enlarged view of the qubit of FIG. 7A. The capacitor 730 includes a first conductive layer 305 (e.g., a layer of niobium diselenide), an insulating layer 310 (e.g., a layer of boron nitride (e.g., of hexagonal boron nitride)), and a second conductive layer 315 (e.g., a layer of niobium diselenide). The capacitance of the capacitor is largely determined by an area of overlap 735, within which each of the first conductive layer 305, the insulating layer 310, and the second conductive layer 315 is present. The capacitor is connected to a SQUID 505, the magnetic field in which may be controlled by adjusting the current flowing in a conductive segment 740 (which may be connected to the first wire bond pad 705 through a coplanar microwave waveguide).

35 **[0049]** The capacitor 730 of FIGs. 7A and 7B may be fabricated as follows. The first conductive layer 305 may be exfoliated from a niobium diselenide bulk crystal

1 using a suitable adhesive exfoliating tool, and transferred to the bare silicon substrate.
The insulating layer 310 may then be exfoliated from a boron nitride bulk crystal, and
placed in a position partially overlapping the first conductive layer 305 (and leaving a
portion of the first conductive layer 305 exposed), and the second conductive layer
5 315 may then be exfoliated from a niobium diselenide bulk crystal and placed on the
substrate, such that a portion of the second conductive layer 315 overlaps the region
in which the insulating layer 310 overlaps the first conductive layer 305. Electrodes
(e.g., aluminum electrodes) may then be fabricated to contact the first conductive layer
305 (e.g., the exposed portion of the first conductive layer 305) and the second
10 conductive layer 315.

[0050] The fabrication of the electrodes may include (i) forming a layer of
photoresist over the wafer, (ii) patterning the photoresist (e.g., using e-beam
lithography) to remove the photoresist in areas in which metal (e.g., aluminum) is to
be deposited, (iii) depositing a layer of metal (e.g., aluminum) over the wafer, and (iv)
15 removing the photoresist and the portions of the metal layer that are on photoresist,
using a lift-off process. The conductors forming the external connections (e.g., the first
wire bond pad 705, the second wire bond pad 710, the coplanar waveguides
connected to them, and the microwave resonator 715) may be formed at the same
time. Because the shapes of the exfoliated layers may be unpredictable (e.g., they
20 may vary from one exfoliation operation to another), the shape of the metal (e.g.,
aluminum) layer to be formed may be designed after the first conductive layer 305, the
insulating layer 310, and the second conductive layer 315 have been placed on the
substrate. The SQUID 505 may be fabricated before or after the capacitor.

[0051] As used herein, “a portion of” something means “at least some of” the thing,
25 and as such may mean less than all of, or all of, the thing. As such, “a portion of” a
thing includes the entire thing as a special case, i.e., the entire thing is an example of
a portion of the thing. As used herein, the word “or” is inclusive, so that, for example,
“A or B” means any one of (i) A, (ii) B, and (iii) A and B.

[0052] It will be understood that when a layer is referred to as being “between” two
30 layers, it can be the only layer between the two layers, or one or more intervening
layers may also be present. The terminology used herein is for the purpose of
describing particular embodiments only and is not intended to be limiting of the
inventive concept. As used herein, the terms “substantially,” “about,” and similar terms
are used as terms of approximation and not as terms of degree, and are intended to
35 account for the inherent deviations in measured or calculated values that would be
recognized by those of ordinary skill in the art.

[0053] As used herein, the term “major component” refers to a component that is
present in a composition, polymer, or product in an amount greater than an amount of

1 any other single component in the composition or product. In contrast, the term
"primary component" refers to a component that makes up at least 50% by weight or
more of the composition, polymer, or product. As used herein, the term "major portion",
when applied to a plurality of items, means at least half of the items. As used herein,
5 any structure or layer that is described as being "made of" or "composed of" a
substance should be understood (i) in some embodiments, to contain that substance
as the primary component or (ii) in some embodiments, to contain that substance as
the major component. It will be understood that when an element or layer is referred
to as being "on", "connected to", "coupled to", or "adjacent to" another element or layer,
10 it may be directly on, connected to, coupled to, or adjacent to the other element or
layer, or one or more intervening elements or layers may be present. In contrast, when
an element or layer is referred to as being "directly on", "directly connected to", "directly
coupled to", or "immediately adjacent to" another element or layer, there are no
intervening elements or layers present.

15 **[0054]** It will be understood that when an element is referred to as being "directly
connected" or "directly coupled" to another element, there are no intervening elements
present. As used herein, "generally connected" means connected by an electrical path
that may contain arbitrary intervening elements, including intervening elements the
presence of which qualitatively changes the behavior of the circuit. As used herein,
20 "connected" means (i) "directly connected" or (ii) connected with intervening elements,
the intervening elements being ones (e.g., low-value resistors or inductors, or short
sections of transmission line) that do not qualitatively affect the behavior of the circuit.

[0055] Although limited embodiments of a van der Waals capacitor and a qubit
constructed with such a capacitor have been specifically described and illustrated
25 herein, many modifications and variations will be apparent to those skilled in the art.
Accordingly, it is to be understood that a van der Waals capacitor and a qubit
constructed with such a capacitor employed according to principles of this disclosure
may be embodied other than as specifically described herein. Features of some
embodiments are also defined in the following claims, and equivalents thereof.

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1 **WHAT IS CLAIMED IS:**

1. A capacitor, comprising:
a first conductive layer;
5 an insulating layer, on the first conductive layer; and
a second conductive layer on the insulating layer,
the first conductive layer being composed of one or more layers of a first van
der Waals material,
the insulating layer being composed of one or more layers of a second van
10 der Waals material, and
the second conductive layer being composed of one or more layers of a third
van der Waals material.

2. The capacitor of claim 1, further comprising:
15 an insulating lower layer, under the first conductive layer; and
an insulating upper layer, on the second conductive layer,
wherein:
the insulating lower layer being composed of one or more layers of a
first van der Waals material, and
20 the insulating upper layer being composed of one or more layers of a
first van der Waals material.

3. The capacitor of any of claims 1-2, further comprising:
a first layer of graphene, between the first conductive layer and the insulating
25 layer; and
a second layer of graphene, between the insulating layer and the second
conductive layer.

4. The capacitor of any of claims 1-3, wherein the first conductive layer is
30 a superconducting layer and the second conductive layer is a superconducting layer.

5. The capacitor of any of claims 1-4, wherein the first van der Waals
material is a material selected from the group consisting of NbSe₂, MoTe₂, WTe₂,
TaS₂, BSCCO, graphene, and combinations thereof.

35 6. The capacitor of any of claims 1-5, wherein the third van der Waals
material is the same material as the first van der Waals material.

- 1 7. The capacitor of any of claims 1-6, wherein the second van der Waals
material is a material selected from the group consisting of BN, WSe₂, MoS₂, MoSe₂,
WS₂, MoTe₂, PtS₂, PtSe₂, PtTe₂, HfS₂, HfSe₂, ReS₂, ReSe₂, SnS₃, SnSe₂, ZrS₂,
ZrSe₂, silicene, germanene, black phosphorus, and combinations thereof.
- 5 8. The capacitor of any of claims 1-7, further comprising:
a first electrode, in contact with the first conductive layer, and
a second electrode, in contact with the second conductive layer.
- 10 9. The capacitor of claim 8, wherein the first electrode is composed of a
superconducting material.
- 15 10. The capacitor of claim 9, wherein the first electrode is composed of a
material selected from the group consisting of aluminum, niobium, niobium nitride,
niobium titanium nitride, titanium nitride, and molybdenum rhenium.
- 20 11. A quantum bit, comprising:
a capacitor according to claim 1, and
a Josephson junction, connected to the capacitor.
- 25 12. The quantum bit of claim 11, further comprising:
an insulating lower layer, under the first conductive layer; and
an insulating upper layer, on the second conductive layer,
wherein:
the insulating lower layer being composed of one or more layers of a
first van der Waals material, and
the insulating upper layer being composed of one or more layers of a
first van der Waals material.
- 30 13. The quantum bit of any of claims 11-12, further comprising:
a first layer of graphene, between the first conductive layer and the insulating
layer; and
a second layer of graphene, between the insulating layer and the second
conductive layer.
- 35 14. The quantum bit of any of claims 11-12, wherein the first conductive
layer is a superconducting layer and the second conductive layer is a
superconducting layer.

1 15. The quantum bit of any of claims 11-12, wherein the first van der Waals material is a material selected from the group consisting of NbSe₂, MoTe₂, WTe₂, TaS₂, BSCCO, graphene, and combinations thereof.

5 16. The quantum bit of any of claims 11-12, wherein the third van der Waals material is the same material as the first van der Waals material.

 17. The quantum bit of any of claims 11-12, wherein the second van der Waals material is a material selected from the group consisting of BN, WSe₂, MoS₂,
10 MoSe₂, WS₂, MoTe₂, PtS₂, PtSe₂, PtTe₂, HfS₂, HfSe₂, ReS₂, ReSe₂, SnS₃, SnSe₂, ZrS₂, ZrSe₂, silicene, germanene, black phosphorus, and combinations thereof.

 18. The quantum bit of any of claims 11-12, further comprising:
 a first electrode, in contact with the first conductive layer, and
15 a second electrode, in contact with the second conductive layer.

 19. The quantum bit of claim 18, wherein the first electrode is composed of a superconducting material.

20 20. The quantum bit of claim 19, wherein the first electrode is composed of a material selected from the group consisting of aluminum, niobium, niobium nitride, niobium titanium nitride, titanium nitride, and molybdenum rhenium.

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