ABSTRACT

A METHOD OF STACKING THIN SUBSTRATES BY TRANSFER BONDING

This invention describes a method of stacking, bonding, and electrically interconnecting a plurality of thin integrated circuit wafers to form an interconnected stack of integrated circuit layers. The first integrated circuit layer is formed by conventional processing on a silicon wafer to the stage where bond pads are patterned on a wiring layer interconnecting the subjacent semiconductive devices. The remaining integrated circuit layers are formed by first processing a standard wafer to form integrated circuit devices and wiring levels up to but not including bond pads. Each of these wafers is mounted onto a handler wafer by its upper face with a sacrificial bonding agent. The wafer is thinned, permanently fastened to the top surface of the first base wafer by a non-conductive adhesive applied to the thinned under face, and dismounted from the handler. Vertical openings are etched through the thinned layer to the bond pads on the subjacent wafer. Robust conductive pass-through plugs with integrated upper bond pads are formed in the openings. Additional thinned integrated circuit layers may be prepared, thinned, cemented onto the stack. Wiring interconnections can be made between any two or more layers. The process is unique in that it can be used to further stack and interconnect any number of thinned wafer layers to form a three dimensional integrated circuits, including MEMS devices. This approach provides a low temperature wafer bonding method using an adhesive which results in process simplicity and cost effectiveness by eliminating an additional masking and patterning process for under bump metal thereby enabling standard wafers to be integrated into a 3D stack with existing wire bonded wafers.

Fig. 13