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(54) IMPROVEMENTS IN OR RELATING TO INTEGRATED CIRCUIT DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor integrated circuit devices in which there are a plurality of circuit cells in a single chip of semiconductor material.

It is well known to provide an integrated circuit array with associated circuits which intersect one another. Such circuit intersections are termed "crossovers" or "crossunders" depending upon whether at the circuit intersection one circuit bridges over or tunnels under the other circuit. For convenience the invention will be described with reference to circuit crossunders.

Crossunder electrical impedance is significant and can have a substantial effect on signal transmission and thus on circuit access time. Circuit access time is of considerable importance in a circuit, such as a memory, that is repeatedly accessed. Time delays in gaining access to such a circuit constitute a delay in the system in which the circuit is used, and their cumulative effect can be a serious disadvantage.

In some circuit designs for coincident access integrated circuits crossunders have been provided on primarily one of several types of access circuits for purposes of chip layout simplicity. The different signal rise times that result on different access circuits are allowed for by adapting the operation of the device to the worst rise time. In semiconductor memories such an approach results in row circuits, for example, suffering the bulk of the crossunders with the

result that signal rise time at a remote end of a row circuit is much longer than the rise time for similar column circuit signals, and the memory cycle time is correspondingly extended. Other circuit designs more nearly equalise the crossunder loading between row and column circuits but in doing so use large numbers of crossunders evenly distributed along the circuits so that both row and column circuits have similar long signal rise times.

According to this invention an integrated circuit device comprises a chip of semiconductor material having a plurality of circuit cells therein arranged in rows and columns, a plurality of row conductive paths and a plurality of column conductive paths arranged in intersecting array, each of said paths including low impedance and higher impedance conductive sections, and each of said paths having a first portion to which a first plurality of said cells is connected and which does not include a said higher impedance conductive section, and a second portion to which a second plurality of said cells is connected and which includes at least one said higher impedance conductive section where it crosses another path or paths without electrical contact therewith.

Preferably each of said paths has an access point, and said first portion of each of said paths is electrically closer to said access point than is said second portion thereof.

Preferably, each said second portion has the same number of said higher impedance conductive sections.

Considering said cells to be grouped in four different quadrants, each of said paths may extend through two of said quadrants with its said first and second portions being connected respectively to the cells of the first and second ones of its two quadrants, the cells in each quadrant being connected to said first portion of a row or column path

and to said second portion of a column or row path respectively.

Each said low impedance conductive section may be a metal conductor deposited on a face of said device, and each said higher impedance conductive section may comprise a portion of said semiconductor material of higher conductivity than the surrounding material and extending through said material under at least one intersecting path.

The said row paths may extend in pairs and said column paths may extend in pairs between rows and columns of said cells respectively, each path of a said pair being connected to a different row or column of cells as the case may be.

The device may include means connected to each of said cells, said means comprising a plurality of further conductive paths each extending in physical parallel relation with said first portion of a different one of said row or column paths, and circuit buses connecting said further conductive paths together.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram of a bistable or flip-flop memory cell circuit;

Fig. 2 is a simplified schematic diagram of an arrangement of principal interconnecting circuits for a plurality of memory cells in a semiconductor chip;

Fig. 2A shows in cross-section a circuit crossunder of Fig. 2;

Figs. 3A, 3B, and 3C are equivalent circuit diagrams; and

Fig. 4 shows schematically a memory cell layout for the cell of Fig. 1 in the chip of Fig. 2.

Referring now to Fig. 1, two field effect transistors 11 and 12, preferably of the P-channel insulated gate field effect type having different selected gain levels to facilitate operation as a memory cell, are cross-coupled drain-to-gate. Source electrodes of the transistors are connected to the positive terminal of a potential source 13 whose negative terminal is connected to ground. Drain electrodes of transistors 11 and 12 are connected to flip-flop circuit output terminals 16 and 17, respectively, and to the source electrodes of two additional transistors 18 and 19 which are arranged to operate as load resistors in the flip-flop circuit. The drain electrodes of the latter two transistors are connected together and to ground at a terminal 20. Gate electrodes of the same load transistors are connected together and to a negative potential source 22 at a terminal 21.

Access is attained by the coincident application of voltage signals on an X circuit 23 and a Y circuit 26. The latter signals are

preferably driven from a positive level toward ground to enable conduction in a pair of X-gate transistors 27 and 28 and a pair of Y-gate transistors 29 and 30, respectively. When such enabling signals are applied in coincidence, conduction can take place in either direction between the output terminal 16 and a Bit circuit 31 and be-

tween the output terminal 17 and a Bit circuit 32. Double-rail logic signals are applied from a digit drive source, not shown,

by way of the Bit and Bit circuits to drive the flip-flop circuit into one of its stable states in accordance with the digit signals. Similarly, during memory readout the binary state of information stored in cell 10 and represented by different voltage levels at output terminals 16 and 17 is coupled through the gate transistors and the same Bit

and Bit circuits to a digit detector, not shown.

During standby operation of the cell, holding current flows from the source 13 through the bistable circuit to ground to maintain a particular stable state. During readout some of the cell current which flows from source 13 through the conducting one of the transistors 11 or 12 is diverted through gate transistors to one of the Bit or

Bit circuits and the digit detector to reach the ground return path for the source 13. Likewise during writing operations current is applied by way of the digit circuits and gate transistors through one or the other of the load transistors 18 or 19 to develop appropriate potential differences at terminals 16 and 17 for forcing the desired stable state upon the flip-flop circuit.

Fig. 2 is a simplified schematic diagram of the layout of 64 memory cells of the type shown in Fig. 1 in a common semiconductor substrate 33 which may be interconnected with others, not shown, on a common ceramic substrate, also not shown. Cells are arranged in cell groups having a predetermined ratio of numbers of cells per group and a predetermined group configuration. In a presently preferred embodiment the chip is divided into quadrants, each containing the same number of cells and having the same number of crossunders, of approximately the same impedance each, in control circuits for supplying enabling signals to the cells.

Each cell 10 from Fig. 1 is represented by a different square in Fig. 2. The schematic diagram is shown on the face of the substrate in order to facilitate an understanding of the invention, and one form of actual circuit and device relationships for a cell is shown in, and will be described

subsequently in connection with, Fig. 4. Each cell in Fig. 2 is served by power connections, the X and Y access circuit connections for enabling cell operation, and a pair of digit circuit connections in the manner indicated in Fig. 1. The X, Y and digit circuit connections are shown for several cells in the upper left-hand corner of substrate 33, but other such connections are not shown to preserve the simplicity of the drawing. Power connections are only partially shown in Fig. 2.

Broken lines, such as line 36, extending through different parts of the substrate represent schematically the path followed within a diffusion layer in the chip to provide a ground bus connection for the various cells. This bus does not appear at the surface of the chip since it connects directly within the diffusion layer to the drain electrode diffusion for transistors 18 and 19 of each cell. An external connection for this ground bus to the power supply is shown at the left-hand side of chip 33, but one or more such connections can be provided at any convenient points around the chip. The positive connection is shown at the lower edge of chip 33 but it can be made to the substrate 33 at any convenient point along the chip perimeter. Within the chip the source electrode diffusions of each of the transistors 11 and 12 are connected to the substrate at each cell. The negative supply connection for the gate electrodes of transistors 18 and 19 in each cell is by way of a metallic circuit on the surface of the substrate generally following over the path of the ground bus diffusion but it is not shown in Fig. 2 since the arrangement thereof on the substrate does not critically affect the invention. As the negative supply circuit simply provides a continuous voltage slightly below ground to the terminals 21 in all of the cells and otherwise carries no significant current, it may be formed to include crossunders for any intersecting circuits wherever appropriate.

It is known in the art that diffused conduction paths can be formed in a semiconductor chip for various circuit purposes including power buses and circuit crossunder structures. Such paths are doped to display a substantially higher conductivity than the surrounding semiconductor material but they have a significantly lower conductivity than a metallic circuit material such as gold or aluminium. Circuit crossunder structures in the chip of Fig. 2 include a diffused conduction path extending under, and insulated from a circuit in an intersecting circuit location. Electrical connection is made at the ends of the diffused conduction path to the parts of a metallic circuit that are to be included with the crossunder in series in a circuit path.

Such a crossunder is shown in simplified form in Fig. 2A where circuits 24 and 25 intersect and the latter includes in series a diffused path 34 extending through semiconductor material 35 and under insulating material 44 and conductor 24. Although insulated circuit crossings are usually schematically indicated by crossed lines, half loops or jumps, such as the half loop 45 in the upper left portion of Fig. 2, are utilised herein to indicate most circuit crossunders to make it clear which of two or more intersecting circuits includes the crossunder impedance.

A single basic memory cell configuration is utilised throughout the chip of Fig. 2 and it will be seen that adjacent pairs of cells along any row within a chip quadrant are the mirror image of one another, while adjacent pairs of cells along any column within a quadrant are similarly the mirror image of one another. In the embodiment of Fig. 2 it will be seen that diagonally opposed quadrants are similarly oriented versions of the same cell arrangement, while the adjacent quadrant portions likewise comprise the same cell quadrant arrangement but rotated 90 degrees in the plane of the drawing. Although the cells are for convenience shown in Figs. 1 and 2 as being separate from the X, Y and digit circuits, it will be shown in connection with Fig. 4 that segments of the latter circuits are likewise included in the cell arrangement which is rotated in one direction or another to provide the full chip array of cells. This cell uniformity facilitates chip layout under the control of computer-aided design techniques which are now known in the art.

The completed chip array in Fig. 2 includes X circuits which are metal circuits deposited on the face of the chip and traverse the full two-quadrant width of the chip in pairs of circuits extending between adjacent rows of cells with each circuit of a pair serving a different one of the adjacent rows. Each X circuit is free of crossunders to accommodate Y circuits and digit circuits in half of its extent and includes crossunders for those circuits in the other half. The half which is free of such crossunders is all metallic and is in the chip quadrant adjacent to its access or driving point. The portion of the circuit which includes the crossunders is in the chip quadrant remote from the access or driving point.

Thus the X circuits X1 and X2 extend across the substrate 33 between the two upper rows of cells and are driven at the left-hand side of the substrate adjacent to the upper left quadrant of the chip. These X circuits in the latter quadrant include crossunders for only a digit circuit bus at the left-hand side of the quadrant. In the

upper right-hand quadrant of the chip the same X circuits include crossunders for both digit circuits and Y circuits. Circuits X3 and X4 are similarly arranged to extend through the two upper quadrants of the chip and to be driven from the left-hand side. In a similar fashion X circuits X5 and X6 extend between the fifth and sixth rows of cells and are driven at the right-hand side of the chip adjacent to the lower right quadrant where they are essentially free of crossunders. Likewise the X circuits X7 and X8 extend between the two bottom rows of the chip in a fashion similar to the circuits X5 and X6. The column circuits of the memory are arranged in a fashion similar to that just described for the X circuits with the Y circuits Y1 to Y4 being driven at the lower edge of the lower left quadrant of the chip and Y5 to Y8 being driven adjacent to the upper edge of the upper right quadrant.

Digit circuits for the chip are conveniently considered in terms of digit lines which serve sets of memory cells, digit buses which interconnect digit lines for respective quadrants of the chip, and digit terminals for making external digit bus connections for the chip. All of the digit circuits are metallic except for short connective diffused portions at each cell as will be noted in connection with Fig. 4. Digit lines such as lines 37 and 38 extend between adjacent rows of cells in chip quadrants adjacent to X row circuits in the upper left, and similarly in the lower right, quadrants in Fig. 2. Digit lines such as lines 40 and 41 extend between adjacent columns of cells in the upper right, and similarly in the lower left, quadrants where Y column circuits are driven. These digit circuits are arranged

in Bit and Bit pairs which lie between pairs of X or Y circuits serving the same memory cells. Each cell is connected to both a Bit

line and a Bit line as shown in Fig. 1. Although the latter connections are illustrated in Fig. 2 as crossing different numbers of circuits, the crossunders are in fact approximately the same since in the actual layout, the outer, or Y-gate transistors 29 and 30 are preferably located between the digit lines of a pair at each cell location, as will be shown in Fig. 4.

Within any particular quadrant the Bit and Bit digit lines enter the quadrant from opposite sides respectively, and corresponding lines of the same type within the quadrant are bussed together. Thus, in

Fig. 2 Bit lines, such as the line 38, enter the upper left quadrant of the chip from the right-hand side and are on that side con-

nected by a bus 42 to a Bit terminal 43. Similarly, Bit lines such as the line 37 in the same quadrant enter from the left-hand side and are connected by a bus 46 to a Bit terminal 47. The buses of the same type are further interconnected so that each cell on the chip has access to the Bit terminals 43 and 47 as well as to a corresponding pair of Bit terminals 48 and 49 at the diagonally opposite corner of the chip. This arrangement permits digit circuits for several chips to be connected in series.

Terminals 47 and 49 are connected together by way of Bit bus 46 in the upper left quadrant, a Bit line 50 and a Bit bus 51 in the lower left quadrant, and a connection 52 in the lower right quadrant. Also arranged as a branch on the same connection between Bit terminals is the series combination of a Bit bus 53 serving the lower right quadrant and a Bit bus 56 serving the upper right quadrant. In a

similar manner Bit terminals 43 and 48 are

interconnected by a connection 57, Bit bus

58, Bit line 59, and Bit bus 60, all of which cooperate with a branch connection includ-

ing the Bit bus 42 serving the upper left

quadrant and a Bit bus 61 serving the lower left quadrant.

A chip circuit has a characteristic impedance including series resistance and shunt distributed capacitance to the surrounding circuit elements. An ideal equivalent circuit would be as shown in Fig. 3A where a shunt capacitor 62 represents the capacitance lumped near the driving point and a series resistor 63 connected to the load. Upon application of a voltage at the driving point, the capacitor 62 is rapidly charged through a circuit portion of extremely low time constant to build up an output voltage rapidly for application through resistor 63 to the load. This ideal circuit is not actually attainable in a chip row or column control circuit because of the distributed character of the impedance, but, if it were, it would provide the least signal rise time delay.

Fig. 3B is the equivalent circuit for the distributed impedance in a chip circuit of a type not otherwise shown in the drawing, where crossunders are included all along the circuit. Each crossunder includes a certain amount of shunt distributed capacitance, which is relatively small, and significant series resistance which is attributable to the fact that the semiconductor material included in the crossunder diffusion has a much higher resistance than does a corres-

ponding length of the metallic portion of the circuit. In Fig. 3B a series resistor 66 and a shunt capacitor 67 represent an initial circuit crossunder to accommodate a digit circuit bus and are followed by a plurality of similar sections, each including a resistor 68 and a capacitor 69 representing subsequent crossunders at each intersecting circuit. Metallic circuit part distributed capacitance is included in capacitors 67 and 69. It is apparent that a signal applied at the circuit driving point will have an extended rise time because the capacitances of successive sections of the iterative network must be sequentially charged.

Fig. 3C is an approximate equivalent circuit of an X or Y circuit of Fig. 2. The equivalent circuit includes an input resistor 66 and a capacitor 67¹ representing the initial crossunder impedance to accommodate a digit circuit bus, as in the case of Fig. 3B. However, this combination is followed by a capacitor 70 which represents the dominant distributed capacitance of the X or Y control circuit quadrant portion which is otherwise free of crossunders. The capacitor 70 is followed by an iterative network including a plurality of resistor-capacitor sections each including a resistor 68¹ and a capacitor 69¹ each section representing a crossunder. However, the total resistive effect is reduced as compared with what it might otherwise be because each crossunder accommodates a plurality of circuits, i.e. a pair of X or Y circuits and two digit circuits. Thus, the total length of diffused portions passing under intersecting circuits is held to a practical minimum. Accordingly, the individual control circuit arrangement of Fig. 2, as represented by the equivalent circuit of Fig. 3C, provides a better signal rise time. The dominant portion of the distributed capacitance is that represented by the crossunder-free metallic circuit portion lumped adjacent to the circuit drive point where it can be charged through the smallest possible impedance, i.e. that represented by a single crossunder. Likewise the ladder effect of the part of distributed impedance including the resistances in all the other crossunders is confined to the circuit portion remote from the driving point and is distributed among both X and Y circuits so that signal rise time delay for either type of circuit is reduced.

Fig. 4 depicts an actual integrated circuit layout on a semiconductor chip for a memory cell of the type shown in Fig. 1. Because an integrated circuit is really a three-dimensional complex of conductors and active devices, Fig. 4 employs a schematic notation that is often utilised in the art to represent three-dimensional features in a two-dimensional drawing. Three levels of interest are shown in Fig. 4. These are

a diffusion level wherein the conductive portions are outlined by relatively broad solid lines, a channel level wherein the conductive channels of insulated gate field effect transistors are outlined by relatively narrow solid lines, and surface metalisation wherein bands of metallic conductor deposited on the face of the chip are outlined by broken lines. In actual practice many of the broken lines representing the metalised conductors would be directly over lines representing diffused semiconductor regions, and in most cases where this occurs the broken lines have been slightly displaced in order that they may be separately perceived. Connections between the diffusion layer and metalised surface conductors are accomplished in a manner similar to that shown for conductor 25 in Fig. 2A. Thus, holes are etched through an insulating layer which otherwise covers the entire surface of the semiconductor material, including diffused regions. Conductor metal thereafter deposited on the insulating layer extends through the holes to contact the semiconductor material. Such contact posts extending through insulation holes are represented by pairs of concentric rectangles. The transistors in Fig. 4 are identified by underlined reference characters which are the same as the reference characters utilised in Fig. 1 and which are located in the channel region for the transistor. Otherwise, reference characters employed in Fig. 4 correspond to those utilised in other figures of the drawing.

Bit circuit 32 and Bit circuit 31 in Fig. 4 are the two metal bands extending transversely across the upper portion of the figure above and below two dual transistors which include the Y-gate transistors 29 and 30. It was previously noted in connection with Fig. 2 that the Y-gate transistors of the cells were located on the chip between

the Bit and Bit lines. Thus, the dual transistors in Fig. 4 each include a different Y-gate transistor for a different memory cell. Two contact posts 71 and 72 connect the Bit

and Bit lines 31 and 32 to the diffusion level where diffused conductive paths connect the paths to electrodes of transistors 29 and 30, respectively. Above each of these transistors in the drawing is another transistor which comprises the Y-gate transistor of an additional memory cell above the one shown in the drawing. Thus, for example, the cell shown in Fig. 4 would correspond to the cell in Fig. 2 which is second from the left in the second row of cells from the top of the figure. The conduction paths for transistors 29 and 30 extend through their respective channels to additional diffused conductors 73 and 76 which provide connec-

tions to electrodes of the X-gate transistors 27 and 28, respectively.

Overlying the transistors 29 and 30 is a metal conductor 77 with enlarged portions 77a and 77b that comprise both the gate electrodes and connections thereto for transistors 29 and 30 and which are further connected through a contact post 78 to a Y-conductor crossunder 26a. Similar enlarged portions in the X conductor 23 provide gate electrodes and connections thereto for X-gate transistors 27 and 28.

The last-mentioned transistors have diffused electrode portions which are connected through further diffused conductors 16¹ and 17¹, corresponding to flip-flop output terminals 16 and 17, to source electrodes of flip-flop load transistors 18 and 19, respectively, and to drain electrodes of the flip-flop transistors 11 and 12, respectively. Metalised band 21¹ corresponds to terminal 21 in Fig. 1 for interconnected gate electrodes of load transistors 18 and 19 as an extension of the negative bus system for the chip. The latter system includes extensions 22¹ at the central left-hand portion of Fig. 4 for providing negative voltage to cells to the left of that illustrated in Fig. 4 and a pair of similar downward extensions from the bottom of Fig. 4 to cells below that shown in Fig. 4. Drain electrodes of the load transistors 18 and 19 are connected through diffused conductors to the ground diffusion bus 20¹ extending across the bottom of Fig. 4.

Flip-flop transistors 11 and 12 have their drain electrodes connected into the diffused conductors 16¹ and 17¹, respectively. Source electrodes of those transistors are connected through diffused conductors 13¹ to a post 79 that extends over both the diffused conductor 13¹ and the common substrate, not shown, where the connection to positive potential source 13 (shown in Fig. 1) is made. A contact post 80 provides the cross-coupling connection from the metalised gate electrode of transistor 11 to the diffused drain electrode of transistor 12 included in conductor 17¹. Similarly, a contact post 81 provides the crosscoupling connection from the drain electrode of transistor 11 to the gate of transistor 12. It will also be seen that additional transistors 11a and 12a are connected in respect to all electrodes in parallel with transistors 11 and 12, respectively. These additional transistors 11a and 12a may be considered disjoint parts of transistors 11 and 12, respectively, and are consequently not separately shown in Fig. 1. They have been provided in Fig. 4 as separate entities solely for the purpose of utilising chip space efficiently.

The Y circuit 26 which serves the cell of Fig. 4 extends up the left side of the figure and includes a metal lower portion which

is then coupled through a contact post 82 to the diffused conductor portion 26a which passes under the aforementioned negative bus 22¹, the X conductor 23, Bit line 31, post 78 for connection to conductor 77, and

Bit line 32.

If the cell representation of Fig. 4 is rotated 90 degrees in a clockwise direction in the plane of the drawing, it will be seen then to correspond to cells located in the lower left and upper right quadrants of the chip as illustrated in Fig. 2. However, in this new orientation the circuits that were designated Y circuits must now be designated as X circuits and vice versa. Such an orientation interchanges the X—Y gate functions of the transistor pairs 27, 28 and 29, 30, but the interchange is immaterial since the gate transistors are utilised for a coincidence function and no operative coupling is established unless all four transistors are enabled.

WHAT WE CLAIM IS:—

1. An integrated circuit device comprising a chip of semiconductor material having a plurality of circuit cells therein arranged in rows and columns, a plurality of row conductive paths and a plurality of column conductive paths arranged in intersecting array, each of said paths including low impedance and higher impedance conductive sections, and each of said paths having a first portion to which a first plurality of said cells is connected and which does not include a said higher impedance conductive section, and a second portion to which a second plurality of said cells is connected and which includes at least one said higher impedance conductive section where it crosses another path or paths without electrical contact therewith.

2. A device as claimed in claim 1 wherein each of said paths has an access point, and said first portion of each of said paths is electrically closer to said access point than is said second portion thereof.

3. A device as claimed in claim 1 or 2 wherein each said second portion has the same number of said higher impedance conductive sections.

4. A device as claimed in any one preceding claim wherein, considering said cells to be grouped in four different quadrants, each of said paths extends through two of said quadrants with its said first and second portions being connected respectively to the cells of the first and second ones of its two quadrants, and the cells in each quadrant are connected to said first portion of a row or column path and to said second portion of a column or row path respectively.

5. A device as claimed in any one preceding claim wherein each said low im-



tions to electrodes of the X-gate transistors 27 and 28, respectively.

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Bit line 32.

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2. A device as claimed in claim 1 wherein each of said paths has an access point, and said first portion of each of said paths is electrically closer to said access point than is said second portion thereof.

3. A device as claimed in claim 1 or 2 wherein each said second portion has the same number of said higher impedance conductive sections.

4. A device as claimed in any one preceding claim wherein, considering said cells to be grouped in four different quadrants, each of said paths extends through two of said quadrants with its said first and second portions being connected respectively to the cells of the first and second ones of its two quadrants, and the cells in each quadrant are connected to said first portion of a row or column path and to said second portion of a column or row path respectively.

5. A device as claimed in any one preceding claim wherein each said low im-

pedance conductive section is a metal conductor deposited on a face of said device, and each said higher impedance conductive section comprises a portion of said semiconductor material of higher conductivity than the surrounding material and extending through said material under at least one intersecting path.

6. A device as claimed in any one preceding claim wherein said row paths extend in pairs and said column paths extend in pairs between rows and columns of said cells respectively, and each path of a said pair is connected to a different row or column of cells, as the case may be.

7. A device as claimed in any one preceding claim including means connected to each of said cells, said means comprising a plurality of further conductive paths each

extending in physical parallel relation with said first portion of a different one of said row or column paths, and circuit buses connecting said further conductive paths together.

8. A device as claimed in any one preceding claim wherein each of said cells is a flip-flop circuit.

9. An integrated circuit device substantially as herein described with reference to Figs. 1, 2, 2A, 3C and 4 of the accompanying drawings.

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