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IPOS

INTEGRATED CIRCUIT WIRING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to wiring systems for integrated circuits (IC) and, more particularly, to wiring systems which facilitate engineering changes for the following functions: electrical characterization; diagnostic testing; and circuit modifications for repair or evaluation. These functions may hereinafter be collectively referred to as Engineering Changes or EC's.

2. Description of the Prior Art

The formation of integrated circuit chips in accordance with different technologies has been known for a number of years. A demand for increased complexity of electronic systems including such integrated circuits has caused the development of techniques for wiring modification and repair of such IC chips.

The IC multi-layer construction is similar to multi-layer circuit boards in that wiring can be run in a direction parallel to the surface at the interface between any two dielectric layers. Wiring can be run perpendicular to the surface and between wiring layers with through-holes or "vias" in the layers which are selectively filled with conductive materials. Multi-layer wiring and modules have been implemented with a variety of technologies including multi-layered co-fired ceramics, silicon based thin film structures, ceramic based thin film structures and

combinations of those techniques.

However, because of the multi-layer construction, there is no ready access to wiring other than on the surface of the multi-layer structure. Therefore, engineering changes cannot readily be made.

Perhaps of equal importance is the fact that while electronic modules are large relative to the chips they contain, they are often very complex and of fairly small overall dimensions. Therefore, they are subject to connector or conductor defects in the same manner as the chips to be mounted thereon and so manufacturing yields of the multi-layer structure must also be considered. The length of the conductors is quite substantial because complex wiring metallization must be provided to allow each output terminal of one chip to be connected to a plurality of other input terminals on other chips. Additionally, so-called fanout wiring is often provided to interface between the fine wiring patterns characteristic of the connector spacing of the chips and the relatively more coarse wiring patterns on multi-chip modules (MCM). The problem of circuit defects is aggravated by the manufacturing processes used to create the multi-layer structures, which are difficult to characterize, diagnose, or effect repairs.

Since such structures are complex and require a number of processing steps for each layer, substantial expense is involved in fabrication of the multi-layer structure. It is therefore economically important that the multi-layer module be repairable. It is similarly important that diagnostics

are conducted, design changes are possible, or circuit repairs are possible on IC's to ensure corrective masks used in the IC fabrication are effective. In the past, this has been accomplished on modules by a process known as ECing or the implementing of engineering changes, which required providing one or more layers of redistribution wiring from the I/O pads to EC pads on the top surface. However, these layers of redistribution wiring are also subject to the same potential defects as other wiring layers and are not repairable. Further, such patterns of redistribution wiring are in close proximity to each other, requiring high line (e.g., wiring patterns) quality, and, parasitic capacitance will exist causing signal delays, reduced noise margins and other effects, thereby posing a severe restriction on wiring design rules. Additionally, in order to facilitate engineering changes for the following functions: electrical characterization; diagnostic testing; and circuit modifications for repair or evaluation, a significant amount of product and process complexity is required. This function also traditionally requires additional area for the redistribution wiring and EC pads, thus limiting the maximum possible density of the wiring.

Within the individual IC chip, the complexity of the problem is further complicated because electrical access to internal circuit nodes must be accomplished on an extremely small scale. However, such access to an integrated circuit is often necessary in order to characterize the electrical behavior of the node, electrically stimulate the node, or to establish continuity between the node and some other circuit node or access point for EC purposes. These exercises are

done in failure analysis, characterization, and design debug environments to address business needs.

The need to electrically establish continuity between the node of interest and a pad, test point, or circuit node that is substantially distant is increasing. This is often driven by the need to bring out a node of interest to a location where it is not obstructed by the packaging, probe equipment, or other chip surface features for characterization purposes. Additionally, the rerouting of circuit nets for engineering changes may require substantial lengths of wiring between nodes to be linked.

The EC's of internal circuit nodes for initial design verification/debug or failure analysis has been addressed in the past by opening an access point to the circuit node of interest with blanket delayering, localized delayering or focused-ion-beam (FIB) milling techniques, the optional depositions of a conductive pad or line using FIB, laser chemical vapor deposition (LCVD), or conventional IC processing techniques, and possibly followed with the probing of the exposed node or deposited pad using contact probing or electron-beam probing approaches.

An early approach to electrically access internal nodes involved using lithography techniques in a laboratory setting to pattern a mask used to define regions where holes would be etched down to the circuit nodes of interest. Subsequent to this preparation of the chip, mechanical probes were used to make contact to the exposed circuit nodes. In time, electron-beam probes were used for the

interrogation or stimulation of these nodes; e.g., voltage contrast and electron beam induced current techniques. This approach worked well for devices patterned with up to two levels of wiring and where the input/output pads to the device were located around the perimeter of the chip leaving most of the chip circuitry exposed even when probe cards were used to electrically stimulate the chip circuitry.

As additional levels of wiring were added to integrated circuit designs, the former technique of etching holes to the underlying circuit nodes lost its effectiveness due to poor aspect ratios of the etched holes. FIB approaches offered the high aspect ratio feature needed and are currently widely used to access circuit nodes. Additionally, many circuit designers have brought key circuit nodes up to test points at the upper levels of wiring in their initial hardware designs to facilitate the electrical access to these nodes.

FIB techniques are also widely used today for circuit modifications for engineering changes which are incorporated herein by reference to the article entitled "Design Guidelines for FIB Modifiability and a Case Study of High Performance SCSI Chip with Timing Problems" by S. X. Li et al, published in the Proceedings of the 20th International Symposium for Testing and Failure Analysis, 13-18 November 1994. However, this approach is limited to placement of spare metal lines. FIB deposited lines contain a very high impurity concentration (e.g., carbon) and for typical line widths, lengths exceeding 50 microns may pose a problem due to high resistance (typically around 500 milliohms per

square). Long FIB deposited lines also require a lengthy deposition time. A current practice to address this problem is to use an LCVD metal deposition technique to deposit the bulk of the line segment along with shorter elements of FIB deposited lines to complete the net. Additionally, semiconductor manufacturers are designing in spare wires at the upper levels of metal for the potential future use for circuit modifications.

The various approaches used in the past have a number of disadvantages; namely:

1. Wires must be placed (manually or through some sort of automated "fill" tool) during the design layout phase;
2. If left floating, the spare wires are susceptible to electrostatic charging problems;
3. Random placement of the spare wires makes it difficult for an analyst to locate them, especially if a stud via technology is used eliminating any features that would distinguish the spare wires from functional wires; and,
4. Such wires have no function unless used for a circuit change.
5. No facility is offered for external electrical access through chip pads to internal circuit nodes, for characterization and diagnostics purposes.

An example of prior art module wiring schemes which allow some degree of repairs and engineering changes to be made is described in U.S. Pat. No. 4,489,364 to Chance et al which shows an electronic circuit module in which connections to pads to which chips are connected are buried within the body

of the multi-layer structure but are periodically brought to the surface of the module and linked by EC pads of a so-called "dog-bone" shape. Continuity of these connections may be broken by severing the narrow portion of the dog-bone and EC connections may be made thereto either with or without severing the original connection. However, if a defect occurs in or between the C4 pad and the first EC pad, no repair is possible and the module must be discarded. The wiring through via holes is particularly vulnerable to the occurrence of discontinuities, as well, which may or may not be repairable and, in any event, repair would require point-to-point wiring over a considerable distance, further increasing parasitic impedance of the overall wiring system. It can also be readily appreciated that the length of wiring involved in this scheme, including the repeated vertical traversals of the multi-layer structure through vias, is large and has a large lumped capacitance.

Additionally, U.S. Pat. No. 4,746,815 to Bhatia et al provides a switching circuit within the module to allow sharing of EC pads between received and driver circuits. U.S. Pat. No. 4,453,176 to Chance et al shows wiring to capacitances buried within the multi-layer structure. U.S. Pat. No. 4,840,924 to Kinbara shows a particular structure for the dog-bone EC pads. U.S. Pat. No. 4,254,445 to Ho shows a staggered chip location arrangement for a large number of chips in a module to minimize potential wiring crossovers and maximize the number of EC pads which can be provided. U.S. Patent 4,549,200 to Ecker et al shows a repairable multi-level overlay system using redistribution. U.S. Pat. No. 4,546,413 to Feinberg et al shows a module

structure in which EC pads are provided on both major surfaces of the multi-layer structure. U.S. Pat. No. 4,706,165 to Takenaka et al shows a multi-layer structure in which connections to module connection pins are made through vias to EC pads at the upper surface of the module to increase the types of engineering changes and repairs which can be made. U.S. Pat. No. 5,155,577 to Chance et al shows a connection matrix between terminals of IC carrier and EC pads. U.S. Pat. No. 5,243,140 to Bhatia et al shows a wiring system on the top surface of a multiple chip module which includes a redistribution layer. U.S. Pat. No. 5,508,938 to Wheeler shows special interconnect layer employing offset trace layout for advanced multi-chip module packages using conventional EC approach. U.S. Pat. No. 5,214,250 to Cayson et al shows a method of reworking circuit panels which can overlay encapsulated replacement lines one on top of another.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a system for engineering changes (EC), that is, to facilitate the following: electrical characterization; diagnostic testing; and circuit modifications for repair or evaluation.

It is another object of the present invention to provide a wiring distribution to characterize, diagnose or change IC functionality using multipurpose conductive stripes which may be incorporated into the IC design.

It is a further object of the present invention to provide

the ability to route EC wires or stripes around chip surfaces or crossing other EC wires or stripes.

It is another further object of the present invention to provide access to a characterization node at a location not obstructed by I/O interconnect circuitry, packaging, or probe apparatus used to interface with the IC chip.

In order to satisfy the above and other objects of the present invention, a novel structure is provided for wiring layouts of an IC chip that includes conductive stripes that can be directed at a later time to link up with internal circuit nodes. The conductive stripes serve a functional utility in the as-designed device yet also allow the IC chip operation to be retained even after they are redirected for engineering changes. Optionally provided are pads and test points that can be directed to desired circuit nodes using the aforementioned EC wires, and interrogated or stimulated using standard test interfaces and programs.

In accordance with another aspect of the invention, a method for electrical characterization, failure analysis or for circuit modifications, is provided by allowing access to internal IC chip nodes.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is plan view of the present invention showing a first and second level of wiring;
FIG. 2 is another plan view of the invention showing details of FIG. 1 wiring; and
FIG. 3 is another plan view of the invention showing further details of FIG. 1 and FIG. 2 wiring.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to the drawings, and more particularly to FIG. 1, a plan view of a portion of a wiring or interconnect layer in an integrated circuit is shown. This layer may be included at any level above the substrate on which semiconductor devices or elements are constructed. Preferably, the conducting or interconnect level of this invention would be applied near the uppermost level(s) of the integrated circuit for ease of access from the outside of the chip. Further, these levels may also be used for distribution of power or signals to the semiconductor elements or device as will be more fully explained hereinafter.

It is well known in the semiconductor field that wiring layers may be constructed in various wiring patterns of electrically conductive material such as copper or aluminum formed therein and thereon to connect or to provide power to various devices embedded in or mounted on the semiconductor substrate. FIG. 1 shows a portion of the two uppermost wiring distribution grid or networks 11 and 12, which could be at two different points or voltage levels (V_{dd} and

ground), placed on a semiconductor substrate (not shown). Each grid includes parallel rails 13 and 14 which are connected to and extend from a peripheral base conductor 15 and 16. Another layer of wiring distribution grids includes rails 21 and 22 is shown in relief on a second level or layer immediately below the uppermost layer. The rails 21 and 22 are analogous to the rails 13 and 14. It should now be evident that additional layers below these two layers may also be included in the semiconductor integrated circuits. The two layers may be electrically interconnected using vias or other conductive paths at points 17 and 18. With this understanding, our discussion will now focus on the uppermost wiring distribution grid which may be used to conduct and distribute power or signals to the semiconductor circuits in a conventional manner on the substrate below.

Referring now to FIGS. 1, 2 and 3, narrow stripes 23 and 24 are positioned parallel to and spaced from the rails 13 and 14. The spacing between the stripes and rails will depend on a number of factors including the process used to create the semiconductor devices and the voltages or signal carried by the wiring and parasitic constraints. For voltage or power distribution purposes the stripes are also connected to the base conductor 15 and 16. For signal or power distribution purposes, they may also be connected to the rails 13 and 14 and optionally by shunts 28. The stripes 23 and 24 are constructed such that they may be separated from the rails or the base conductor by breaking away a small portion or portions 31 of the stripe at appropriate locations along the stripe 23 or other areas such as

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immediately adjacent to the base conductor and removal of the optional shunts 28. It should be understood that other geometric wiring arrangements may be employed as long as the stripes and/or rails are kept electrically in parallel.

In FIG. 1, additional test points 33 may also be attached to the narrow stripes 23 and 24 in order to provide ease of access for testing selected semiconductor elements. If wider or more robust connections are required, a pad 34 may be associated and electrically connected to the stripe 23. Stripe 23 may then be severed in areas 36 and 31 to separate the rail leaving the stripe attached to pad 34 as shown in FIG. 3. Accordingly, these pads, and isolated stripes, or test points, may be later strapped into the internal circuit using FIB or laser CVD.

Conventional techniques such as FIB or LCVD may now be used to connect these isolated stripes 35 optionally containing pads 34 or test points 33 to internal circuit nodes as shown in FIG. 3. Internal circuit nodes may be accessed by a deposited connection 42 to an existing probe point 40 or by using conventional FIB techniques to access buried nodes at 40. Another embodiment would be to use electrically alterable lines at the points where the stripes 23 and 24 join the rails 15 and 16. The electrically alterable links might be fuse elements, or switches controlled by SRAM, or even latches in a scan chain.

It is contemplated that the wiring patterns described may be used in conjunction with any other conventional etching,

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milling, and line deposition techniques including focused-ion-beam (FIB) approaches or LCVD. These conventional techniques are used with the aforementioned stripe segments, test points, and pads to effect access to internal circuit nodes. In fact, combinations of conventional techniques may be used such as:

--Milling or etching a hole to a circuit net of interest in order to gain access to the node. Similarly, various Stripes 23 and 24 may be accessed;

--Severing an internal circuit net in order to establish two circuit nodes. In a similar manner, the stripes 23 and 24 and any shunts 28 may be isolated from the rails 13 and 14 or base conductors 15 and 16; or

--Depositing a wire to a circuit node or stripe segment that traverses up through the milled opening and along the surface of the IC to some other location on the chip.

Using the foregoing techniques with any combination of stripe segments from any number of levels from which the stripes are available may be used to establish a new wire across a wide expanse of the chip.

Anyone skilled in the art with conventional FIB practices can appreciate the various techniques for milling and deposition of conductors and dielectrics to accomplish the operations described above.

Many other methodologies are also available to perform the engineering changes in IC's using the conventional techniques described above in conjunction with the present invention. These changes may include establishing access to an internal circuit node through a test point or chip pad for electrical characterization purposes, making circuit diagnostic tests, or modifications and repairs. This methodology has several advantages over previous methods that did not have the circuit wiring of the present invention such as:

--Long low resistance stripes are available for long excursions across the chip offering the best conductive characteristics at minimal size which would reduce the analyst's tool set since any need for depositing low resistance lines such as with LCVD deposition tools is reduced or eliminated.

--Engineering change wires may now cross over each other using stripes on differing planes while formerly dielectric insulators were needed at such intersections of engineering change wires placed on the IC surface.

--Obstacles on the chip surface such as pads and fuse block openings may be more readily averted using the embedded stripes.

--The wiring may be used to re-direct existing pads for characterization or engineering changes requiring access through conventional pad probers or through the IC module packaging.

--The wiring may be used to strategically place test points that can be linked to any internal circuit net on the chip. This might be used to provide test point access that is not obstructed by probe apparatus used to interface with the pads of the chip.

--The wiring minimizes the chip area needed for designed-in wire structures and in the preferred embodiment, offers a ready means for the analyst to identify the stripes since they are a derivative of the power distribution network.

The derivation of spare wires from a power distribution network is particularly advantageous for application specific IC because the network is often fixed for most parts using any given master image. Therefore, the design overhead, although minimal, is spread over all parts fabricated in that master image. Memory parts might take advantage of power, data, or work select lines (depending upon the layout approach) that already traverse significant expanses of the cell arrays. The custom and semi-custom environments in which microprocessors, controllers, and specials are fabricated in may utilize a combination of power and signal distributions to derive the re-routable stripes. Since any parallel stripe scheme adds capacitance, it is far more desirable to target power rails over signal lines.

Although the invention has been described in detail herein with reference to its preferred embodiment, it is to be understood that this description is by way of example only, and is not to be construed in a limiting sense. It is to be

further understood that numerous changes in the details of the embodiments of the invention, and additional embodiments of the invention, will be apparent to, and may be made by, persons of ordinary skill in the art having reference to this description. It is contemplated that such changes and additional embodiments are within the spirit and true scope of the invention as claimed below.

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CLAIMS

1. A distribution wiring system for a semiconductor substrate having a number of semiconductor devices forming integrated circuits comprising:

   a conducting rail which is connected to a peripheral base conductor said rail interconnects with the semiconductor devices; and

   a conducting stripe parallel to and separable from said rails for providing connections to said semiconductor devices whereby engineering changes may be accomplished.

2. A wiring system as recited in Claim 1 which includes a plurality of rails that are arranged in parallel to each other and a plurality of stripes.

3. A wiring system as recited in Claim 2 wherein said rails provide power to said semiconductor devices.

4. A wiring system as recited in Claim 2 wherein said rails provide signals to said semiconductor devices.

5. A wiring system as recited in Claim 3 which includes shunts connected to and between said rails and stripes which may be removed.

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6. A wiring system as recited in Claim 2 which includes test points attached to said stripes which may be used to facilitate electrical access to the semiconductor devices.

7. A wiring system as recited in Claim 2 which includes pads attached to said stripes which may be used to facilitate electrical access to the semiconductor circuits.

8. A wiring system as recited in Claim 2 which includes electrically alterable links to interconnect the rails to the stripes.

9. A distribution wiring system for a semiconductor substrate having a number of semiconductor devices forming integrated circuits comprising:

a conducting rail which carries signals and interconnects with the semiconductor devices; and

a conducting stripe which is electrically in parallel to and separable from said rail for providing connections to said semiconductor devices whereby engineering changes may be accomplished.

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10. A method of performing engineering changes to a semiconductor integrated circuit having a plurality of devices arranged on a substrate which are interconnected by a plurality of parallel conducting rails comprising the steps of:

providing parallel conducting stripes having test pads or test points which are electrically connected to the rails;

severing the stripes from the rails anywhere required;

connecting the severed stripe to certain devices; and

making engineering changes to the IC.

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