CLAIMS

1. A semiconductor device comprising:

a first circuit comprising a first transistor and a second transistor one of a source and a drain of which is electrically connected to a gate of the first transistor; and

a second circuit comprising a third transistor and a fourth transistor one of a source and a drain of which is electrically connected to a gate of the third transistor,

wherein a gate of the second transistor is electrically connected to a gate of the fourth transistor,

wherein a first signal is supplied to the gate of the second transistor and the gate of the fourth transistor,

wherein a second signal is supplied to the other of the source and the drain of the second transistor,

wherein a third signal is supplied to the other of the source and the drain of the fourth transistor,

wherein an amplitude of the first signal is larger than an amplitude of the second signal and an amplitude of the third signal, and

wherein when one of the second signal and the third signal is high, the other of the second signal and the third signal is low.

2. The semiconductor device according to claim 1, further comprising a circuit configured to generate the first signal.

3. The semiconductor device according to claim 1, wherein a high-level potential of the first signal is higher than a high-level potential of the second signal and a high-level potential of the third signal.

4. The semiconductor device according to claim 1, wherein a low-level potential of the first signal is lower than a low-level potential of the second signal and a low-level potential of the third signal.

5. The semiconductor device according to claim 1, wherein each of the second transistor and the fourth transistor comprises a channel formation region in an oxide semiconductor film.

6. The semiconductor device according to claim 5, wherein the oxide semiconductor film comprises indium, gallium, and zinc.

7. A semiconductor device comprising:

a first circuit comprising a first transistor and a second transistor one of a source and a drain of which is electrically connected to a gate of the first transistor;

a second circuit comprising a third transistor and a fourth transistor one of a source and a drain of which is electrically connected to a gate of the third transistor; and

a third circuit configured to generate a first signal which is supplied to a gate of the second transistor and a gate of the fourth transistor,

wherein a second signal is supplied to the other of the source and the drain of the second transistor,

wherein a third signal is supplied to the other of the source and the drain of the fourth transistor,

wherein the first signal comprises a pulse signal,

wherein an amplitude of the pulse signal is larger than an amplitude of the second signal and an amplitude of the third signal, and

wherein when one of the second signal and the third signal is high, the other of the second signal and the third signal is low.

8. The semiconductor device according to claim 7, wherein a high-level potential of the pulse signal is higher than a high-level potential of the second signal and a high-level potential of the third signal.

9. The semiconductor device according to claim 7, wherein a low-level potential of the pulse signal is lower than a low-level potential of the second signal and a low-level potential of the third signal.

10. The semiconductor device according to claim 7, wherein each of the second transistor and the fourth transistor comprises a channel formation region in an oxide semiconductor film.

11. The semiconductor device according to claim 10, wherein the oxide semiconductor film comprises indium, gallium, and zinc.

12. The semiconductor device according to claim 1, wherein the semiconductor device is configured so that a high-level potential of the first signal is set higher than a high-level potential of the second signal by a threshold voltage of the second transistor.

13. The semiconductor device according to claim 7, wherein the semiconductor device is configured so that a high-level potential of the pulse signal is set higher than a high-level potential of the second signal by a threshold voltage of the second transistor, and

wherein the semiconductor device is configured so that a high-level potential of the pulse signal is set higher than a high-level potential of the third signal by a threshold voltage of the fourth transistor.

14. A semiconductor device comprising:

a programmable logic device comprising a switch circuit comprising:

a first transistor; and

a second transistor comprising a channel formation region in an oxide semiconductor film,

wherein a first signal is supplied to a gate of the second transistor,

wherein a second signal is supplied to one of a source and a drain of the second transistor,

wherein a gate of the first transistor is electrically connected to the other of the source and the drain of the second transistor,

wherein an amplitude of the first signal is larger than an amplitude of the second signal.

15. The semiconductor device according to claim 14, further comprising a circuit configured to generate the first signal.

16. The semiconductor device according to claim 14, wherein a high-level potential of the first signal is higher than a high-level potential of the second signal.

17. The semiconductor device according to claim 14, wherein the semiconductor device is configured so that a high-level potential of the first signal is set higher than a high-level potential of the second signal by a threshold voltage of the second transistor.

18. The semiconductor device according to claim 14, wherein the oxide semiconductor film comprises indium, gallium, and zinc.

19. The semiconductor device according to claim 1, wherein the first signal comprises a pulse signal.

20. The semiconductor device according to claim 14, wherein the first signal comprises a pulse signal.