

FIG. 1

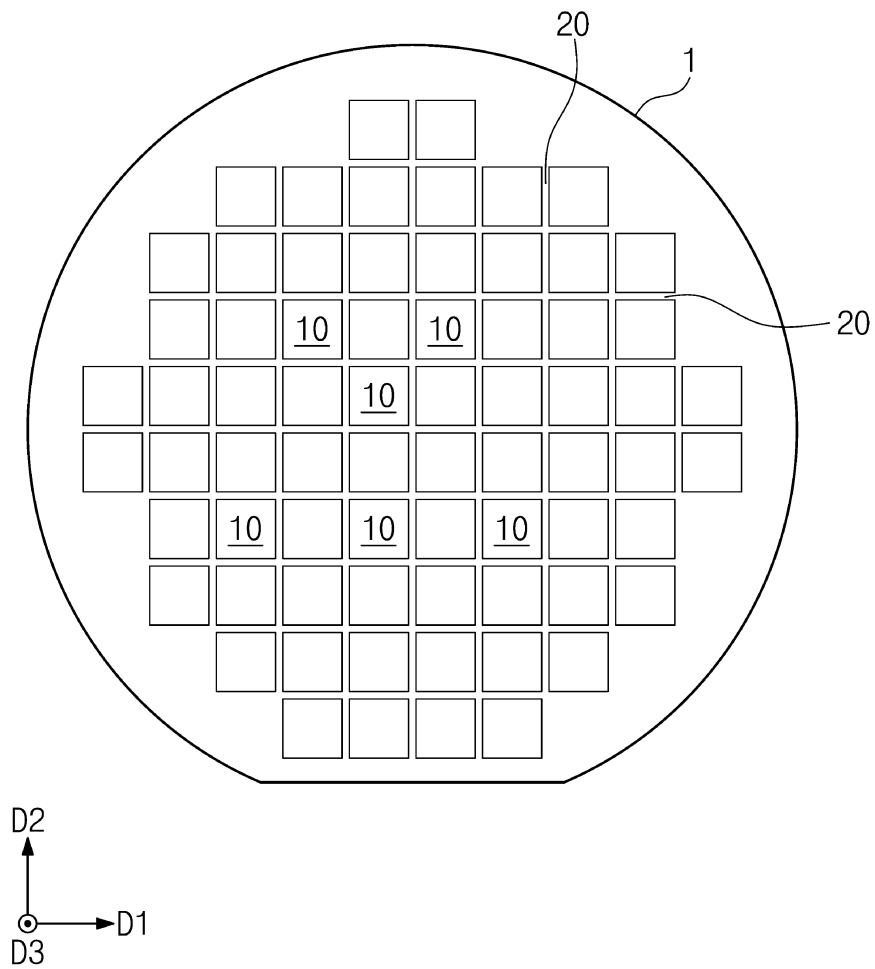


FIG. 2

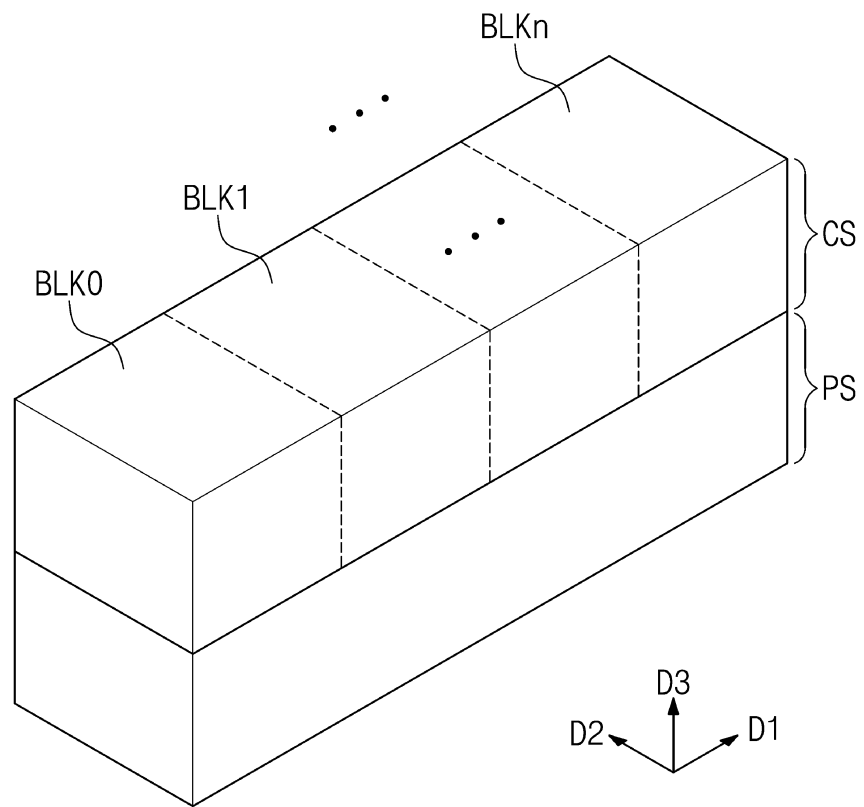


FIG. 3

10

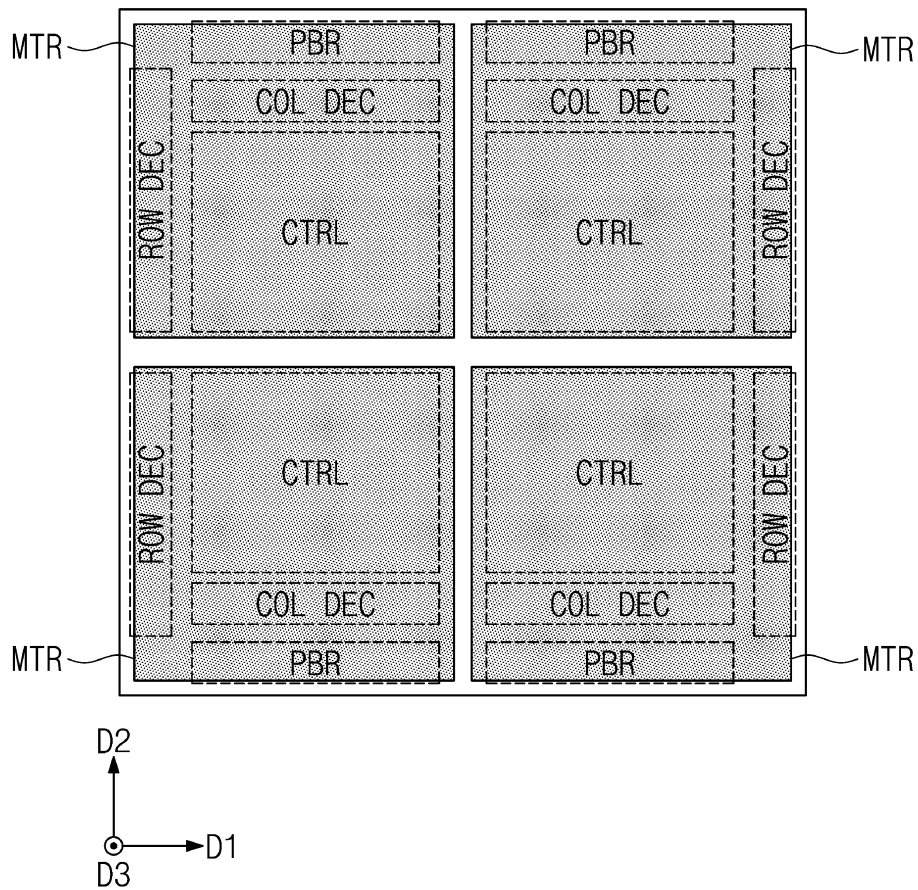


FIG. 4A

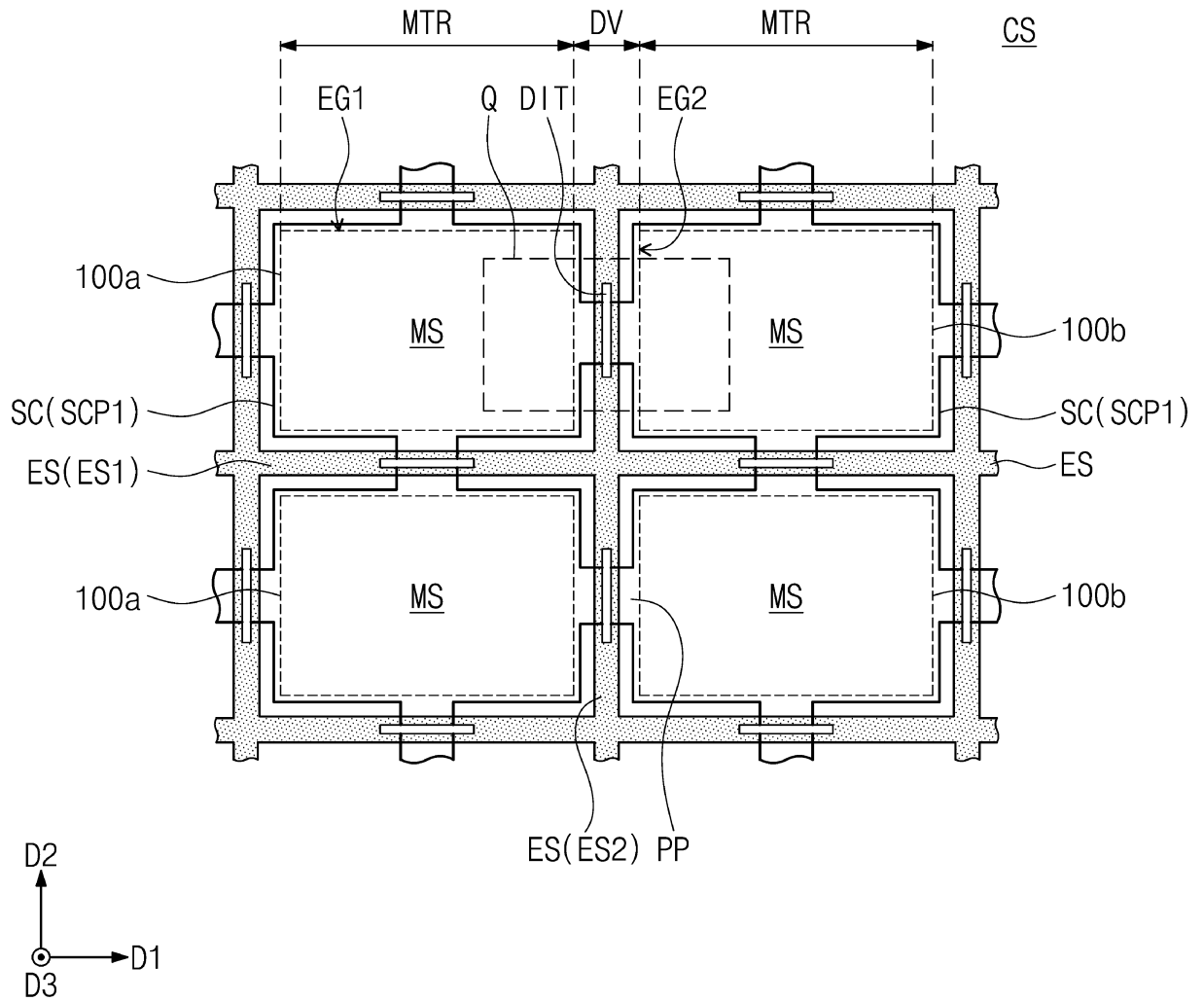


FIG. 4B

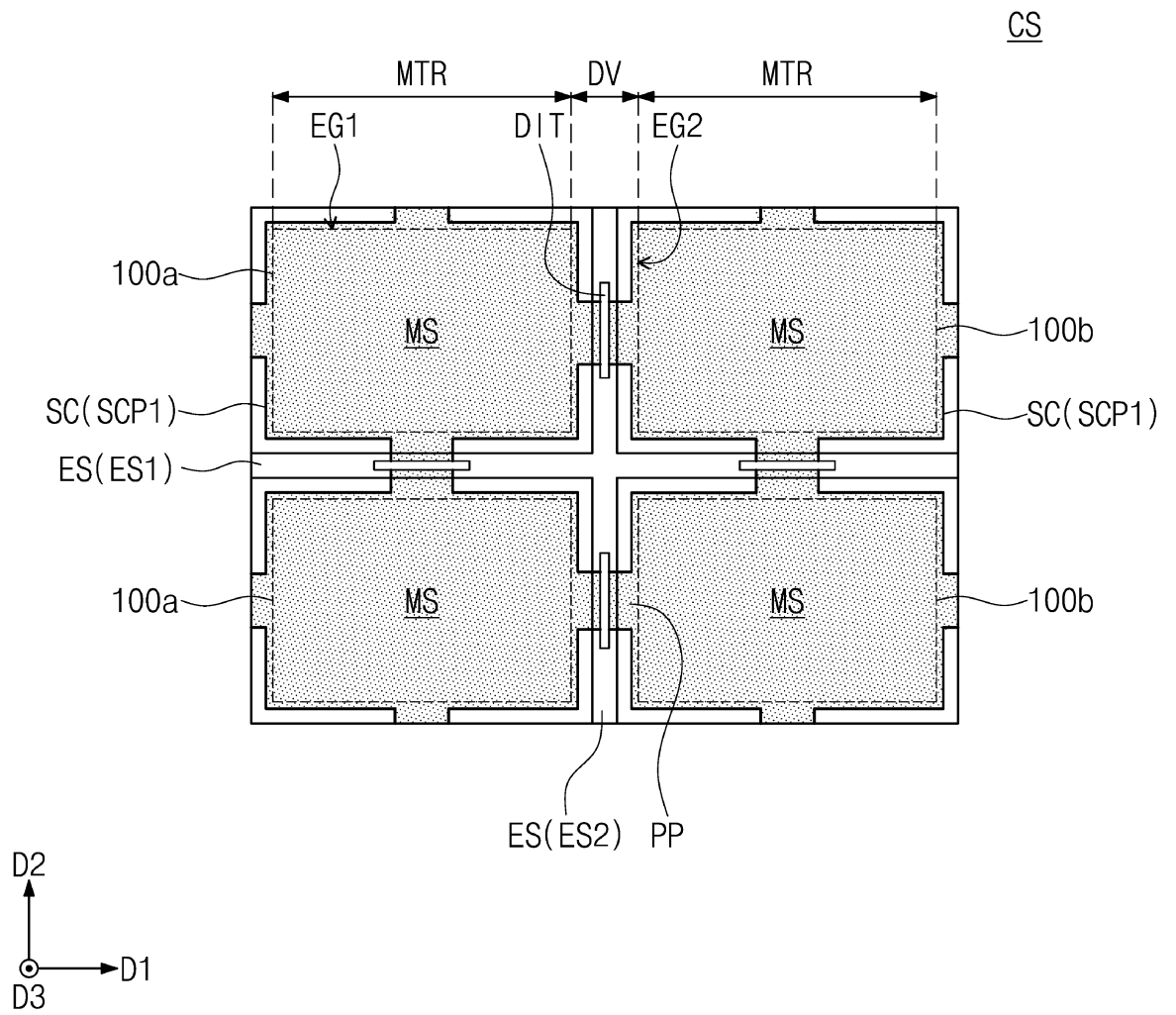


FIG. 5

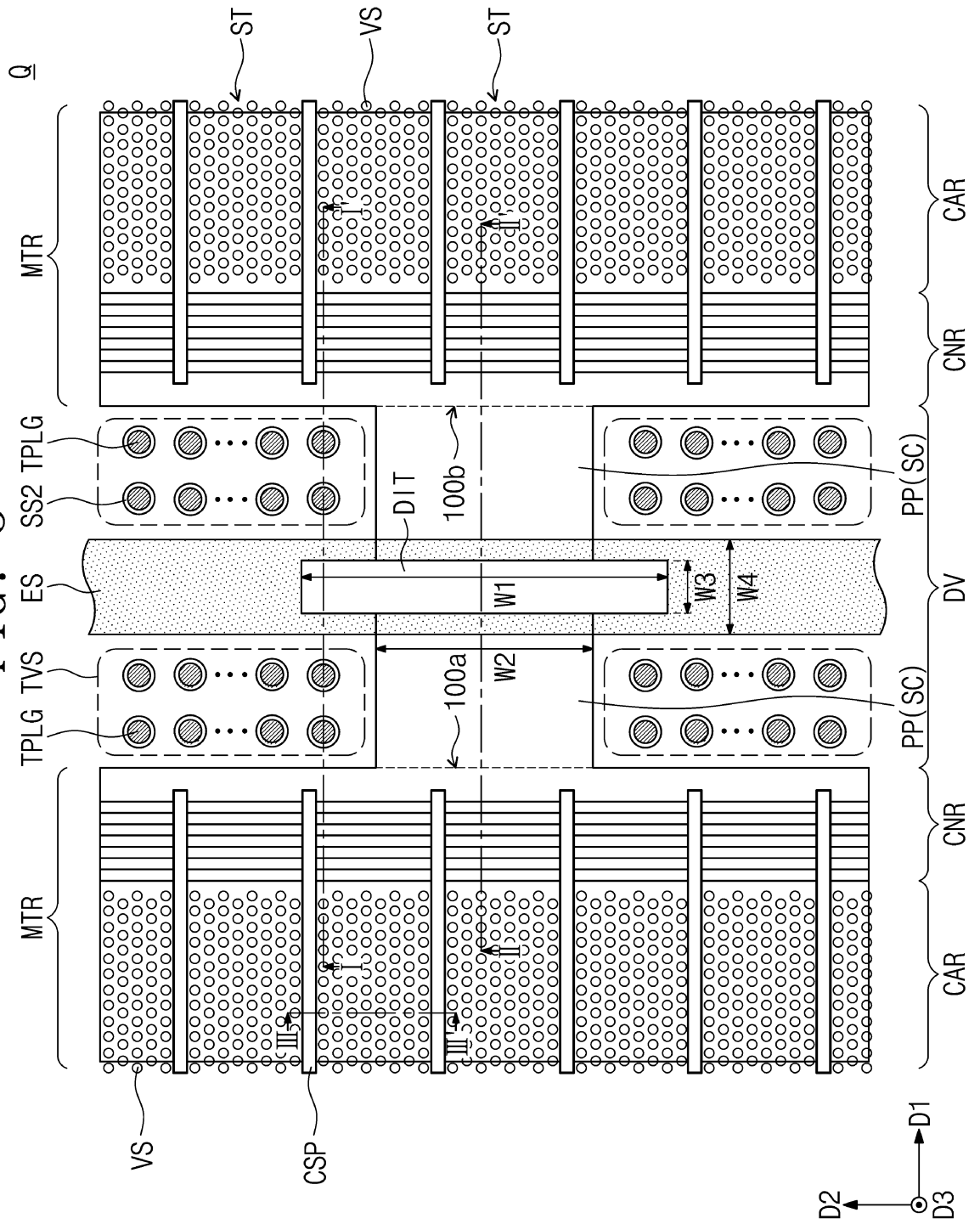


FIG. 6

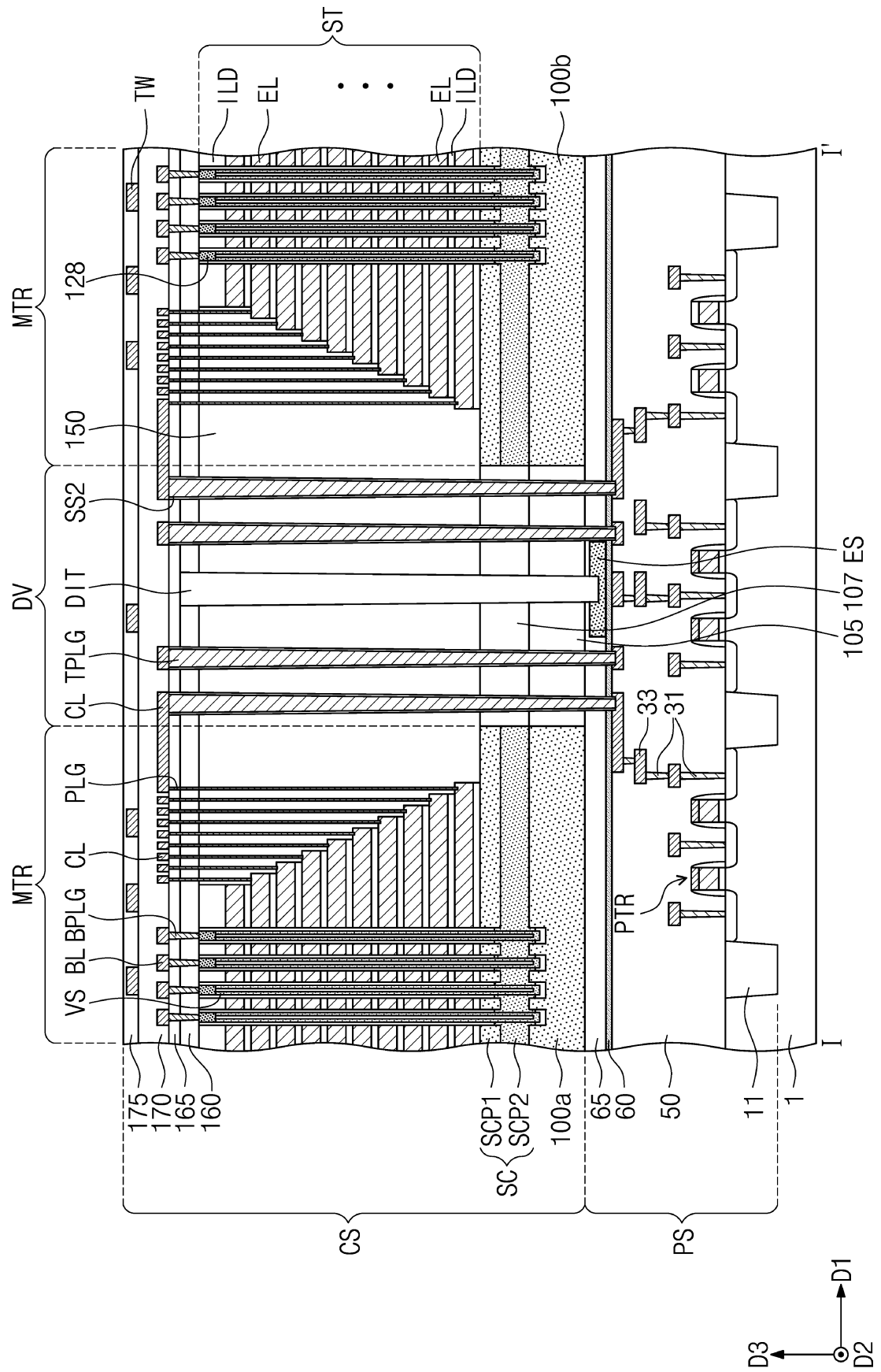


FIG. 7

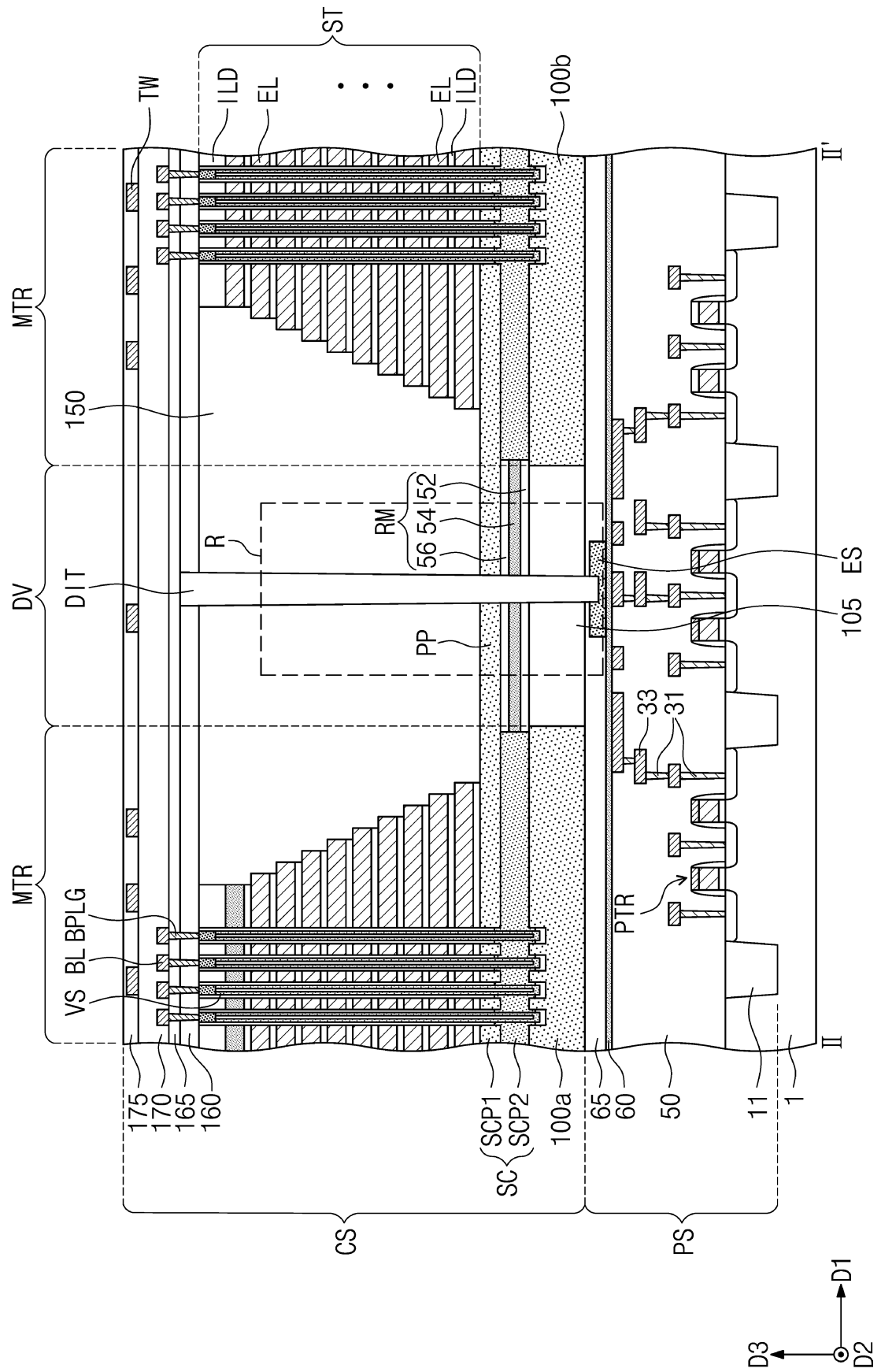


FIG. 8

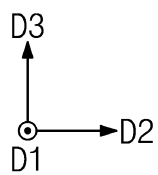
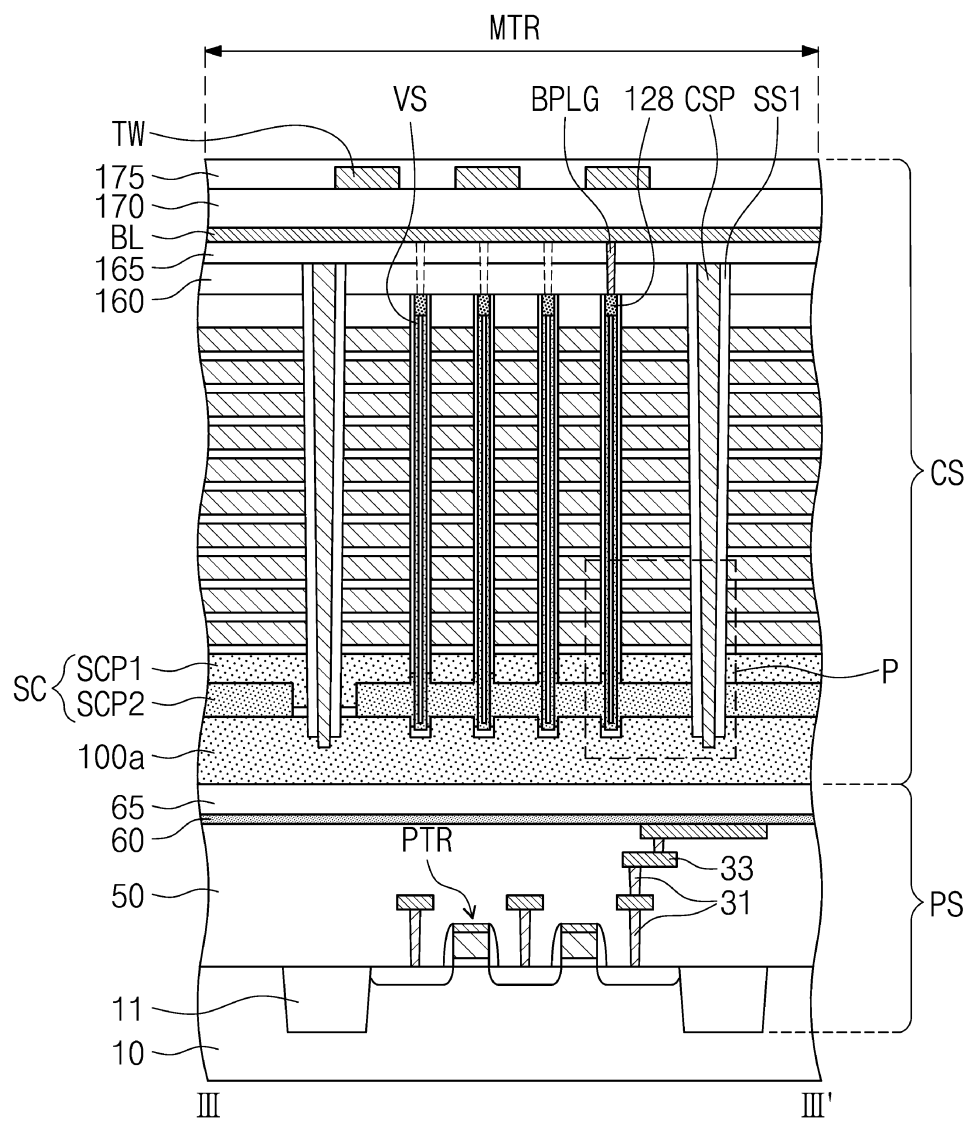


FIG. 9A

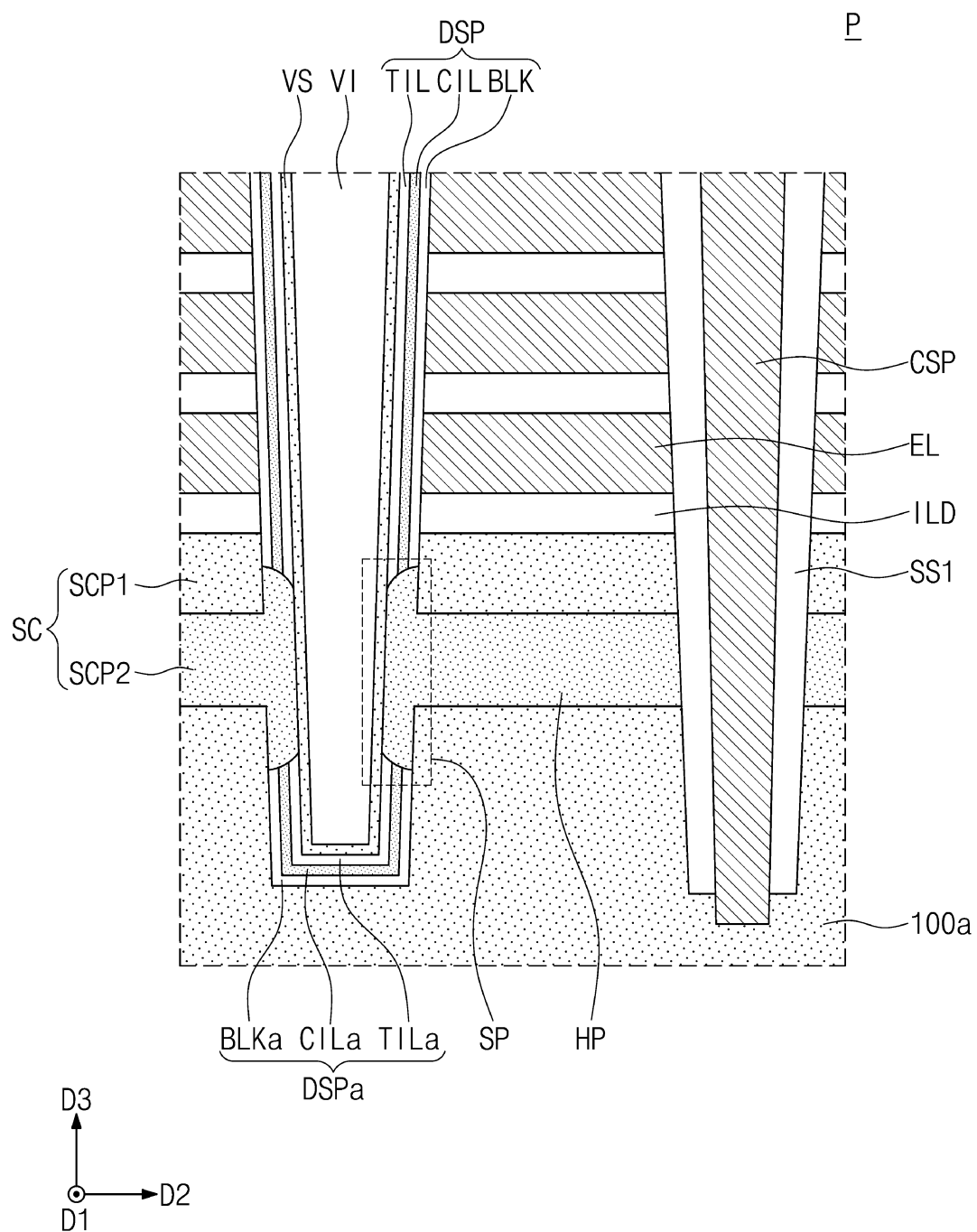


FIG. 9B

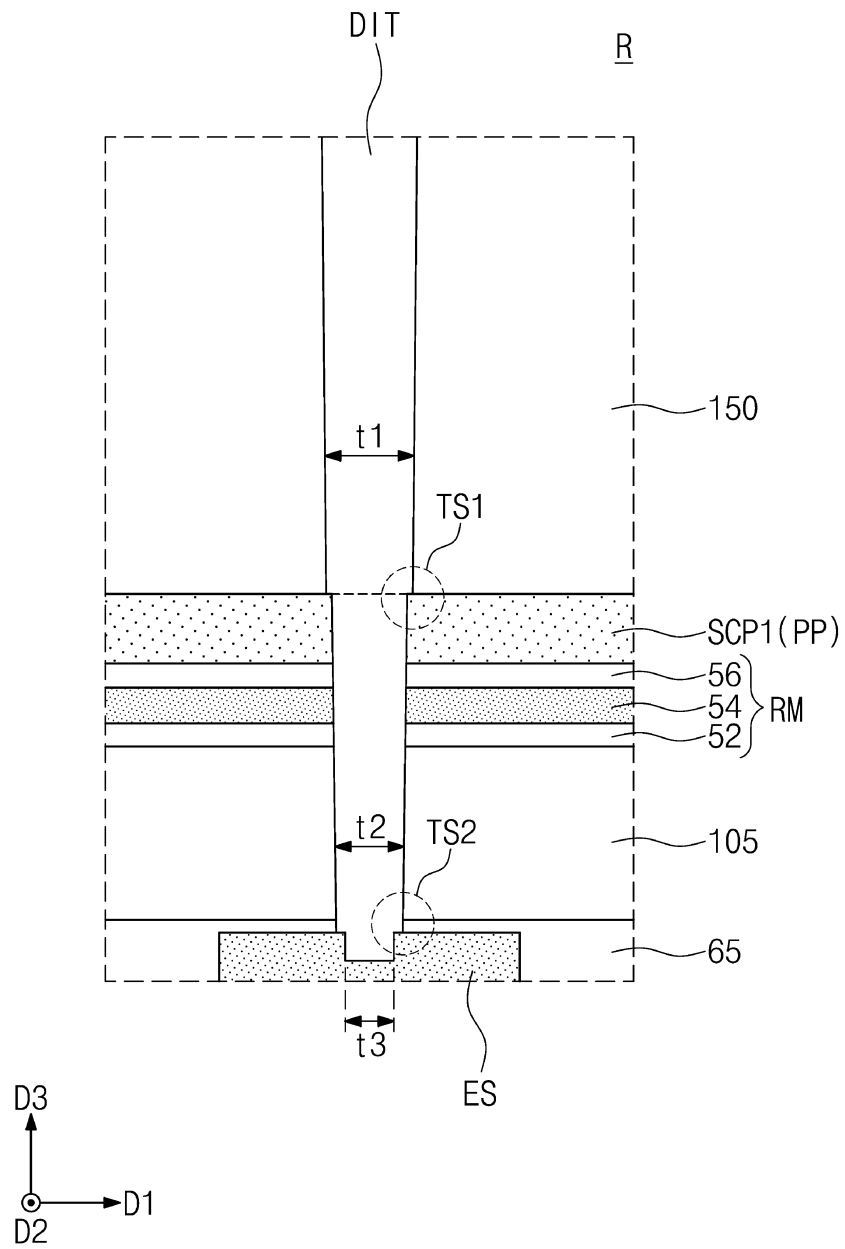


FIG. 10

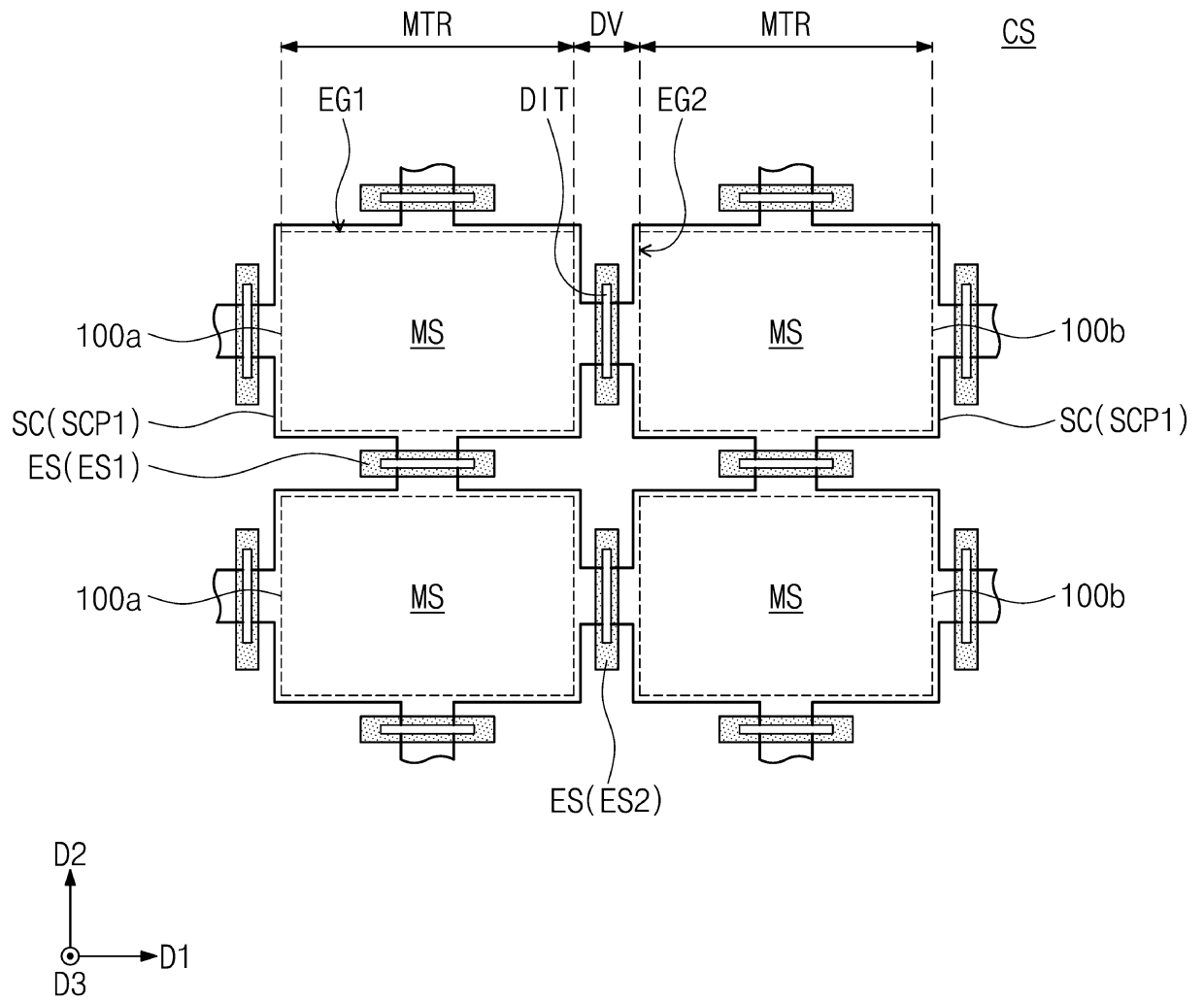


FIG. 11

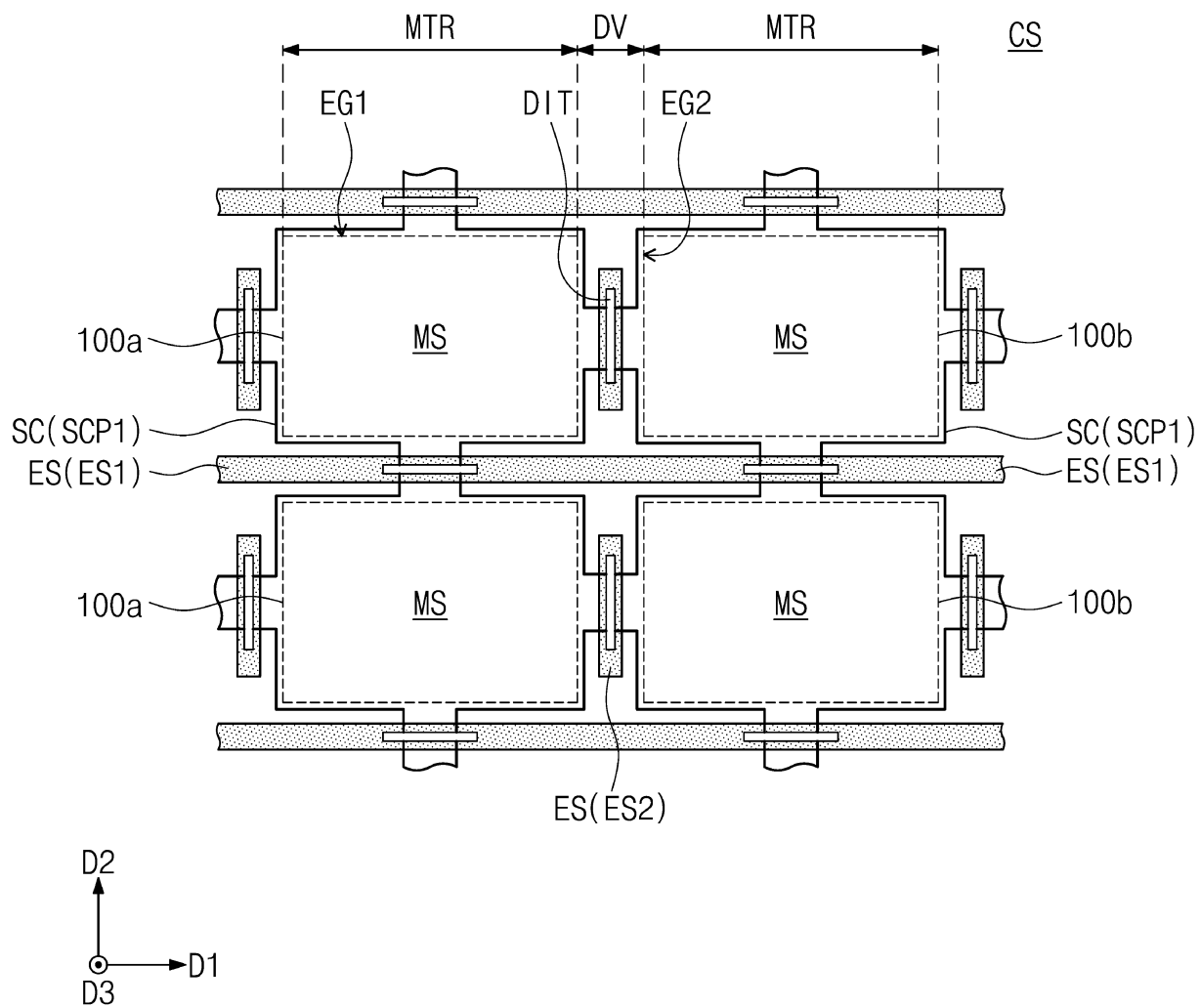


FIG. 12

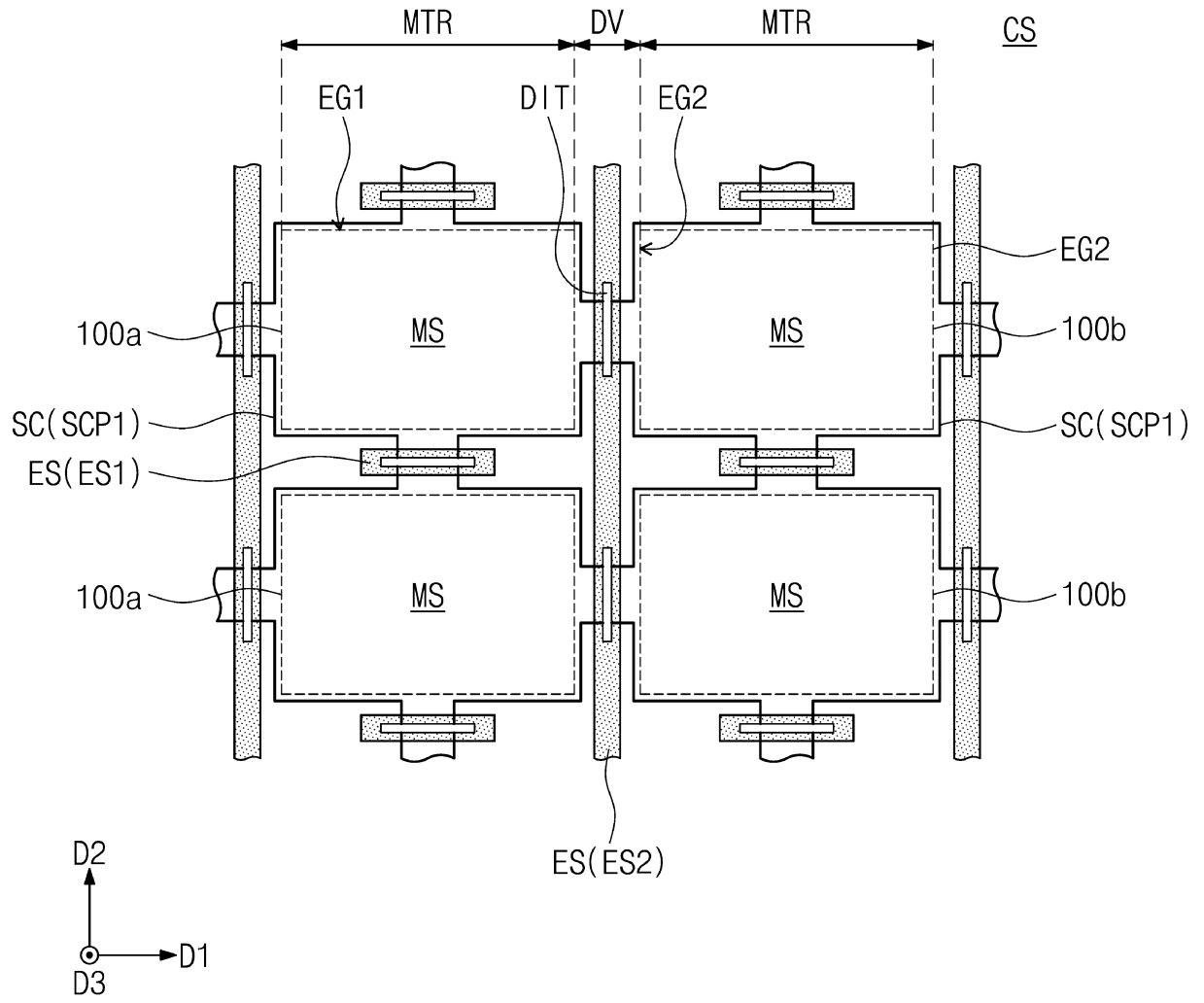


FIG. 13

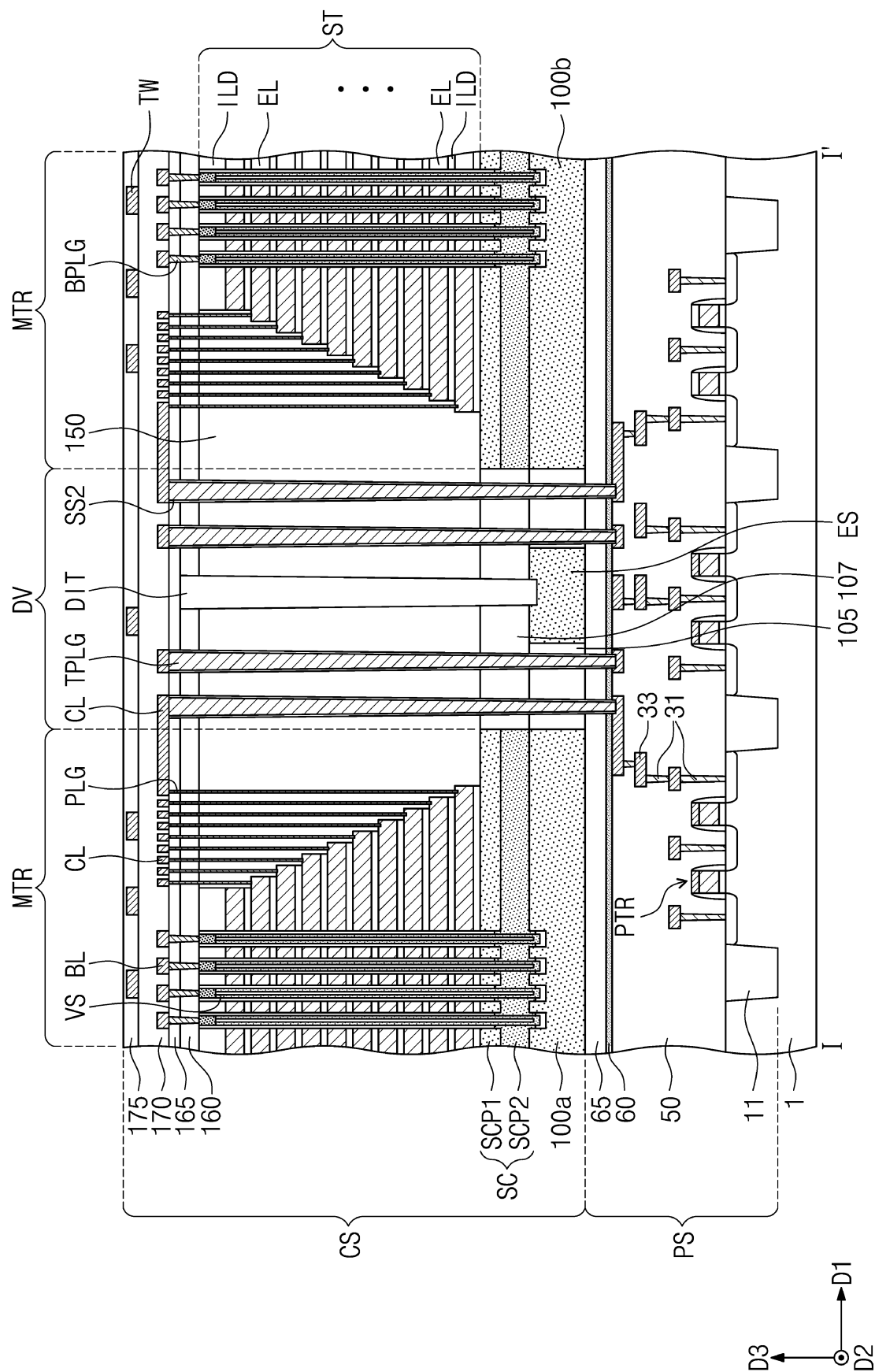


FIG. 14

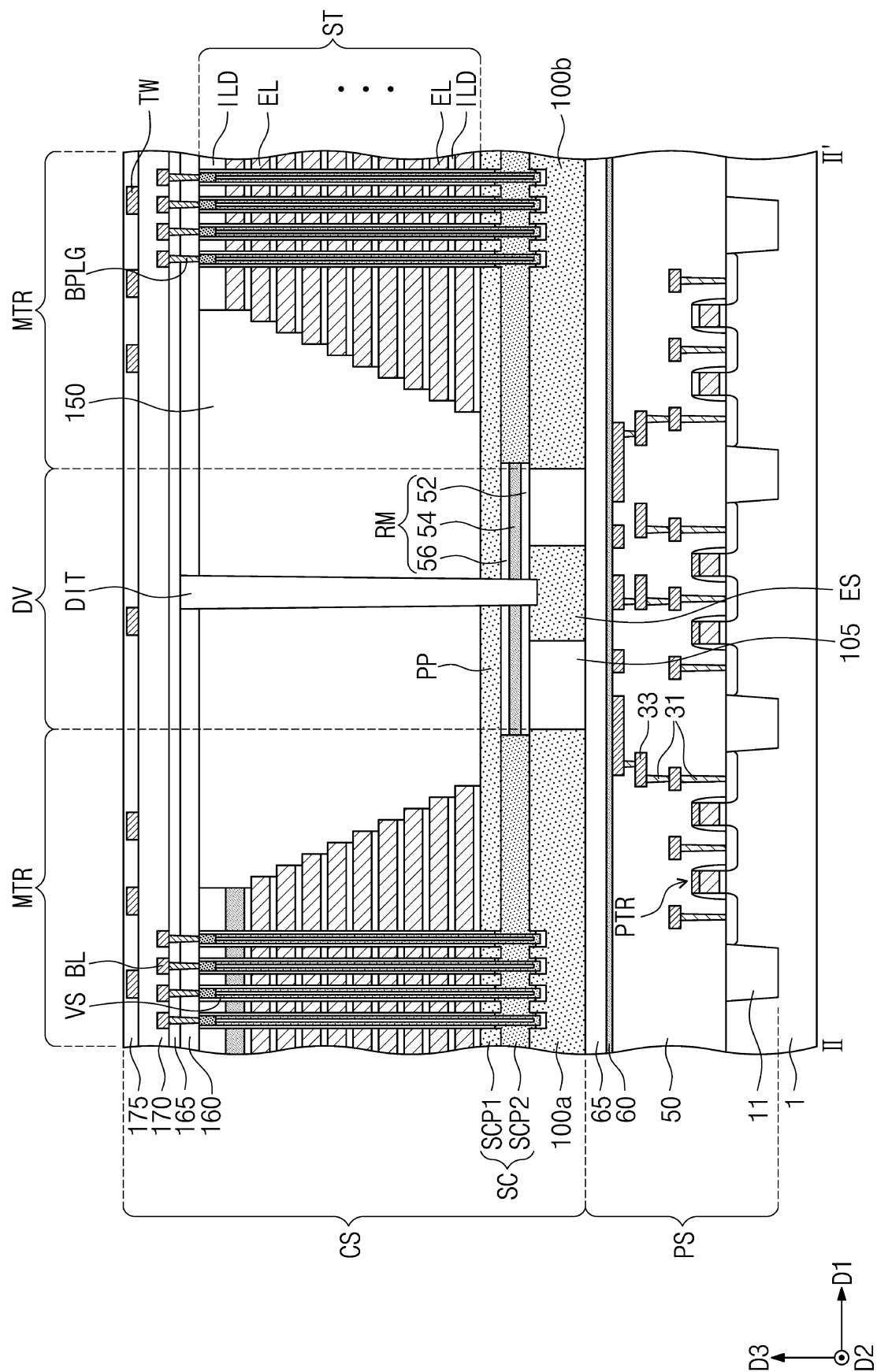


FIG. 15

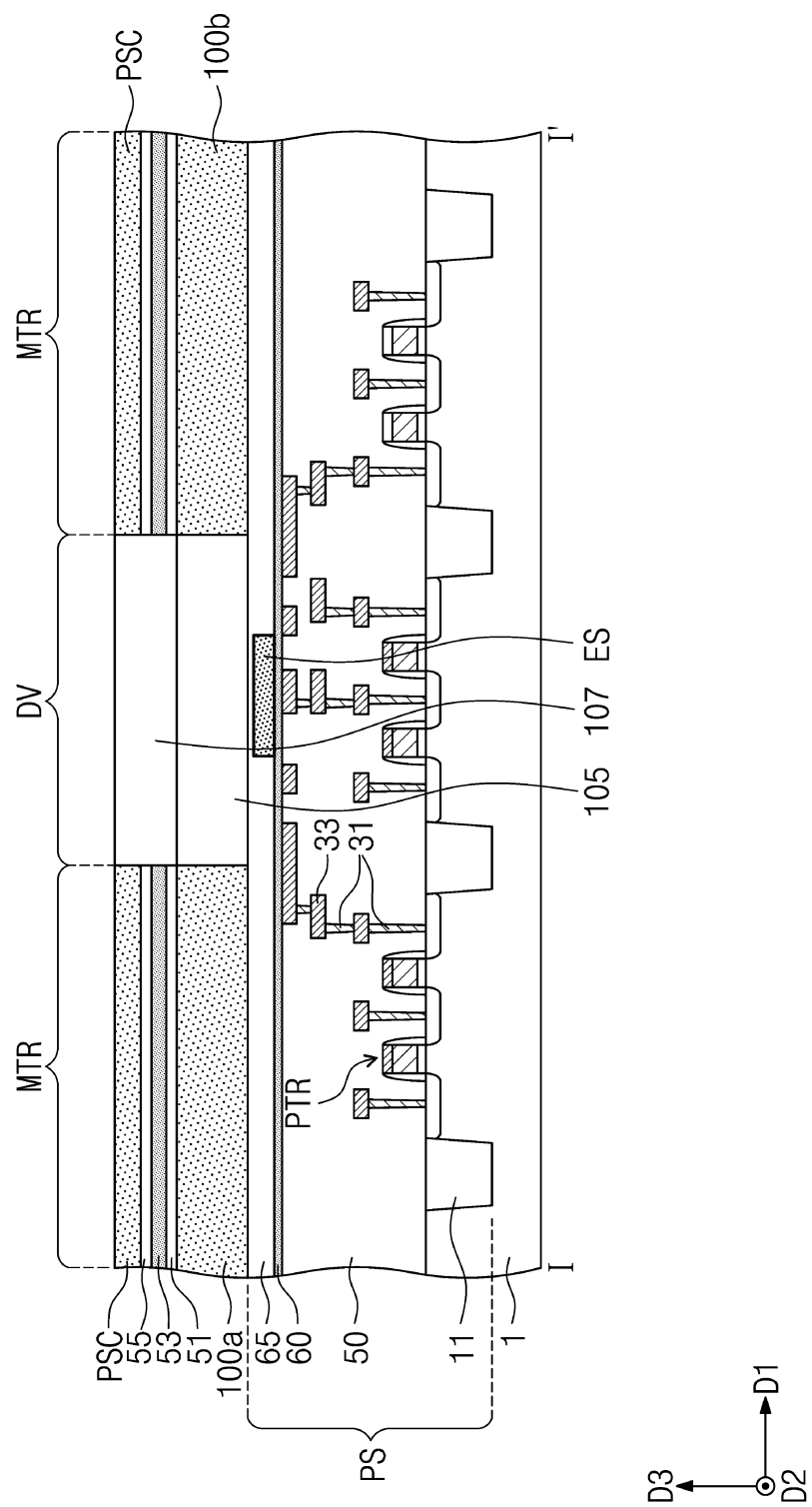


FIG. 16

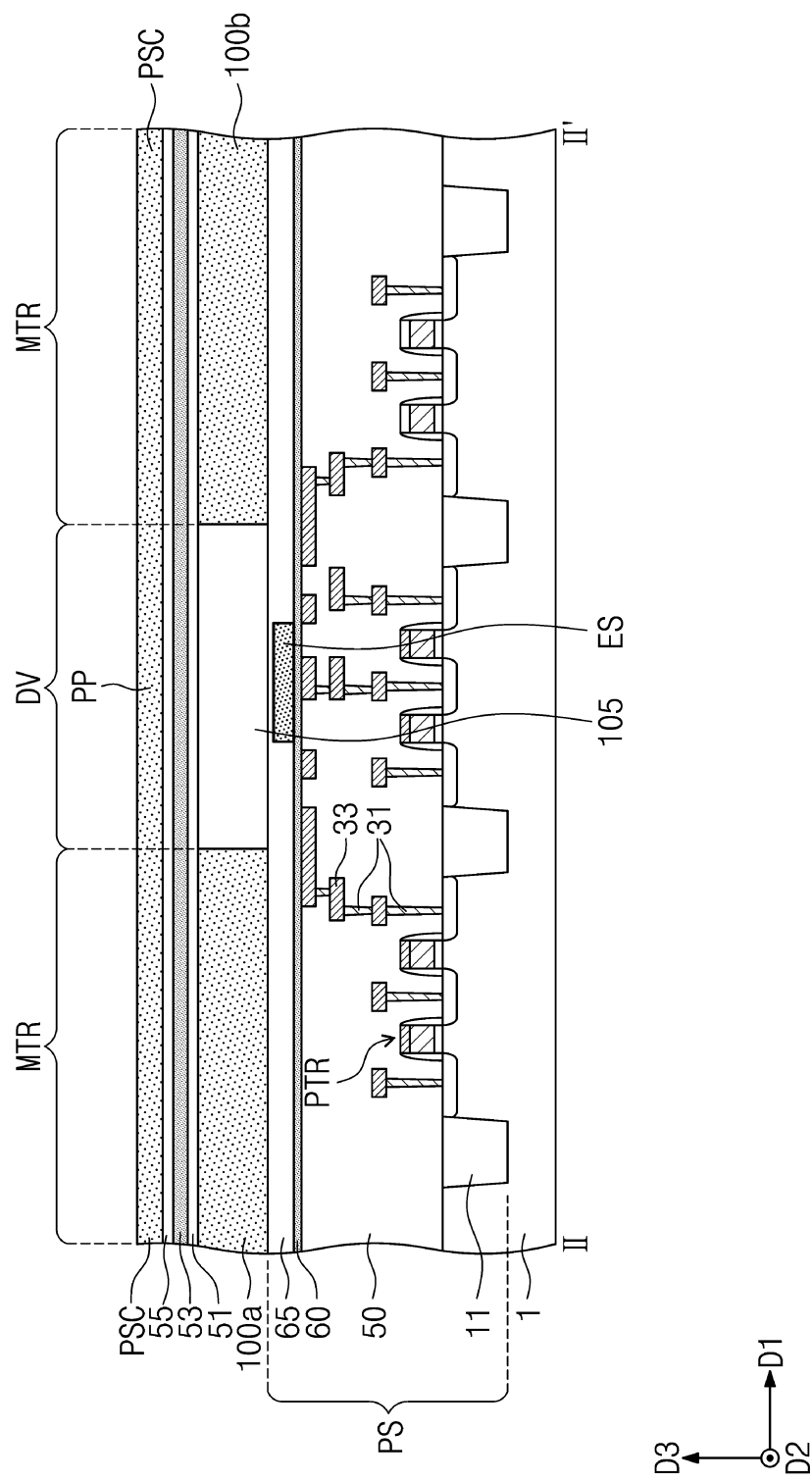
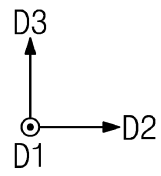
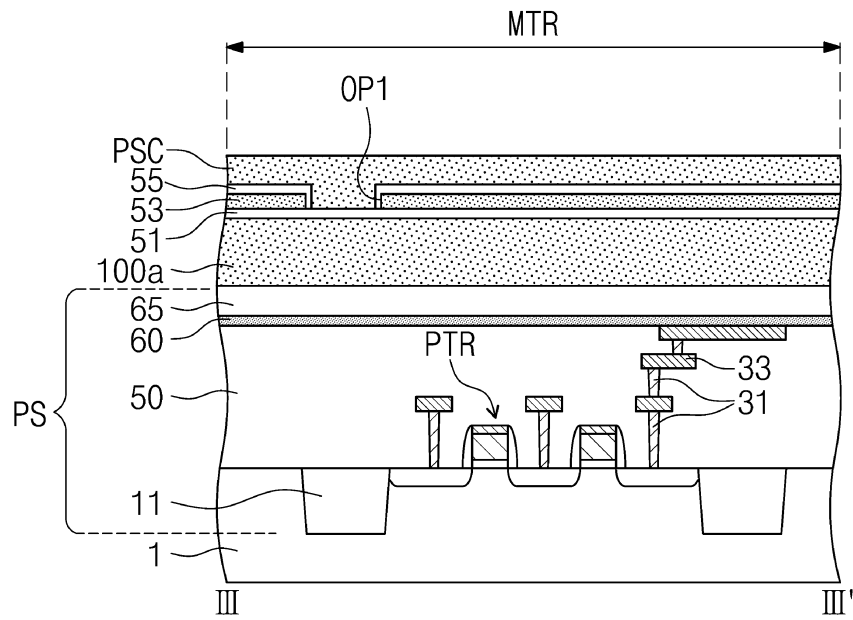


FIG. 17



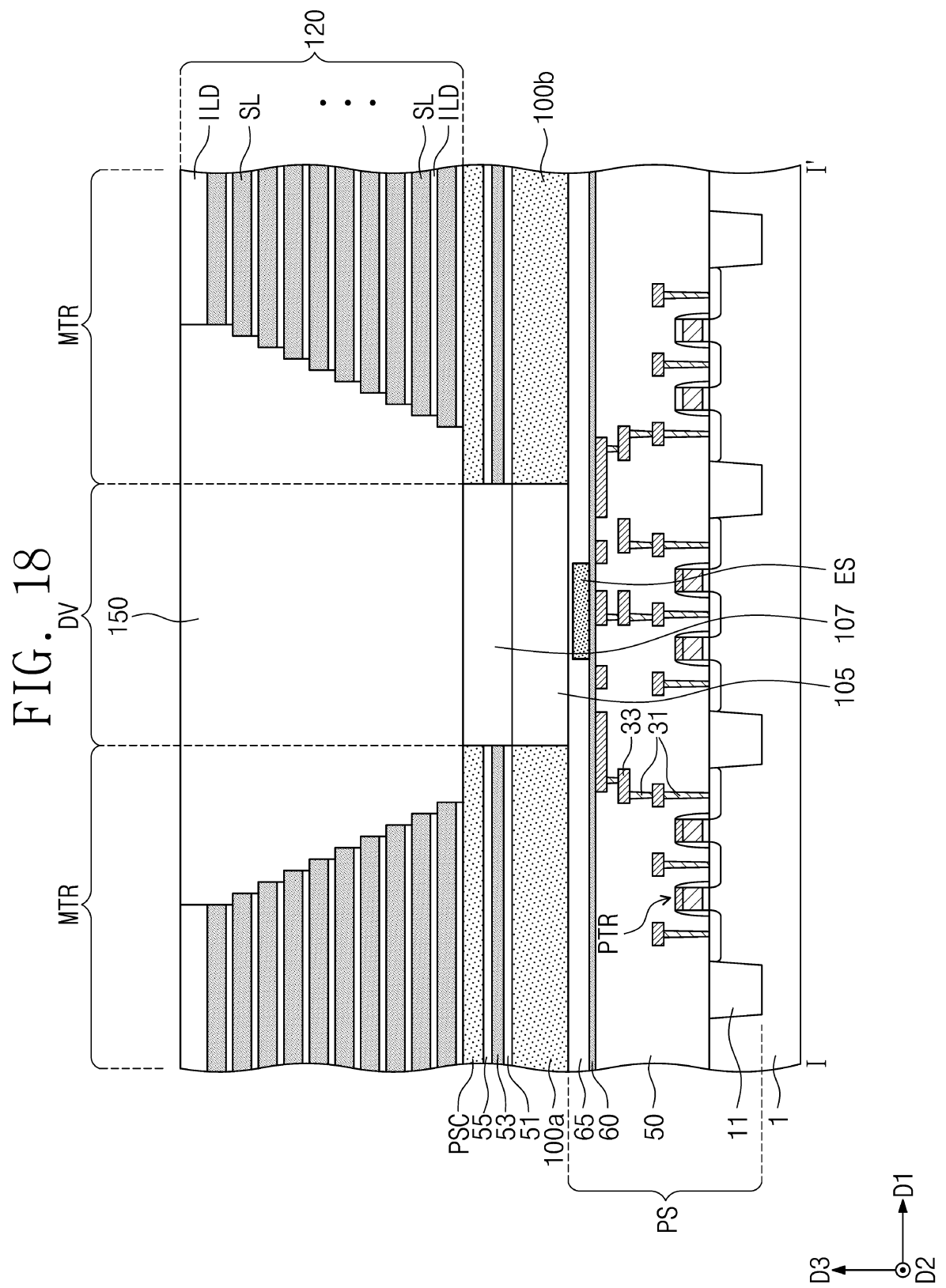


FIG. 19

FIG. 19 is a cross-sectional view of a semiconductor device, taken along a vertical plane II-II'. The device is built on a substrate 1, which has a patterned layer 11. Above the substrate, there is a stack of layers including 50, 60, 65, 100a, 51, 53, 55, and PSC. A central region 150 is defined by dashed lines, flanked by two MTR (Main Transfer Region) regions. The central region 150 contains a stack of layers 100b, 51, 53, 55, and PSC. The MTR regions contain a stack of layers 120, 51, 53, 55, and PSC. The stack 120 includes alternating layers of ILD (Interlayer Dielectric) and SL (Sacrificial Layer). A PTR (Pattern Transfer Region) layer is located between the central region 150 and the MTR regions. The device is further divided into DV (Device Vertical) and MTR regions. A coordinate system is shown at the bottom right with axes D1, D2, and D3.

FIG. 20

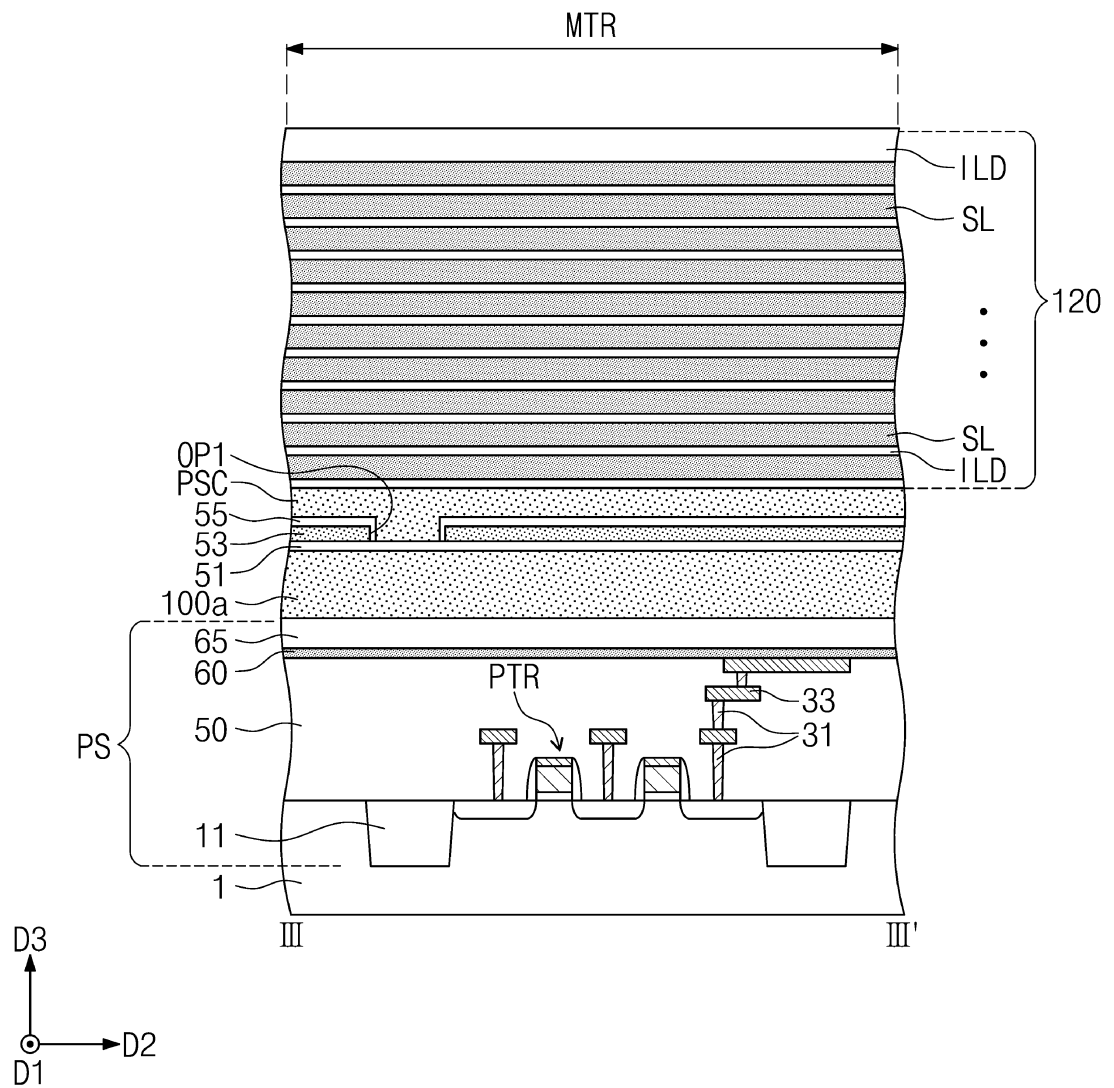


FIG. 21

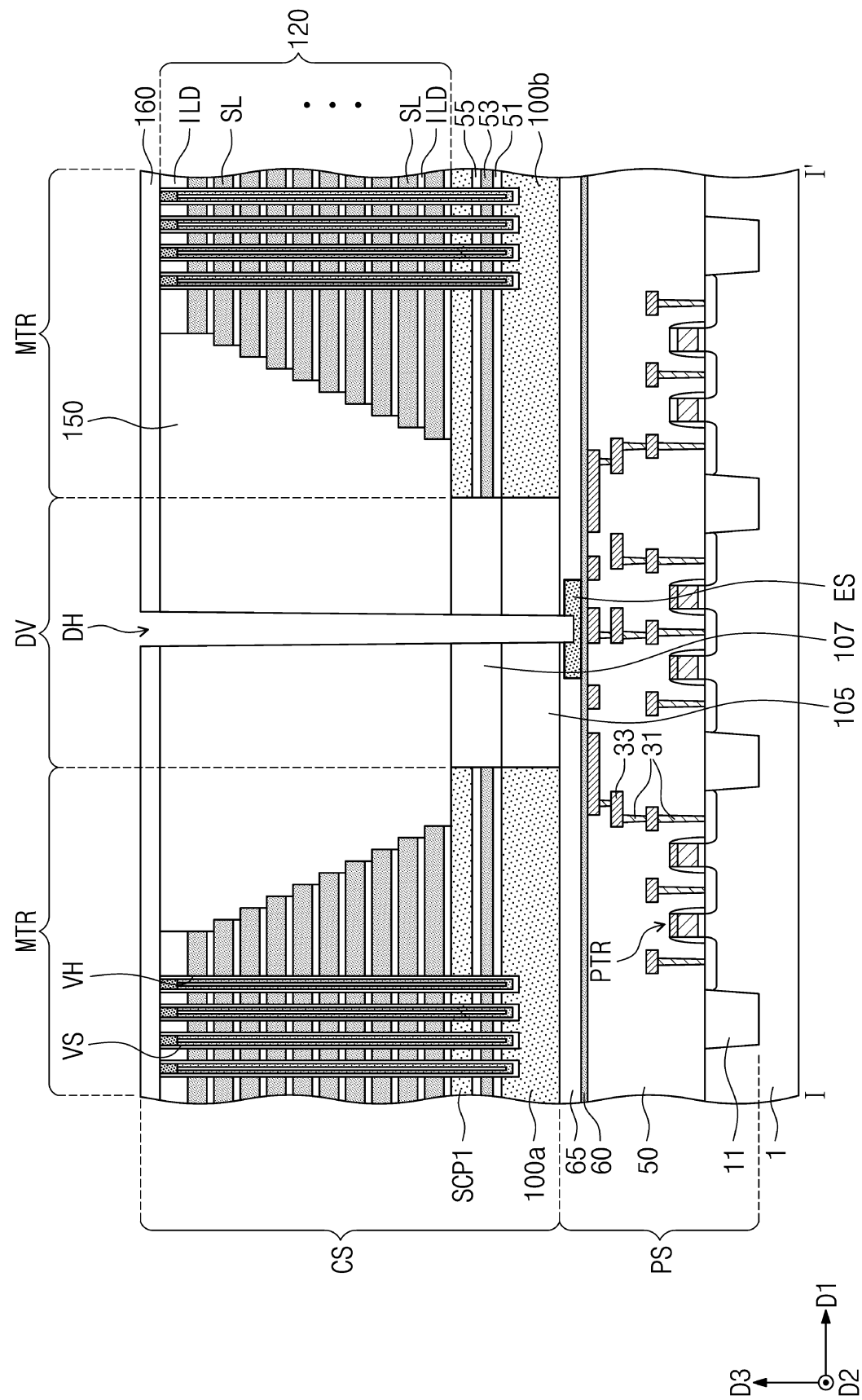


FIG. 22

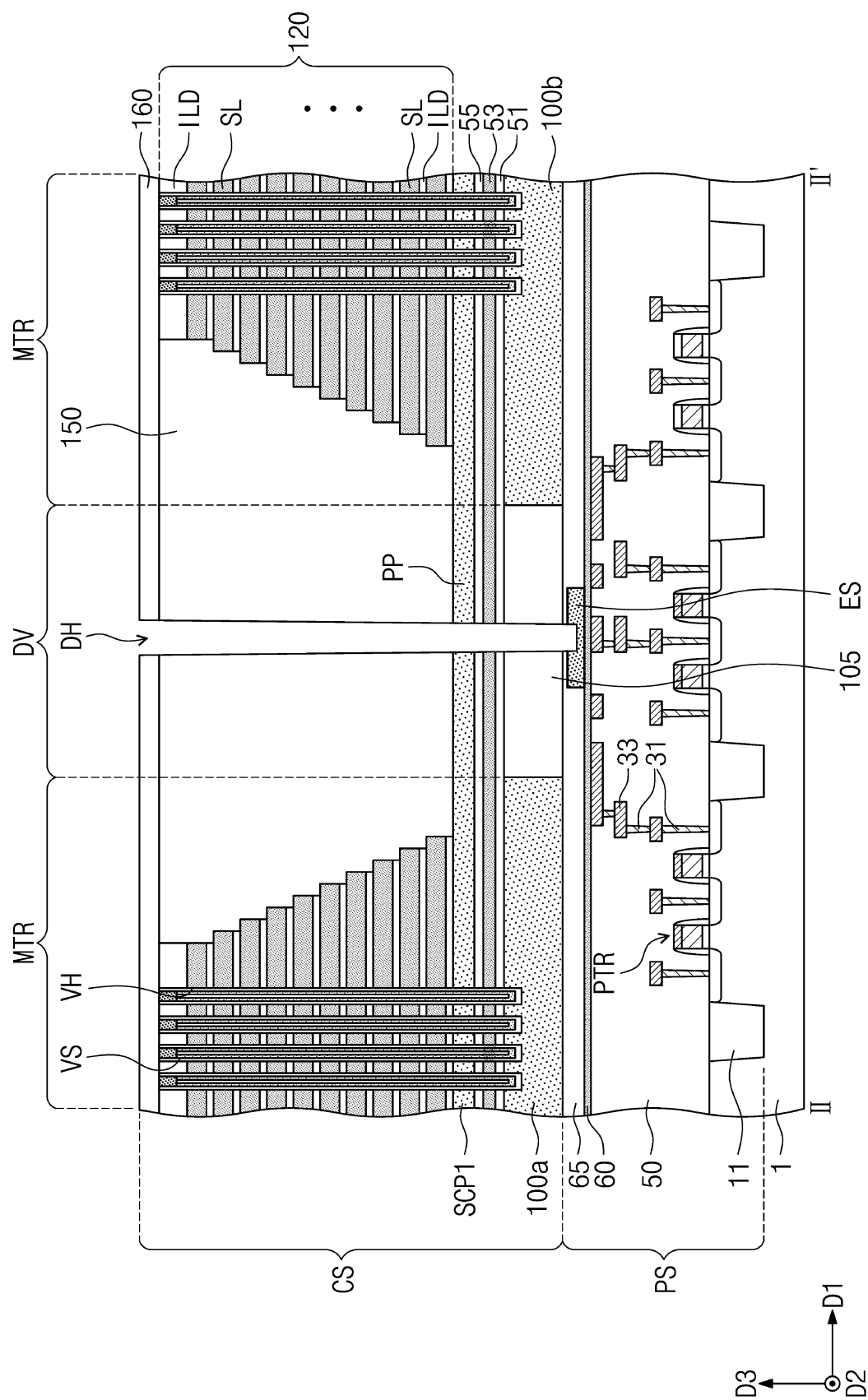


FIG. 23

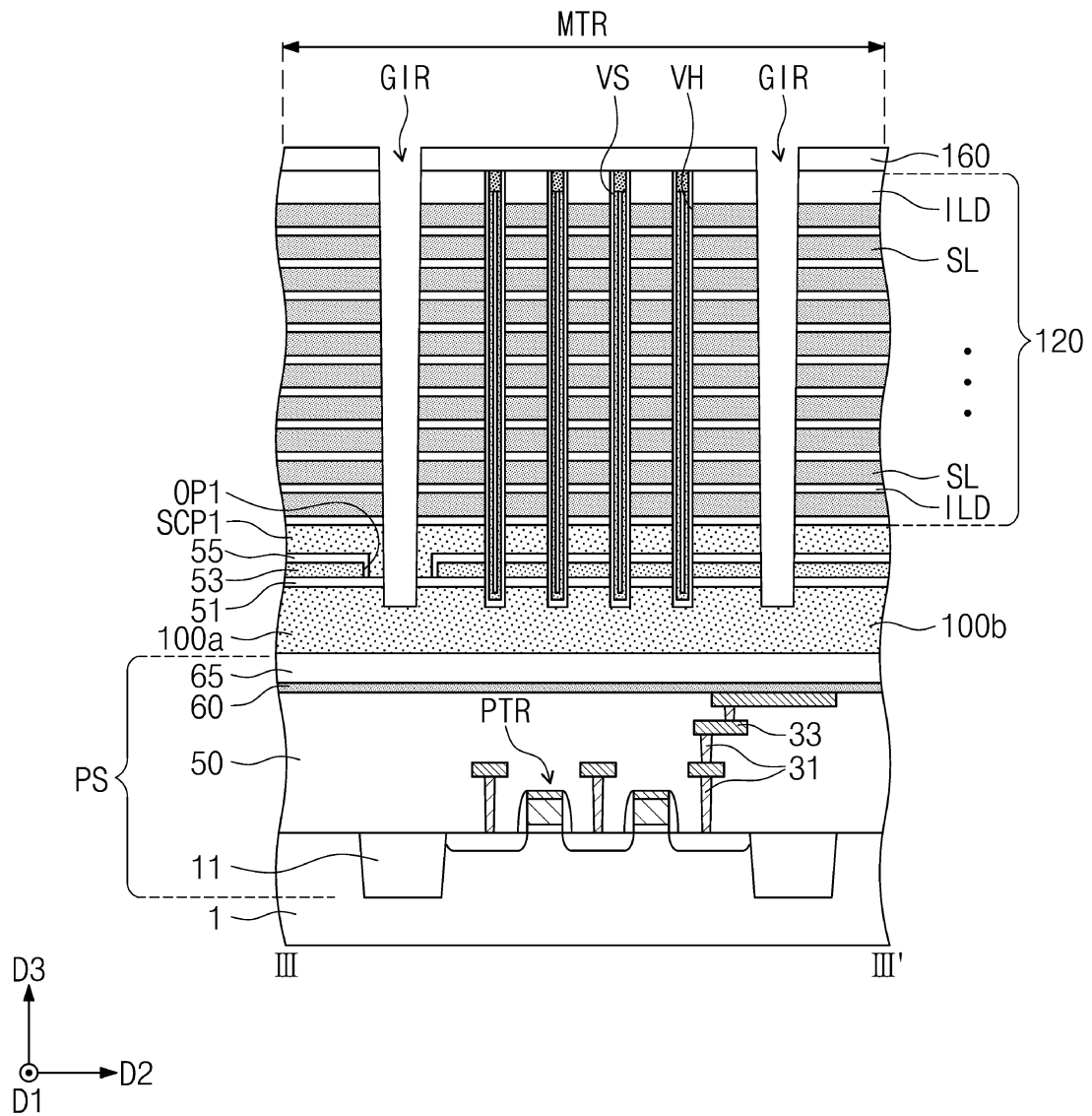


FIG. 24

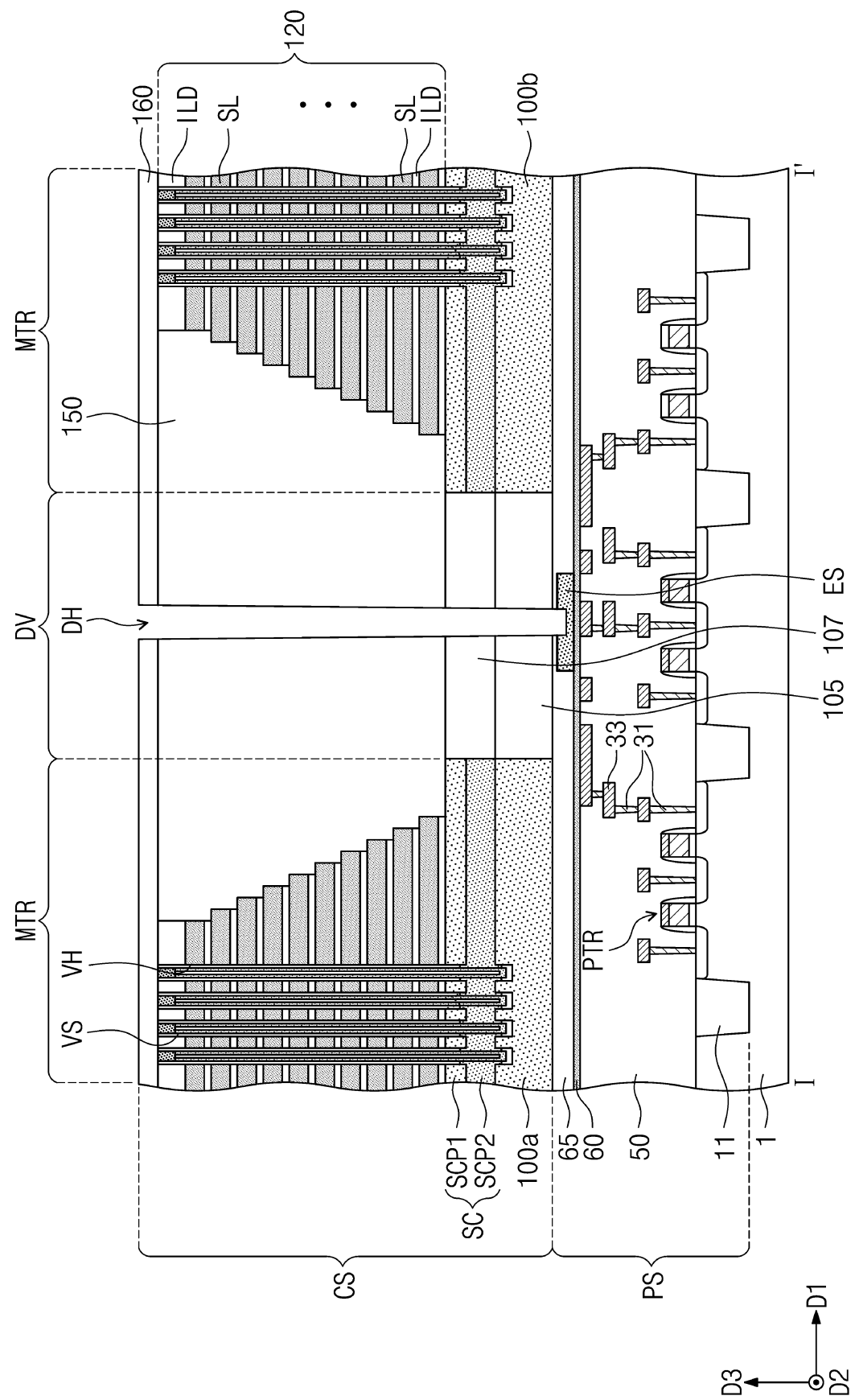


FIG. 25

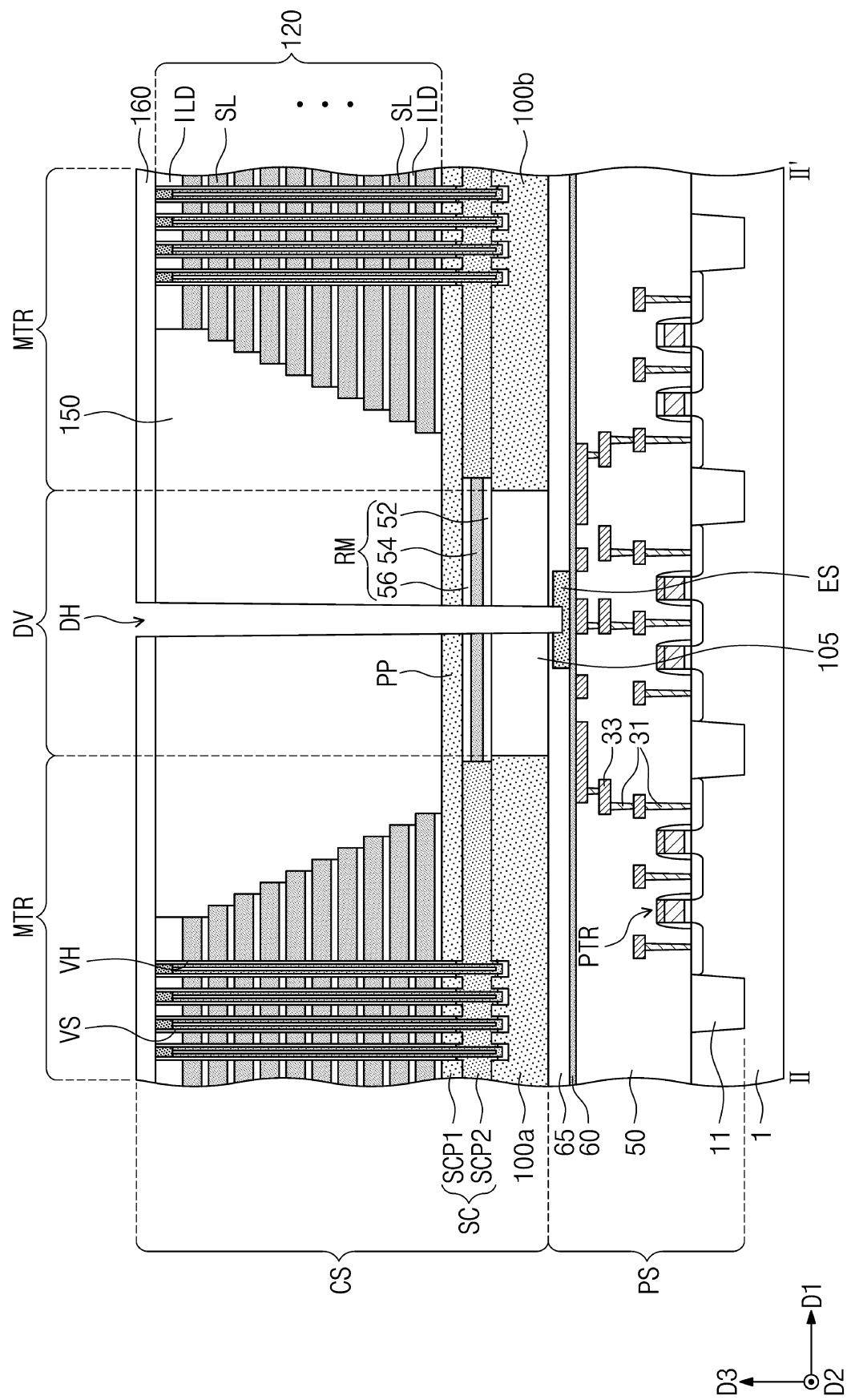


FIG. 26

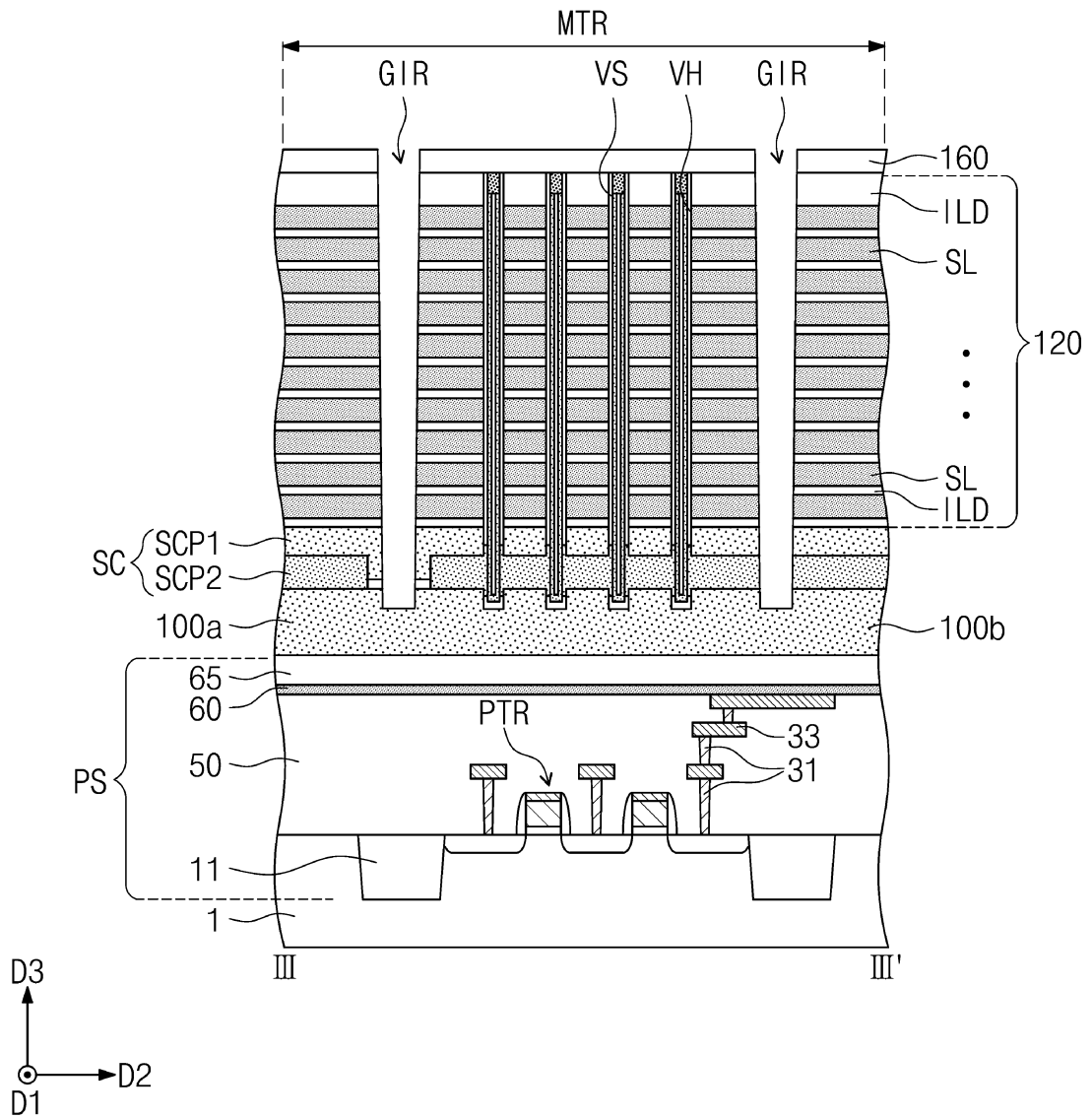


FIG. 27

