Claims

1. A Field Programmable Gate Array capable of implementing a logic function said Field Programmable Gate Array comprising a plurality of hardware lookup tables, the select lines or outputs of each lookup table being programmably interconnected with the select lines or outputs of another said lookup table by means of a plurality of programmable switches, said Field Programmable Gate Array characterized by further comprising:

a plurality of flip flops in a shift register configuration, each said Lookup table having at least one input coupled to an output of a respective said flip flop, and each said programmable switch coupled to an output of a further respective said flip flop; and

wherein said Field Programmable Gate Array is arranged to operate in a first mode in which said shift register is loaded with predefined test values, and a second mode in which said shift register is loaded with values implementing said logic function.

2. The Field Programmable Gate Array of any preceding claim wherein a first flip flop in said shift register is coupled to an input multiplexer, said input multiplexer receiving said predefined test values on a first input and said values implementing said logic function a second input, and responsive to a mode selection signal adapted to feed either said test pattern or said data bitstream to said first flipflop.

3. The Field Programmable Gate Array of any preceding claim wherein said shift register is one of a plurality of such shift registers configured to supply different parts of said Field Programmable Gate Array.

4. The Field Programmable Gate Array of claim 3 wherein said plurality of shift registers are configured to be loaded with said predefined test values in said first mode or said values implementing said logic function in said second mode in parallel.

5. The Field Programmable Gate Array of claim 3 wherein said plurality of shift registers are configured to be loaded with said predefined test values in said first mode or said values implementing said logic function in said second mode in series.

6. The Field Programmable Gate Array of claims 3 to 5 further comprising an addressing system whereby any of said plurality of shift registers may be individually or by group addressed in order to be loaded with said predefined test values in said first mode or said values implementing said logic function in said second mode.

7. The Field Programmable Gate Array of claim 6 wherein said addressing system comprises a respective addressable clock gate associated with each said shift register, said clock gate being adapted to provide a clock signal to the shift register with which it is associated when thus addressed.

8. The Field Programmable Gate Array of any preceding claim further adapted to implement a third mode of operation in which said values implementing said logic function loaded into said shift registers in said second mode of operation are read back out of said shift registers.

9. A method of operating an FPGA comprising the steps of:

instructing a multiplexer having an output coupled to a programming shift register to select an input receiving configuration values implementing a test protocol,

instructing a plurality of LUT flip flops, to enter a test configuration wherein each said LUT flip flop receives inputs implementing said test protocol, and wherein said LUT flip flops are connected as a shift register,

clocking said programming shift register to load a first set of elements thereof with LUT Configuration values belonging to said configuration values implementing said test protocol;

clocking said programming shift register to load a second set of elements of said shift register with routing switch configuration belonging to said configuration values implementing said test protocol,

instructing said plurality of LUT flip flops to enter an operational configuration wherein each said LUT flip flop receives inputs from the outputs of a plurality of LUTs respectively,

applying data inputs to said plurality of LUTs,

clocking said LUT flipflops to sample the outputs of each said LUT into a respective said flipflop, said outputs being responsive to said test protocol and said data inputs,

instructing said LUT flip flops to enter into a test configuration in which said LUT flip flops are connected in a LUT shift register, and connected as a shift register, and

clocking said LUT flipflops to read out the values of said LUT shift register comprising said outputs of said LUTs responsive to said test protocol and said data inputs.

10. A computer program adapted to implement the steps of the method of claim 9.

11. A computer readable medium incorporating the computer program of claim 10.