

ETCHING METHOD OF MULTILAYERED FILM

TECHNICAL FIELD

[0001] The embodiments described herein pertain generally to an etching method of etching a multilayered film.

BACKGROUND

[0002] As a kind of semiconductor device, there is known a NAND type flash memory device having a three-dimensional structure. In the manufacture of this NAND type flash memory device having the three-dimensional structure, a deep hole is formed in a multilayered film, which is composed of alternately stacked two layers having different permittivities, by performing an etching process. This etching process is described in Patent Document 1.

[0003] To elaborate, in Patent Document 1, there is described a method of etching a multilayered film by exposing a processing target object having a mask on the multilayered film to plasma of a processing gas containing a HBr gas, a C_4F_8 gas and a BCl_3 gas. In the method described in Patent Document 1, a polycrystalline silicon film of the multilayered film is etched by an active species generated from the HBr gas; a silicon oxide film of the multilayered film is etched by active species generated from the C_4F_8 gas; and a protective film generated from the BCl_3 gas is deposited on a sidewall surface formed by the etching of the multilayered film. The protective film suppresses the multilayered film from being etched in a direction (*i.e.*, a horizontal direction) orthogonal to a stacking direction (*i.e.*, a vertical direction) of the multilayered film. Therefore, verticality of a space such as a hole formed in the multilayered film can be improved.

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[0005] In the etching method described in Patent Document 1, however, the size of the opening of the mask may become smaller, and, occasionally, the opening may be completely clogged. Further, it is still required to further improve the verticality of the space formed in the multilayered film by forming a stronger protective film.

[0006] Thus, in the present technical field, the clogging of the opening of the mask needs to be suppressed, and the verticality of the space formed in the multilayered film needs to be improved.

SUMMARY

[0007] In one exemplary embodiment, an etching method of etching a multilayered film is provided. The multilayered film includes a first film and a second film that have different permittivities and are alternately stacked on top of each other. The etching method includes preparing, within a processing vessel of a plasma processing apparatus, a processing target object having the multilayered film and a mask provided on the multilayered film; and etching the multilayered film by exciting a processing gas containing a hydrogen gas, a hydrofluorocarbon gas, a fluorine-containing gas, a hydrocarbon gas, a boron trichloride gas and a nitrogen gas within the processing vessel.

[0008] The processing gas used in this etching method includes a nitrogen gas. Active species generated from the nitrogen gas etches a carbon-containing deposit deposited on the mask, so that an opening of the mask is suppressed from being clogged with the deposit. Further, the active species of the nitrogen gas nitrifies a protective film formed on a sidewall surface forming a space formed in the multilayered film, that is, a protective film containing boron. As a

result, the protective film is modified to be a stronger protective film. Thus, verticality of the space formed in the multilayered film can be further improved.

[0009] In the exemplary embodiment, the hydrofluorocarbon gas may be a CH_2F_2 gas, a CH_3F gas or a CHF_3 gas. The fluorine-containing gas may be a NF_3 gas or a SF_6 gas. The hydrocarbon gas may be a CH_4 gas.

[0010] In the exemplary embodiment, the first film may be a silicon oxide film, and the second film may be a silicon nitride film. The first film may be a silicon oxide film, and the second film may be a polysilicon film. The first film and the second film may be stacked in twenty-four or more layers in total.

[0011] In the exemplary embodiment, the mask may be made of amorphous carbon.

[0012] According to the exemplary embodiment described above, it is possible to improve verticality of the space formed in the multilayered film while suppressing the opening of the mask from being clogged.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] In the detailed description that follows, embodiments are described as illustrations only since various changes and modifications will become apparent to those skilled in the art from the following detailed description. The use of the same reference numbers in different figures indicates similar or identical items.

FIG. 1 is a flowchart for describing a method of etching a multilayered film according to an exemplary embodiment;

FIG. 2 is a diagram showing an example wafer prepared in a process ST1;

FIG. 3 is a diagram illustrating an outline of a plasma processing apparatus;

FIG. 4 is a diagram providing a detailed view of a valve group, a flow rate controller group and a gas source group shown in **FIG. 3**;

FIG. 5 is a diagram showing a wafer being etching in a process ST2;

FIG. 6 is a diagram for describing inclination angles obtained in an experimental example and a comparative example;

FIG. 7 is a diagram for describing a deviation amounts of a central line obtained in the experimental example and the comparative example; and

FIG. 8 is a table showing the inclination angles and the deviation amounts obtained in the experimental example and the comparative example.

DETAILED DESCRIPTION

[0014] In the following detailed description, reference is made to the accompanying drawings, which form a part of the description. In the drawings, similar symbols typically identify similar components, unless context dictates otherwise. Furthermore, unless otherwise noted, the description of each successive drawing may reference features from one or more of the previous drawings to provide clearer context and a more substantive explanation of the current exemplary embodiment. Still, the exemplary embodiments described in the detailed description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter

presented herein. It will be readily understood that the aspects of the present disclosure, as generally described herein and illustrated in the drawings, may be arranged, substituted, combined, separated, and designed in a wide variety of different configurations, all of which are explicitly contemplated herein.

[0015] FIG. 1 is a flowchart for describing a method of etching a multilayered film according to an exemplary embodiment. The method MT shown in FIG. 1 is applicable to a manufacture of, for example, a NAND flash memory having a three-dimensional structure. The method MT includes a process ST1 and a process ST2.

[0016] In the process ST1, a processing target object (hereinafter, referred to as “wafer”) is prepared. FIG. 2 is a diagram illustrating an example of the wafer W prepared in the process ST1. The wafer W shown in FIG. 2 has a base layer UL, a multilayered film IL and a mask MSK. The base layer UL may be a polycrystalline silicon layer provided on a substrate. The multilayered film IL is provided on the base layer UL. The multilayered film IL has a structure in which two dielectric films IL1 and IL2 having different permittivities are alternately stacked. In the exemplary embodiment, the dielectric film IL1 may be a silicon oxide film, and the dielectric film IL2 may be a silicon nitride film. In other exemplary embodiments, the dielectric film IL1 may be a silicon oxide film, and the dielectric film IL2 may be a polysilicon film. By way of non-limiting example, a thickness of the dielectric film IL1 is in the range from, but not limited to 5 nm to 50 nm, and a thickness of the dielectric film IL2 is in the range from, but not limited to, 10 nm to 75 nm. The dielectric films IL1 and IL2 may be stacked in twenty-four or more layers in total. The mask MSK is provided on the multilayered film IL. The mask MSK has a pattern for forming a space such as a hole in the multilayered film IL. The mask MSK may be made of, by way of

example, but not limitation, amorphous carbon. Alternatively, the mask MSK may be made of, for example, organic polymer.

[0017] Referring back to **FIG. 1**, in the process ST1 of the method MT, the wafer W is prepared within a processing vessel of a plasma processing apparatus. As an example, the plasma processing apparatus may be configured as a capacitively coupled plasma processing apparatus. Below, an example of the plasma processing apparatus in which the method MT can be performed will be first explained. **FIG. 3** is a diagram depicting an outline of the plasma processing apparatus and illustrates a longitudinal cross-sectional view of the plasma processing apparatus.

[0018] The plasma processing apparatus 10 shown in **FIG. 3** is configured as a capacitively coupled plasma etching apparatus and includes a substantially cylindrical processing vessel 12. An inner wall surface of the processing vessel 12 is made of anodically oxidized aluminum. This processing vessel 12 is frame-grounded.

[0019] A substantially cylindrical supporting member 14 is provided on a bottom of the processing vessel 12. Within the processing vessel 12, the supporting member 14 is vertically extended from the bottom of the processing vessel 12. The supporting member 14 sustains a placing table PD provided within the processing vessel 12. To elaborate, as depicted in **FIG. 3**, the supporting member 14 may support the placing table PD on an inner wall surface thereof.

[0020] The placing table PD is configured to hold the wafer W on a top surface thereof. The placing table PD may include a lower electrode 16 and a supporting unit 18. The lower electrode 16 is made of a metal such as, but not limited to, aluminum and has a substantially circular plate shape. The supporting unit 18 is provided on a top surface of this lower electrode 16.

[0021] The supporting unit 18 is configured to support the wafer W and includes a base member 18a and an electrostatic chuck 18b. The base member 18a is made of a metal such as, but not limited to, aluminum and has a substantially circular plate shape. The base member 18a is provided on the lower electrode 16 and is electrically connected with the lower electrode 16. The electrostatic chuck 18b is provided on the base member 18a. The electrostatic chuck 18b has a structure in which an electrode as a conductive film is embedded between a pair of insulating layers or insulating sheets. The electrode of the electrostatic chuck 18b is electrically connected with a DC power supply 22. The electrostatic chuck 18b is configured to attract and hold the wafer W by an electrostatic force such as a Coulomb force generated by a DC voltage applied from the DC power supply 22.

[0022] A focus ring FR is provided on a peripheral portion of the base member 18a of the supporting unit 18 to surround a peripheral of the wafer W and the electrostatic chuck 18b. The focus ring FR is provided to improve etching uniformity. The focus ring FR is made of a material that is appropriately selected depending on a material of an etching target film. By way of non-limiting example, the focus ring FR may be made of quartz.

[0023] A coolant path 24 is formed within the base member 18a. The coolant path 24 constitutes a temperature control device according to the exemplary embodiment. A coolant of a preset temperature is supplied into and circulated through the coolant path 24 from an external chiller unit via pipelines 26a and 26b. By controlling the temperature of the coolant being circulated, a temperature of the wafer W held on the supporting unit 18 can also be controlled.

[0024] Further, the plasma processing apparatus 10 is also equipped with a gas supply line 28. The gas supply line 28 is configured to supply a heat transfer gas from a heat transfer gas

supply unit, for example, a He gas, to between a top surface of the electrostatic chuck 18b and a rear surface of the wafer W.

[0025] In addition, the plasma processing apparatus 10 also includes an upper electrode 30. The upper electrode 30 is provided above the placing table PD to face the placing table PD. The lower electrode 16 and the upper electrode 30 are provided to be substantially parallel to each other. A processing space S in which a plasma process is performed on the wafer W is formed between the upper electrode 30 and the lower electrode 16.

[0026] The upper electrode 30 is held at a top portion of the processing vessel 12 with an insulating shield member 32 therebetween. The upper electrode 30 may include an electrode plate 34 and an electrode supporting body 36. The electrode plate 34 confronts the processing space S and is provided with a multiple number of gas discharge holes 34a. The electrode plate 34 may be made of a low-resistance conductor or semiconductor having a low Joule heat.

[0027] The electrode supporting body 36 is configured to support the electrode plate 34 in a detachable manner, and may be made of a conductive material such as, but not limited to, aluminum. The electrode supporting body 36 may have a water-cooling structure. A gas diffusion space 36a is formed within the electrode supporting body 36. A multiple number of gas through holes 36b respectively communicating with the gas discharge holes 34a is extended downwards from the gas diffusion space 36a. Further, the electrode supporting body 36 is provided with a gas inlet opening 36c through which a processing gas is introduced into the gas diffusion space 36a. The gas inlet opening 36c is connected with a gas supply line 38.

[0028] The gas supply line 38 is connected to a gas source group 40 via a valve group 42 and a flow rate controller group 44. FIG. 4 provides a detailed view of the valve group, the flow rate controller group and the gas source group shown in FIG. 3. As depicted in FIG. 4, the gas

source group 40 includes an N number of (N is a natural number) gas sources 401 to 406. The gas sources 401 to 406 are sources of a hydrogen gas (H_2 gas), a hydrofluorocarbon gas, a fluorine-containing gas, a hydrocarbon gas, a boron trichloride (BCl_3) gas and a nitrogen gas (N_2) gas, respectively. As an example of the hydrofluorocarbon gas, a CH_2F_2 gas, a CH_3F gas or a CHF_3 gas may be used. As an example of the fluorine-containing gas, a NF_3 gas or a SF_6 gas may be used. An example of the hydrocarbon gas may be CH_4 . Further, the gas source group may further include various other gas sources of, for example, a rare gas such as an Ar gas.

[0029] The flow rate controller group 44 includes the N number of flow rate controllers 441 to 446. These flow rate controllers 441 to 446 are configured to control flow rates of the gases supplied from the corresponding gas sources. These flow rate controllers 441 to 446 may be implemented by mass flow controllers (MFC) or FCS. The valve group 42 includes the N number of valves 421 to 426. The gas sources 401 to 406 are connected to a gas supply line 38 via the flow rate controllers 441 to 446 and the valves 421 to 426, respectively. The gases of the gas sources 401 to 406 are supplied into the gas diffusion space 36a via the gas supply line 38 to be discharged into the processing space S through the gas through holes 36b and the gas discharge holes 34a.

[0030] Referring back to FIG. 3, the plasma processing apparatus 10 may further include a grounding conductor 12a. The grounding conductor 12a is of a substantially cylindrical shape and is extended upwards from a sidewall of the processing vessel 12 to a position higher than the upper electrode 30.

[0031] Further, the plasma processing apparatus 10 is also equipped with a deposition shield 46. The deposition shield 46 is detachably provided along an inner wall of the processing vessel 12. The deposition shield 46 is also provided on an outer periphery of the supporting

member 14. The deposition shield 46 suppresses an etching byproduct (deposit) from adhering to the processing vessel 12 and may be made of an aluminum member coated with ceramics such as Y_2O_3 .

[0032] At a bottom portion of the processing vessel 12, a gas exhaust plate 48 is provided between the supporting member 14 and the inner wall of the processing vessel 12. The gas exhaust plate 48 may be made of, by way of example, but not limitation, an aluminum member coated with ceramics such as Y_2O_3 . The processing vessel 12 is also provided with an exhaust port 12e under the gas exhaust plate 38, and the exhaust port 12e is connected with a gas exhaust device 50 via a gas exhaust line 52. The gas exhaust device 50 includes a vacuum pump such as a turbo molecular pump and is capable of depressurizing the inside of the processing vessel 12 to a desired vacuum level. Further, a carry-in/out opening 12g for the wafer W is formed at the sidewall of the processing vessel 12, and this carry-in/out opening 12g is opened or closed by a gate valve 54.

[0033] Further, a conductive member (GND block) 56 is provided on the inner wall of the processing vessel 12. The conductive member 56 is fixed to the inner wall of the processing vessel 12 to be disposed on a substantially level with the wafer W in a height direction. This conductive member 56 is DC-connected to the ground and has an effect of suppressing an abnormal discharge. Further, the position of the conductive member 56 may not be limited to the position shown in FIG. 3 as long as it is provided within a plasma generation region.

[0034] The plasma processing apparatus 10 further includes a first high frequency power supply 62 and a second high frequency power supply 64. The first high frequency power supply 62 is configured to generate a first high frequency power for plasma generation of a frequency ranging from 27 MHz to 100 MHz. As an example, the first high frequency power supply 62

generates a high frequency power having a frequency of 40 MHz. The first high frequency power supply 62 is connected to the lower electrode 16 via a matching unit 66. The matching unit 66 is a circuit for matching an output impedance of the first high frequency power supply 62 with an input impedance on a load side (on the side of the lower electrode 16). The first high frequency power supply 62 may also be connected to the upper electrode 30 via a matching unit 66.

[0035] The second high frequency power supply 64 is configured to generate a second high frequency power for ion attraction into the wafer W, *i.e.*, a high frequency bias power, of a frequency in the range from 400 kHz to 13.56 MHz. As an example, the second high frequency power supply 64 generates a high frequency power of 3 MHz. The second high frequency power supply 64 is connected to the lower electrode 16 via a matching unit 68. The matching unit 68 is a circuit for matching an output impedance of the second high frequency power supply 64 with an input impedance on the load side (on the side of the lower electrode 16).

[0036] Further, the plasma processing apparatus 10 further includes a DC power supply unit 70. The DC power supply unit 70 is connected to the upper electrode 30. The DC power supply unit 70 is configured to generate a negative DC voltage to apply the DC voltage to the upper electrode 30.

[0037] Furthermore, in the exemplary embodiment, the plasma processing apparatus 10 may further include a controller Cnt. The controller Cnt is a computer including a processor, a memory, an input device, a display device, and so forth and is configured to control individual components of the plasma processing apparatus 10. Through the controller Cnt, an operator can input commands or the like to manage the plasma processing apparatus 10 by using the input device of the controller Cnt, and an operational status of the plasma processing apparatus 10 can be visually displayed by the display device. The memory stores therein control programs for

implementing various processes in the plasma processing apparatus 10 under the control of the processor, or programs for implementing a process in each component of the plasma processing apparatus 10 according to processing conditions, *i.e.*, processing recipes.

[0038] To elaborate, the controller Cnt outputs control signals to the flow rate controllers 441 to 446, the valves 421 to 426 and the gas exhaust device 50 to control them such an etching gas is supplied into the processing vessel 12 during an etching process of the process ST2 and, also, an internal pressure of the processing vessel 12 is set to be a predetermined pressure value.

[0039] Further, the controller Cnt may also output control signals to the first and second high frequency power supplies 62 and 64 to supply the high frequency powers from the first and second high frequency power supplies 62 and 64 to the lower electrode 16. In the exemplary embodiment, the controller Cnt may output the control signals to the first and second high frequency power supplies 62 and 64 to supply the high frequency powers to the lower electrode 16 while ON and OFF of the high frequency powers are switched in a pulse shape. In addition, the controller Cnt may also output a control signal to the DC power supply unit 70 to supply a negative DC voltage, which has an absolute value larger than that of a negative DC voltage applied to the upper electrode 30 during a period during which the high frequency powers are ON, to the upper electrode 30 during a period during which the high frequency powers are OFF. Further, an ON-Off frequency of the high frequency powers from the first and second high frequency power supplies 62 and 64 is in the range of, but not limited to, 1 kHz to 40 kHz. Here, the "ON-OFF frequency of the high frequency powers" refers to a frequency having a single cycle composed of an ON period and an OFF period of the high frequency powers of the first and second high frequency power supplies 62 and 64. Further, a duty ratio indicating a ratio of the

ON period of the high frequency powers with respect to the single cycle is, by way of example, but not limitation, in the range from 50% to 90%. Further, the changeover of the DC voltage of the DC power supply unit may be synchronized with the ON-OFF switchover of the high frequency power supplies 62 and 64.

[0040] Referring back to FIG. 1, the description of the method MT will be continued. In the process ST1 (Prepare wafer), the wafer W is prepared within the processing vessel of the plasma processing apparatus. When the plasma processing apparatus 10 is employed, the wafer W placed on the placing table PD is attracted to and held on the electrostatic chuck 18b. Subsequently, the process ST2 of the method MT is performed.

[0041] In the process ST2 (Etch multilayered film), a multilayered film is etched. For the purpose, the processing gas is supplied into the processing vessel of the plasma processing apparatus, and the internal pressure of the processing vessel is set to be a predetermined pressure. In case of using the plasma processing apparatus 10, the processing gas is supplied into the processing vessel 12 from the gas source group 40, and by operating the gas exhaust device 50, the internal pressure of the processing vessel 12 can be set to be the predetermined pressure.

[0042] The processing gas used in the process ST2 includes a hydrogen gas (H_2 gas), a hydrofluorocarbon gas, a fluorine-containing gas, a hydrocarbon gas, a boron trichloride (BCl_3) gas and a nitrogen gas (N_2) gas. An example of the hydrofluorocarbon gas may be a CH_2F_2 gas, a CH_3F gas or a CHF_3 gas; an example of the fluorine-containing gas, a NF_3 gas or a SF_6 gas; and an example of the hydrocarbon gas, CH_4 . Further, the processing gas may further include a rare gas such as an Ar gas.

[0043] In the process ST2, the processing gas supplied into the processing vessel is excited. In case of using the plasma processing apparatus 10, the high frequency powers from

the first and second high frequency power supplies 62 and 64 are applied to the lower electrode 16.

[0044] Various conditions in the process ST2 are as follows.

- Flow rate of H₂ gas: 50 sccm to 300 sccm
- Flow rate of CH₂F₂: 40 sccm to 80 sccm
- Flow rate of NF₃: 50 sccm to 100 sccm
- Flow rate of CH₄: 5 sccm to 50 sccm
- Flow rate of BCl₃: 5 sccm to 30 sccm
- Flow rate of N₂ gas: 10 sccm to 200 sccm
- Frequency of high frequency power of first high frequency power supply 62: 27 MHz to 100 MHz
- High frequency power of first high frequency power supply 62: 500 W to 2700 W
- Frequency of high frequency power of second high frequency power supply 64: 0.4 MHz to 13 MHz
- High frequency power of second high frequency power supply 64: 1000 W to 4000 W
- Pressure within the processing vessel 12: 2.66 Pa to 13.3 Pa (20 mT to 100 mT)

[0045] Further, according to the exemplary embodiment, the ON-OFF switchover of the high frequency powers of the first and second high frequency power supplies 62 and 64 may be performed in a pulse shape. Further, synchronously with the ON-OFF switchover of the high frequency powers of the first and second high frequency power supplies 62 and 64, the magnitude of an absolute value of the negative DC voltage applied to the upper electrode 30 may be switched. In the present exemplary embodiment, plasma is generated while the high frequency powers are ON, and the plasma directly above the wafer W is extinguished while the

high frequency powers are OFF. Furthermore, while the high frequency powers are OFF, positive ions are attracted to collide with the upper electrode 30 by the negative DC voltage applied to the upper electrode 30. Accordingly, secondary electrons are emitted from the upper electrode 30. The emitted secondary electrons modify the mask MSK to improve etching resistance of the mask MSK. Further, the secondary electrons neutralize a charged state of the wafer W. As a result, verticality of ions toward the hole formed in the multilayered film IL is improved. Example conditions regarding the ON-OFF switchover of the high frequency powers of the first and second high frequency power supplies 62 and 64 and conditions for the negative DC voltage applied to the upper electrode 30 are as follows.

- ON-OFF frequency of high frequency powers: 1 kHz to 40 kHz
- Duty ratio of ON-period of high frequency powers with respect to single cycle; 50% to 90%
- Absolute value of negative DC voltage during ON-period of high frequency powers: 150 V to 500 V
- Absolute value of negative DC voltage during OFF-period of high frequency powers: 350 V to 1000 V

[0046] In the process ST2, the processing gas is excited into plasma. By exposing the wafer W to active species of atoms or molecules contained in the processing gas, the multilayered film IL of the wafer W is etched, as illustrated in FIG. 5. Further, during the etching of the process ST2, a deposit DP generated from carbon contained in the processing gas is deposited on the mask MSK. The deposit DP may clog the opening of the mask MSK. However, a thickness of the deposit DP is reduced by nitrogen contained in the processing gas. As a result, the opening of the mask MSK is suppressed from being clogged.

[0047] Further, during the etching in the process ST2, a compound of boron or boron trichloride and atoms constituting the multilayered film, *e.g.*, oxygen and/or nitrogen is generated. As a result, a protective film PF containing the corresponding compound is deposited on a sidewall surface SW forming a space SP in the multilayered film IL. The protective film PF may be nitrified by the nitrogen contained in the processing gas. Accordingly, the protective film PF may have more improved resistance against the active species that contributes to the etching of the multilayered film IL. That is, a stronger protective film PF is formed. As a result, the verticality of the space SP formed in the multilayered film IL can be improved.

[0048] Further, the processing gas used in the process ST2 contains hydrogen, and the mask MSK is modified by the hydrogen. As a consequence, it is possible to maintain the shape of the mask until the etching in the process ST2 is completed. That is, a mask selectivity against the etching of the multilayered film IL can be improved.

[0049] (Experimental examples and comparative examples)

Below, an experimental example conducted by using the method MT and a comparative example conducted for the comparison will be described.

[0050] In the experimental example, the method MT is applied to the wafer W shown in FIG. 2 by using the plasma processing apparatus 10. Meanwhile, in the comparative example, the multilayered film IL of the wafer W shown in FIG. 2 is etched by using a processing gas containing an HBr gas instead of the BCl₃ gas without containing the N₂ gas. Further, the other conditions for the etching of the comparative example are the same as those for the etching of the experimental example.

[0051] For each of the wafers W to which the etching of the experimental example and the etching of the comparative example are applied, respectively, a cross sectional image of the

multilayered film IL in which the space is formed by the etching is acquired, and a shape of the space is observed by using the corresponding cross sectional image. To elaborate, an inclination angle θ and a center line deviation amount D of the space SP are obtained. The inclination angle θ is obtained, as shown in FIG. 6, by measuring an angle between a center line Lp and an imaginary line Li. Here, the center line Lp refers to a central line between a pair of lines Ls that form the space SP, and the imaginary line Li refers to a line that passes through a center of a top opening of the space SP in a vertical direction. The pair of lines Ls corresponds to sidewall surfaces of the multilayered film IL that form both sides of the space SP on the cross sectional image. Further, the center line deviation amount D is obtained, as illustrated in FIG. 7, by measuring distances Ld between the center line Lp and the imaginary line Li in a horizontal direction at different positions and, then, calculating 3σ of those distances Ld. In addition, the inclination angle θ and the center line deviation amount D are obtained at a center position of the wafer W, an edge position thereof and an intermediate position between the center position and the edge position in a diametric direction of the wafer W.

[0052] FIG. 8 shows the inclination angles θ and the center line deviation amounts D obtained in the experimental example and the comparative example. As can be seen from FIG. 8, the inclination angle θ and the center line deviation amount D of the space formed in the comparative example are found to have fairly large values. The reason why the inclination angle θ and the center line deviation amount D of the space in the comparative example are so large is because the protection of the sidewall surfaces of the space by the protective film is not sufficient and the sidewall surfaces thereof in the multilayered film are horizontally etched by ions entering the space in an inclined direction. Further, the reason why the center deviation amount D of the space in the comparative example is large is also because the opening size of the

mask is reduced with the lapse of the etching time and a width of the space is decreased as it goes deep into the multilayered film. Meanwhile, the inclination angle θ and the center line deviation amount D of the space in the experimental example are found to be fairly smaller than the inclination angle θ and the center line deviation amount D of the space in the comparative example. As can be seen from this result, it is found out that by using the processing gas containing BCl_3 gas and N_2 gas instead of HBr gas, the vertically of the space in the multilayered film can be improved while suppressing the opening size of the mask from being reduced.

[0053] From the foregoing, it will be appreciated that various embodiments of the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present disclosure. A plasma processing apparatus is not limited to a capacitively coupled plasma processing apparatus. For example, the plasma processing apparatus may be an inductively coupled plasma processing apparatus or a plasma processing apparatus configured to generate plasma by introducing a microwave into a processing vessel through a waveguide and an antenna. Accordingly, the various embodiments disclosed herein are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

WE CLAIM

1. An etching method of etching a multilayered film including a first film and a second film that have different permittivities and are alternately stacked on top of each other, the etching method comprising:

preparing, within a processing vessel of a plasma processing apparatus, a processing target object having the multilayered film and a mask provided on the multilayered film; and

etching the multilayered film by exciting a processing gas containing a hydrogen gas, a hydrofluorocarbon gas, a fluorine-containing gas, a hydrocarbon gas, a boron trichloride gas and a nitrogen gas within the processing vessel.

2. The etching method of Claim 1,
wherein the hydrofluorocarbon gas is a CH_2F_2 gas, a CH_3F gas or a CHF_3 gas.

3. The etching method of Claim 1,
wherein the fluorine-containing gas is a NF_3 gas or a SF_6 gas.

4. The etching method of Claim 1,
wherein the hydrocarbon gas is a CH_4 gas.

5. The etching method of Claim 1,
wherein the first film is a silicon oxide film, and the second film is a silicon nitride film.

6. The etching method of Claim 1,

wherein the first film is a silicon oxide film, and the second film is a polysilicon film.

7. The etching method of Claim 1,
wherein the first film and the second film are stacked in twenty-four or more layers in total.

8. The etching method of Claim 1,
wherein the mask is made of amorphous carbon.