Description

This invention relates to data processing and data processor controllers in the form of a microprocessor formed on a semiconductor substrate.

Often in a microcomputer system, a large amount of data needs to be transmitted between data input/output equipment such as a CRT terminal, a hard disk or a floppy disk, and a memory, and between memories. When a microprocessor is charged with such data transmission by software, the load on the microprocessor is greatly increased; consequently, the effective capacity of the system decreases.

To cope with this disadvantage, a DMA (direct memory access) controller has been furnished as one item of equipment for controlling data transmission between component elements of the microcomputer. However, since a conventional DMA controller is an LSI (Large-sized integrated circuit) formed separately from the microprocessor, the use of a conventional DMA controller is disadvantageous in that it complicates the construction of a system for DMA transmission. That is, it becomes necessary to mount the microprocessor LSI as well as the DMA controller LSI on a printed wiring board. Further, it is often required to provide a suitable logic IC such as TTL to form an interface between the microprocessor and the DMA controller. This fact causes the construction of board such as wiring substrate to become complex.

The present inventors thought about simplifying the construction of the system by incorporating the function of a DMA controller in a microprocessor LSI. The mere incorporation of the DMA controller in the conventional microprocessor however, markedly increases the chip size of an LSI, thereby creating a possibility of lowering the production yield.

From US-A-4 181 938, a processor device is known which has functions for executing both, a CPU mode and a DMA mode. In this device, an address register stores address data of an external main memory in response to a signal from a microprogram controller. A register group stores data necessary for calculation and includes a command register, a data register and a location register. Address data read from the microprogram controller are supplied to the location register in said register group and through an ALU (arithmetic logic unit) to the main memory. According to this state of the art, common circuits for both, CPU and DMA modes, are only the microprogram controller and in particular a common memory bus controller for the common use of data bus, whereas circuits including the ALU and the register group are for CPU mode only and circuits including a counter and the address register are for DMA mode only.

Starting from the prior art as known from US-A-4 181 938, it is the object of the present invention to improve the function of a microprocessor without greatly increasing the chip size, and thereby to facilitate the construction of a microcomputer system.

Based on the mutual similarity in the construction of the arithmetic execution elements of a microprocessor and a DMA controller, the present invention as described in claims 1 and 9 uses a common arithmetic execution element for the microprocessor and the DMA controller, while adopting a microprogram system as a system for controlling said two devices and thereby integrating a microprogram ROM in one. In other words, said execution element is commonly used for providing address data as well as for performing predetermined microprogram instructions. By this constitution, duplication in a circuitry can be eliminated, and thereby, a highly functional microprocessor having an additional function as a DMA controller, a function which no conventional microprocessors have, can be constructed without an increase in the chip size.

Claims 2 to 8 and 10 include preferable embodiments of the invention.

The present invention will be described by way of example with reference to the drawings, wherein:

Figure 1 shows a schematic construction of an entire LSI in the case when the present invention is adapted to a microprocessor;

Figure 2 is a block diagram showing one embodiment of the construction of the control unit of said LSI;

Figure 3 is a block diagram showing the construction of the control unit in further detail;

Figure 4 is a diagram showing the construction of micro-instruction;

Figure 5 is a diagram showing the construction of micro-instruction;

Figure 6 is a flow chart of micro-instruction;

Figure 7 is a block diagram which concretely illustrates an arithmetic execution unit;

Figure 8 is a block diagram showing another embodiment of the construction of the control unit;

Figure 9 is a block diagram which shows in further detail the construction of the control unit of Fig. 8; and

Figure 10 is a diagram which concretely illustrates the circuit of a read-only memory.

Figure 1 shows schematically a construction of a microprocessor (hereinafter called a CPU) having the function of a DMA controller, to which the present invention is adapted. The part surrounded by a chain line A in the figure is monolithically formed on one integrated semiconductor chip such as a single-crystal

silicon substrate.

This embodiment is designed to take advantage of the following similarities of CPU and the DMA controllers. A DMA controller has, like the CPU, an ALU (arithmetic logic unit) and a counter such as an incrementor or a decrementor for computing a sending-device address and a receiving-device address required for DMA transmission, and for counting the number of transmitted words, respectively. Moreover, both a CPU and a DMA controller are provided with an interface circuit with an address bus and a data bus respectively for providing computed addresses and data to an internal bus and receiving necessary signals from outside. Based on these similarities, an operation execution unit such as arithmetic execution unit 2 is provided to be used commonly by the CPU and the DMA controller, and ALU 3, a counter 4 and a bus interface circuit 5 in the arithmetic execution unit 2 are designed to be used commonly thereby. According to this construction, the respective operations are executed by using the same ALU 3 and counter 4 in a time-sharing manner, while address signals and data signals are interchanged between the common bus interface circuit 5 and an internal bus 6.

A register 7 in the arithmetic execution unit 2 must be provided separately for the CPU and the DMA controller because of the difference in the use thereof for each of them. If a general purpose register is employed, however, it can be used commonly both for the CPU and the DMA controller.

Moreover, in this embodiment, a microprogram control system of simple, logical design and modification is adopted for use as a control system for control elements of the CPU and the DMA controller; furthermore the control element of the CPU and that of the DMA controller are monolithically integrated into one unit to increase efficiency.

The internal bus 6 of the LSI A is coupled to suitable external equipments via an external bus 61. In the apparatus of Fig. 1, the external bus 61 is coupled to a floppy disk controller 62, a communication controller 63, a ROM (read-only memory) 64, and to a RAM (random access memory) 65.

Onto the ROM 64 have been written a macro-instruction that will be executed by the microprocessor, and a control data or fixed data that will be referred to when the macro-instruction is to be executed.

Onto the RAM 65 are written data that are supplied, for example, from the floppy disk controller 62 and the communication controller 63, data that are to be supplied to these controllers 62, 63, and suitable instructions.

The control unit 1 receives DMA transmission request signals REQ 1, REQ 2 from the controllers 62, 63.

The control unit 1 fundamentally operates as described below. The construction and operation of the control unit 1 will be explained later with reference to Fig. 2.

The macro-instruction read out from the ROM 64 in the macro-instruction fetch operation is supplied to the control unit 1 via the external bus 61 and the internal bus 6. Responsive to the macro-instruction that is supplied, a start address of the micro ROM 11 in the control unit is set, and a micro-instruction is read out from the micro ROM 11. The arithmetic execution unit 2 is controlled by the micro-instruction. The micro ROM 11 produces a next address data which indicates a micro-instruction that is to be read out from the micro ROM in the next step. Therefore, micro-instructions are successively read out from the micro ROM 11 at timings determined by signals such as system clock signals, and the arithmetic execution unit 2 is controlled successively by the micro-instructions. Thus, a plurality of micro-instructions are read out for each macro-instruction, and the microprocessor executes its operation.

When a DMA transmission request signal REQ 1 or REQ 2 is produced from an external equipment such as floppy disk controller 62, a start address data for processing the DMA transmission is formed for the micro ROM 11 depending upon the DMA transmission request signal. Responsive thereto, a series of micro-instructions for the DMA transmission are read out from the micro ROM. Therefore, the DMA transmission processing is executed. After the DMA transmission is processed, the microprocessor operation is operated again.

Figure 2 shows one embodiment of a particular configuration of a control unit 1 of Fig. 1 which is integrated as described above.

In this embodiment, a microprogram relating to the operation of the CPU and a microprogram relating to the operation of the DMA controller are stored in a microprogram ROM 11 (hereinafter called a micro ROM) which is used commonly for these two devices. Moreover, registers for holding an address for reading out a micro-instruction relating to the operation of the CPU and an address for reading out a micro-instruction relating to the operation of the DMA controller are provided separately as a DMA ROM address register (DMA RAR) 14b and a CPU ROM address register (CPU RAR) 14a.

Addresses held by ROM address registers 14a and 14b are supplied selectively by a multiplexer 13 to an address decoder 12, whereby a micro-instruction corresponding to the supplied address is read out. Part of the micro-instruction thus read out is held by a micro-instruction register 10 and then supplied as a

microprogram control signal to the arithmetic execution unit 2, without being processed or being decoded. The micro-instruction also contains a next address for reading out a subsequent micro-instruction, and this next address is supplied to multiplexers 15a and 15b, multiplexed with a start address to be described later, and then held by ROM address registers 14a and 14b.

The ROM address registers 14a and 14b are provided separately because an address of a CPU micro-instruction required for a subsequent operation must be held so as to resume a discontinued CPU operation after the completion of DMA transmission which is conducted on the basis of a demand therefor delivered during the course of the operation of the CPU.

This control unit 1 is further provided with an instruction register 16 holding a macro-instruction to the CPU, a DMA control register 17 setting a transmission mode of the DMA controller, and a decoder 18 decoding an output signal of said DMA control register 17 to form a start address.

According to this embodiment, a macro-instruction read from a ROM 64 or the like provided outside the chip, is held by instruction register 16, and then the operation code of said macro-instruction is supplied to the CPU ROM address register 14a through the multiplexer 15a and further supplied selectively to the address decoder 12 by a multiplexer 13. Then, a corresponding word line in the micro ROM 11 is accessed by the address decoder 12, and thereby a first micro-instruction is read out. Subsequently, a next address contained in the read micro-instruction is supplied to the CPU ROM address register 14a through the multiplexer 15a. A series of micro-instructions are read out sequentially in this way to form a control signal, which is supplied to the arithmetic execution unit to execute one macro-instruction.

Fig. 4 shows one example of a construction of the macro-instruction. Though there is no particular limitation, the macro-instruction comprises of a byte of operation code OPC and a subsequent plurality of bytes of operands OPRD 1 to OPRD 2. The number of operands is determined depending upon the operation code OPC. When the operation code OPC consists of one byte, i.e., consists of eight bits, the number of start addresses of the micro ROM 11 that can be set by the macro-instruction becomes a maximum of 256.

Fig. 5 shows a construction of bits of micro-instruction read out from the micro ROM 11.

Though there is no particular limitation, the micro-instruction is comprised of a sequence control field SCF comprising such as nine bits, a bus control field BSCF comprising such as three bits for controlling the internal bus and for controlling buses 20, 21 that will be explained later with reference to Fig. 7, an ALU operation designation field ALUF comprising such as five bits for controlling the ALU operation in the arithmetic execution unit 1, a register input/output designation field RIOCF comprising such as 13 bits for controlling the input and output of various internal registers, conditional branch and flag change designation field CBIF comprising such as five bits for controlling the conditional branch and for controlling the flag that will be described later, and a control field BSOF comprising such as one bit for designating a bus right open timing.

The sequence control field SCF comprises a control field COPF of one bit, and a next address field of a total of eight bits consisting of, for example, a first field NAF and an operation code branch field BRCF.

Fig. 6 is a flow chart of a microprogram.

In a first step STPOO, an operation code OPC in the macro-instruction is fetched to the instruction register 16 of Fig. 2.

The operation code OPC fetched to the instruction register 16 is supplied to the address decoder 12 via multiplexer 15a, address register 14a and multiplexer 13, whereby a start address of the micro ROM 11 is designated. Namely, one of a plurality of microprocessing flows is designated.

If the start address indicates a processing step STPA 1, a micro-instruction which corresponds to the step is read out from the ROM 11. A processing step STPA 2 is designated by a next address that is designated by the step STPA 1. In the same manner, the processing steps are designated successively. After the processing is executed in a final processing step STPA 3 in a process flow, the process (step STPOO) of macro-instruction fetch is performed again.

According to this embodiment, the microprocesses which are equal to each other are commonly executed in the individual microprocess flows. In Fig. 6, the processing step STPBC represents such processing steps that are performed in common. That is, the microporcess STBC is commonly utilized for each of the microporcess flow which consists of microprocesses STPB 1 to STPB 3, and the microprocess flow which consists of STPC 1 to STPC 2.

Though there is no particular limitation, the next address that is to be designated after the common microprocess STPBC is executed, is formed as described below.

That is, in the common microprocess STPBC, bits of operation code branch field may assume such values as "0", "0", "1" in the micro-instructions produced from the micro ROM 11, and a bit in the control field COPF may assume a level such as "1". The level "1" of the control field COPF means to utilize the

macro-instruction.

When the control field COPF assumes "1", the multiplexer 15a is so controlled as the select three bits of the field BRCF together with the macro-instruction consisting of eight bits produced from the instruction register 16. Therefore, the address register 14a is served with the macro-instruction to which the above-mentioned three bits have been added. The thus added three bits are regarded to form a page data. The macro-instruction modified by the additional three bits is regarded to designate a next address that is designated after a common microprocess such as STPB 2 is executed.

Therefore, if the macro-instruction which has been fetched in advance to the instruction register 16 designates a start address which indicates, for example, the microprocess STPB1, the next address that is designated by the execution of common microprocess STPBC is directed to the microprocess STPB 3.

When the operation code branch field BRCF comprises of a plurality of bits as in this embodiment, the common microprocesses are allowed to exist in one microprocess flow in a number designated by the field BRCF or in a number of pages designated by the field BRCF. That is, when it is regarded that the start address of the macro-instruction is designated with the additional bits being, for example "000", the destination after the common microprocess is executed can be any one of seven determined by the additional three bits, i.e., "001" to "111".

The conditional branch processing such as the microprocess STPD 3 of Fig. 6 is executed as described below.

That is, the bits of the field CBIF of Fig. 5 and the flag data produced from the flag register set to the arithmetic execution unit 1 are supplied to a suitable logic circuit which modifies the next address that is supplied from the micro ROM 11. This determines which one of a plurality of branched processes STPD 4, STPD S should be executed.

According to this embodiment, the control unit 1 has several circuits for the DMA transmission as described earlier.

When the operation of the LSI is shifted to DMA transmission, a start address corresponding to a transmission mode set in the DMA control register 17 is supplied from the decoder 18 to the DMA ROM address register 14b through the multiplexer 15b. Then, it is supplied selectively to the address decoder 12 by the multiplexer 13, so that a first micro-instruction for DMA transmission is read out. Subsequently, in the same way as in the operation for CPU, a next address contained in the micro-instruction is held by the DMA ROM address register 14b through the multiplexer 15b, micro-instructions are read out successively, so that the DMA transmission is executed.

Here, though there is no particular limitation, the data written onto the DMA control register 17 or the data supplied to the decoder 18, consist of bits that are constructed as shown in Table 1.

Table 1

	Bit number							
	7	6	5	4	3	2	1	0
Designation of bit	*	*	*	*	DM1	DM0	SM1	SM0

In Table 1 above, bits DM1 and DM0 are regarded to indicate the mode of device on the destination side, and bits SM1 and SM0 are regarded to indicate the mode of device on the source side. The fourth to seventh bits marked with asterisk are non-reference bits.

A combination of two bits, i.e., bits DM1 and DM0, and a combination of two bits, i.e., bits SM1 and SM2, respectively designate the contents as shwon in Table 2.

Table 2

Bit condition		Content
DM1 (SM1)	DM0 (SM0)	
0	0	Memory address increment
0	1	Memory address decrement
1	0	Memory address fixed
1	1	I/O address fixed

According to Table 2 above, when the four bits DM1 to SM0 are set, for example, to "1100", the DMA transmission is designated so that the memory address of the source side increases, and the address of the input/output device of the destination side is fixed.

The address decoder 18 of Fig. 2 decodes the thus coded DMA transmission control data, in order to form start address data consisting of eight bits, that correspond to each of the DMA transmission control data.

Multiplexers 13, 15a and 15b are designed to be switched over by a control signal supplied by a control circuit which receives as an input signal a part of a control signal of the micro-instruction read from the micro ROM 11 or a part of that control signal and another control signal.

In the construction of Fig. 2, though there is no particular limitation, the multiplexers 15a and 15b are controlled for their operation by a control signal 113 produced from the micro ROM 11. When a series of micro-instructions are to be successively read out responsive to a macro-instruction that is fetched to the instruction register 16, and when a series of micro-instructions for the DMA transmission are to be successively read out responsive to a decode signal supplied from the decoder 18, the control signal 113 assumes a level such that the multiplexers 15a, 15b will select the next address data supplied from the micro ROM 11. The control signal 113 further assumes a level such that the multiplexers 15a, 15b will select the output of the instruction register 16 and the output of the decoder 18 when a new macro-instruction is to be executed succeeding the execution of a macro-instruction and when the DMA transmission control is to be newly initiated as a result of reading and executing a suitable micro-instruction.

In Fig. 2, though there is no particular limitation, the control unit 1 has an exchange control logic circuit 19 for controlling the switching between the CPU operation and the DMA transmission operation. When the DMA transmission request signal REQ1 or REQ2 is generated from the external unit such as unit 62 or 63 of Fig. 1, the exchange control logic circuit 19 causes the register 14a to hold the next address of micro-instruction for the CPU operation, causes the register 14b to receive a decode signal of the decoder 18, and further causes the multiplexer 13 to select the output of the register 14b.

Though the internal construction is not diagramed, the exchange control logic circuit 19 includes an input circuit which receives DMA transmission request signals REQ1 and REQ2, a logic circuit which receives the DMA transmission request signals via the above input circuit, and a signal 111 that indicates a bus right open timing produced from the micro ROM 11, and which produces control signals 190, 191 and 192 at a timing determined by the signal 111 when at least eigther one of the DMA transmission request signal REQ 1 or REQ 2 is generated, and a logic circuit which produces a channel designation signal 193 that indicates DMA transmission request source responsive to DMA transmission request signals REQ 1, REQ 2, and signal 111.

When the DMA transmission request signal REQ 1 or REQ 2 is generated, the control signal 190 does not readily change responsive to the signal REQ 1 or REQ 2, but assumes the control level which causes the register 14a to hold the next address data for the CPU operation after the bus right open designation timing signal 111 is produced from the micro ROM 11.

When the DMA transmission request signals are generated, the control signal 191 assumes a control level which causes the register 14b to receive the data after the output of the decoder 18 is selected by the

multiplexer 15b and the timing signal 111 is generated.

Likewisely, the control signal 192 is controlled for its timing of change by the timing signal 111.

According to this embodiment as described above, the timing signal 111 supplied to the exchange control logic circuit 19 is substantially regarded to be a designation signal that indicates whether the DMA transmission operation can be started or not.

The circuit of this embodiment receives the two DMA transmission request signals REQ 1 and REQ 2, and is hence capable of controlling the DMA transmission of two channels.

Though there is no particular limitation, the channel designation signal 193 produced from the exchange control logic circuit 19 is regarded to be a kind of a micro-instruction, and is supplied to the micro-instruction register 10 together with the micro-instruction that is read out from the micro ROM 11. The arithmetic execution unit 2 is provided with a plurality of registers as will be explained later in detail with reference to Fig. 7 for each of the channels for the purpose of DMA transmission for each of the channels. In the DMA transmission operation, the register of which channel will be accessed is determined by the channel designation signal 193.

When the channel designation signal 193 is regarded to be a micro-instruction as in this embodiment, the micro-instructions read out from the micro ROM 11 during the DMA transmission operation need not be distinguished for each of the channels of DMA. In other words, the micro-instruction can be commonly used for each of the channels. This constitution gives the effect that the capacity of the micro ROM 11 can be reduced.

Fig. 3 is a block diagram which illustrates in further detail the control unit which enables the conditional branch to be performed when the micro-program is being executed.

Among the next address data produced from the micro ROM 11, a data 112a that corresponds to the control field CBIF of Fig. 5 is supplied to a branch control logic circuit 80 which is further surved with the output of a flag register 70 provided in the arithmetic execution unit 2.

The branch control logic circuit 80 modifies an address data 110b by making reference to the conditional branch control data supplied from the field CBIF of micro ROM 11 and to the flag data 700 to 701 supplied from the flag register 70. The address data modified by the branch control logic circuit 80 and the address data 110a corresponding to the field NAF of Fig. 5 produced from the micro ROM 11, are supplied as next address data 110 to the multiplexers 14a and 14b of Fig. 2.

Fig. 7 is a block diagram which concretely illustrates the arithmetic execution unit 2.

According to this embodiment, the arithmetic execution unit 2 comprises of registers 71a to 71b which exclusively participate in the CPU operation, registers 72a to 72b which exclusively participate in the DMA transmission operation, and various other circuits such as ALU 3, flag register 70, counter 4, general-purpose registers 73a to 73b, and bus interface circuit 5, that are commonly used for the CPU operation and the DMA transmission operation.

The registers 71a to 71b for CPU operation constitute, for example, accumulators, program counters and stack pointers.

The registers 72a to 72b for DMA transmission operation constitute source address registers, destination address registers, and transmission word number registers, that are provided for each of the DMA channels in a one-to-one manner.

A DMA source address data is set to each of the source address registers, and a DMA destination address data is set to each of the destination registers. The data that indicates the number of words to be transmitted is set to each of the transmission word number registers.

These circuits of the arithmetic execution unit 2 are provided between a read-only bus 20 and a write-only bus 21.

The ALU 3 receives the data to be operated from the circuits via the read-only bus 20, and sends the operated data to the write-only bus 21.

The flag register 70 receives a flag data formed by the ALU 3. According to this embodiment, though there is no particular limitation, the flag data produced from the ALU 3 is directly supplied to the flag register 70 without passing through the write-only bus 21. This constitution enables the circuit to operate quickly. The flag data of the flag register 70 is directly supplied to the branch control logic circuit 80 of Fig. 3, and is further allowed to be read out via the read-only bus 20.

The counter 4 is used for renewing the data of register for program counter and for renewing the data of registers for DMA.

The bus interface circuit 5 is coupled to the internal bus 6. Therefore, the data can be transmitted among the internal bus 6 and the buses 20, 21 in the arithmetic execution unit 2.

Though not specifically limited, the ROM 64 of Fig. 1 stores the preset data for the register for DMA in the arithmetic execution unit 2 and for the DMA control register 17 of Fig. 2. The data are preset to these

registers for DMA by, for example, the CPU operation at the time of starting the system operation.

According to this embodiment, as described above, concentrated control of the CPU and the DMA can be performed by a single micro ROM, the regulation of logic can be attained, and the efficiency of logical design and control operations can be improved.

Figure 8 shows another embodiment of the construction of the above-described control unit 1.

The integrated decoder 12 for macrocommands and next addresses in the foregoing embodiment are separated into decoders 12a and 12b in the present embodiment, and the part of operation code of a macro-instruction fetched by instruction register 16 is put directly in the instruction decoder 12a, from which a first address is read out. Moreover, an output signal of a DMA control register 17 determining a transmission mode is supplied directly to a multiplexer 13 which selectively passes addresses from the CPU ROM address register 14a and the DMA ROM address register 14b which hold said next addresses.

Furthermore, in the present embodiment, decoder 18, in the previous embodiment decoding the output signal of the DMA control register and forming a start address corresponding to a set transmission mode, is integrated with the address decoder 12b which decodes next addresses.

Though there is no particular limitation, output terminals of the decoders 12a and 12b are coupled to the address input lines of the micro ROM 11. Here, the decoders 12a and 12b are selectively operated so that the micro-instructions can be read out from the micro ROM 11 without competition between outputs of the two decoders 12a, 12b. As will be described later, the control signals for controlling the operation of decoders 12a, 12b are formed by the micro ROM 11.

Fig. 9 is a block diagram which concretely illustrates portions of the decoders 12a, 12b, the micro ROM 11, and a circuit connected thereto.

The decoders 12a, 12b have word line drive circuits WD_{a1} to WD_{a2} and WD_{b1} to WD_{b2} of which the output terminals are coupled to the address input lines WL_1 to WL_2 of the micro ROM 11. Each address input line drive circuit comprises of a circuit such as a so-called clocked inverter circuit whose output condition can be controlled.

The micro ROM 11 has a plurality of address input lines WL1 to WL2, a plurality of data lines or bit lines DO1 to DO4 and D11 to D13, as well as a plurality of output determining elements or memory elements positioned at intersecting points of the address input lines and the data lines. Each output determining element comprises, as shown, for example, in Fig. 10, of a MOSFET Qm of which the gate is connected to a address input line and of which the source and drain are connected between a data line and a ground point of the circuit. Each MOSFET Qm has a threshold voltage which is greater than, or smaller than, the level of a data line that will be set when the MOSFET Qm is selected. A load element LD comprising of such as a MOSFET is coupled between each of the data lines and the power source terminal Vcc of the circuit to supply an operation potential to the data lines.

According to this embodiment, the micro ROM 11 is physically constituted as a single ROM. Theoretically, however, the micro ROM 11 is constituted by two ROM's. That is, the micro ROM 11 comprises of a first portion which includes data lines D01 to D04 that will be used when the decoder 12a is operated, and a second portion which includes data lines D11 to D14 that will be used when the decoder 12b is operated.

The micro ROM 11 produces from the first and second portions thereof control signals 114a and 114b to control the operation of address input line drive circuits WD_{a1} to WD_{a2} and WD_{b1} to WD_{b2} of the decoders 12a, 12b, and further produces control signals 115a and 115b to control the operation of the multiplexer 11b.

Fundamentally, the multiplexer 11b is controlled for its operation by the control signals 115a and 115b supplied from the micro ROM, and selects the control signal or the micro-instruction supplied from the first and second portions of the micro ROM 11. If mentioned in further detail, the multiplexer 11b is controlled for its operation by a control signal 115c that is formed responsive to the control signal 115a and 115b. The level of the control signal 115c has been determined in advance by the control signal 115a or 115b that was selected in the preceding operation sequence. As the micro-instruction is read out as described above, the control signal 115c assumes a level for selecting the succeeding micro-instruction.

Though not specifically limited, the micro ROM 11 is so constituted as to produce a plurality of address data that are to be branched at the time of conditional branch. The multiplexer 11b selects a branching address data depending upon flag data 700 to 701 produced from the flag register 70 in the arithmetic execution unit and a conditional branch control signal produced from the micro ROM 11.

According to this embodiment, the number of word lines required for the micro ROM 11 needs be smaller than the number of word lines required for the micro ROM 11 of the first embodiment. Below is considered the case where a micro ROM is constituted having a micro address number of about 300 to 400, each micro-instruction being comprised of about 40 bits. When the micro ROM has a plurality of word

lines corresponded to the micro addresses in a one-to-one manner and data lines corresponded to micro-instruction bits, its pattern will become very oblong on a semiconductor substrate. With the micro ROM being oblong in shape, the corresponding address decoder will assume a pattern that is markedly elongated on a plane. The circuit having such a markedly elongated pattern brings about problem in laying out circuits of other kinds and with regard to wiring lengths. In the case of the second embodiment, however, the micro ROM 11 and the decoders 12a, 12b are prevented from having extremely elongated patterns.

The control unit 1 of Fig. 8 has the exchange control logic circuit 19 like in the first embodiment.

When the DMA transmission request signal REQ 1 or REQ 2 is generated and when the bus right open timing designation signal 111 is generated, the exchange control logic circuit 19 supplies a control signal 192 to the multiplexer 13 to select the output of the DMA control register 17 for only a predetermined clock period.

In this construction, the multiplexer 13 interrupts the outputs of the ROM address registers 14a and 14b immediately after the shift to DMA transmission and supplies the output of the DMA control register 17 to the address decoder 12b. Then, a first micro-instruction for the DMA transmission is read out of the micro ROM 11, and a next address contained in this instruction is fetched by the DMA ROM address register 14b. Thereafter, a series of micro-instructions are read out successively by next addresses, so that the DMA transmission is executed.

The DMA operation control signals written onto the DMA control register 17 may have been coded as shown in Tables 1 and 2 described earlier. In this case, the circuit is so constituted that a coded 4-bit data produced from the DMA control register 17 immediately after the shift to DMA transmission and a 4-bit data of the address register 14b are selected by the multiplexer 13. Namely, the 4-bit data supplied from the address register 14b is regarded to be a data that designates the fundamental step of the microprogram, and the 4-bit data supplied from the DMA control register 17 is regarded to be a data that designates the detailed steps in the fundamental step.

In the construction of the control unit of the embodiment shown in Fig. 2 the multiplexers 13, 15a and 15b are provided in front and the rear of the ROM address registers 14a and 14b respectively, and this circuit arrangement causes disadvantages in that the logical structure is complicated, the number of gated steps is increased and the speed of operation is somewhat decreased. In contrast to this, the control unit of the embodiment shown in Fig. 8 has the advantage of high operating speed because it has fewer multiplexers.

The present embodiment is constructed to have two separate decoders. However, the size of the circuitry which these decoders add is not considerably different from that including the address decoder in Fig. 2.

Moreover, in this embodiment, a branch condition contained in the sequence control field of a micro-instruction containing a next address is supplied from the CPU ROM address register 14a to instruction decoder 12a so as to form a branch address together with the operation code of a macro-instruction, although the invention is not limited to this configuration. Accordingly, even when the same macro-instruction is fetched, different processes can be executed according to the state of the CPU, and micro-instructions can thus be made common, so as not to require an increase in the size of the micro ROM.

That is, the address register 14a supplies to the decoder 12a an address data 140 which is substantially equal to the 3-bit page data of the aforementioned first embodiment.

When a common microprocess is executed such as the micro process STPBC in the microprocess flow of Fig. 6, the decoder 12a is operated. The decoder 12a decodes the micro-instruction comprising of 8 bits and the data comprising of additional bits 140, and, as a result, selects a word line that corresponds to a return address of the micro ROM 11.

In the above-described embodiments, the operations of the CPU and the DMA are performed by using the arithmetic execution and a bus in a time-sharing manner; consequently, complete parallel processing of the CPU and the DMA is impossible. However, no extreme decrease in the speed of operation is caused thereby, because the time during which the CPU performs an internal operation while the DMA controller executes data transmission during parallel processing accounts for only a few percent of all cycles even in a conventional system having the construction in which the CPU and the DMA controller are separate from each other. Furthermore, the present embodiments enable the elimination of overhead time required for DMA transmission demand signals and acknowledge signals to be interchanged between chips (LSIs), which is required when the CPU and the DMA controller are formed of a multichip. In addition, the present embodiments have an advantage of enabling an increase in a signal speed as well as a reduction in chip size thereby improving the speed of processing of the entire system, compared with a construction in which the CPU and the DMA controller are formed separately on the same chip, which results in an increase in the delay time of a signal due to the increased length of signal lines for connection between blocks and a

bus.

The above description refers to the embodiments having the construction in which the CPU and the DMA controller are integrated on the same chip. Note that a dynamic RAM refresh circuit may also be incorporated into an entity containing the functions of the CPU and the DMA controller, so as to be integrated with these functions.

The above description also refers to the embodiments in which the functions of the CPU and the DMA controller are provided on the same chip. Another construction may be adopted, in this connection, in which a circuit having a function of controlling peripheral devices, such as a hard-disk controller, if formed in place of the DMA controller or together with it on the same chip in such a manner that it uses the common arithmetic execution unit and the integrated control unit.

Since the arithmetic execution unit is used in common with the microprocessor and the DMA controller, and the microprogram system is employed to control these devices to permit the respective microprogram ROMs to be integrated, duplication of circuit components is eliminated, thereby improving the function of the microprocessor without greatly increasing the chip size, and also simplifying the construction of the microcomputer system.

While a microprogram control system is adapted for the control unit in the above-described embodiments, for instance, it is also possible to form the control unit of a random logic circuit with the arithmetic execution unit used in common.

In the above detailed description, the invention is described mainly with reference to the case in which CPU and the DMA controller, which is the field of utilization discussed in the background of the invention, are made to be on a single chip. This invention is not limited, of course, to this case, but it can be utilized for control LSIs in general, including the case where controllers for peripheral devices, such as the DMA controller or a the hard-disk controller, are made to be on a single chip.

Claims

1. A microprocessor on a semiconductor chip, comprising:

memory means (11) for storing a plurality of micro-instructions including first micro-instructions for executing a predetermined macro instruction, said first micro-instructions having a predetermined start address, and second micro-instructions for executing a DMA transmission, wherein said first micro-instructions each includes an address field containing next address data indicating the next address at which a first micro-instruction to be subsequently read out from said memory means (11) is stored, and a control field containing control data for controlling operation execution means (2);

means (12) coupled to said memory means (11) for addressing the memory means (11); and

address providing means coupled to said means (12) and including first means (16) responsive to said predetermined macro instruction for providing said predetermined start address, first storing means (14a) for storing the next address data of a first micro-instruction read out from said memory means (11), second storing means (14b) responsive to a request signal for providing DMA address data indicating a second micro-instruction, and control means (13) coupled to said first storing means (14a) and to said second storing means (14b) and for providing said DMA address data instead of said next address data in response to said request signal; characterised in that

said operation execution means (2) includes, a first circuit (72a, 72b) which exclusively participates in the execution of said DMA transmission, a second circuit (71a, 71b) which exclusively participates in the execution of said predetermined macro instruction, and a third circuit (3, 4, 5, 70, 73a, 73b) which is commonly used for the execution of said DMA transmission and said predetermined macro instruction.

2. A microprocessor according to claim 1, wherein said control means includes a switching means (13) having input terminals coupled to receive said next address data and to receive the DMA address data, respectively, and an output terminal coupled to said means (12), and wherein said switching means (13) provides the DMA address data upon receipt of said request signal.

3. A microprocessor according to claim 2, wherein said control means further includes a control circuit (19) receiving said request signal, said control circuit providing at a first output terminal thereof a first control signal (192) for controlling said switching means (13), and at a second output terminal thereof a second control signal (191) for controlling said second storing means (14b).

4. A microprocessor according to claim 1, wherein said next address data that is stored in said first storing means (14a) at the time when said DMA address data is supplied to said means (12) is supplied

* C L M S *

bus.

The above description refers to the embodiments having the construction in which the CPU and the DMA controller are integrated on the same chip. Note that a dynamic RAM refresh circuit may also be incorporated into an entity containing the functions of the CPU and the DMA controller, so as to be integrated with these functions.

The above description also refers to the embodiments in which the functions of the CPU and the DMA controller are provided on the same chip. Another construction may be adopted, in this connection, in which a circuit having a function of controlling peripheral devices, such as a hard-disk controller, if formed in place of the DMA controller or together with it on the same chip in such a manner that it uses the common arithmetic execution unit and the integrated control unit.

Since the arithmetic execution unit is used in common with the microprocessor and the DMA controller, and the microprogram system is employed to control these devices to permit the respective microprogram ROMs to be integrated, duplication of circuit components is eliminated, thereby improving the function of the microprocessor without greatly increasing the chip size, and also simplifying the construction of the microcomputer system.

While a microprogram control system is adapted for the control unit in the above-described embodiments, for instance, it is also possible to form the control unit of a random logic circuit with the arithmetic execution unit used in common.

In the above detailed description, the invention is described mainly with reference to the case in which CPU and the DMA controller, which is the field of utilization discussed in the background of the invention, are made to be on a single chip. This invention is not limited, of course, to this case, but it can be utilized for control LSIs in general, including the case where controllers for peripheral devices, such as the DMA controller or a the hard-disk controller, are made to be on a single chip.

Claims

1. A microprocessor on a semiconductor chip, comprising:

memory means (11) for storing a plurality of micro-instructions including first micro-instructions for executing a predetermined macro instruction, said first micro-instructions having a predetermined start address, and second micro-instructions for executing a DMA transmission, wherein said first micro-instructions each includes an address field containing next address data indicating the next address at which a first micro-instruction to be subsequently read out from said memory means (11) is stored, and a control field containing control data for controlling operation execution means (2);

means (12) coupled to said memory means (11) for addressing the memory means (11); and

address providing means coupled to said means (12) and including first means (16) responsive to said predetermined macro instruction for providing said predetermined start address, first storing means (14a) for storing the next address data of a first micro-instruction read out from said memory means (11), second storing means (14b) responsive to a request signal for providing DMA address data indicating a second micro-instruction, and control means (13) coupled to said first storing means (14a) and to said second storing means (14b) and for providing said DMA address data instead of said next address data in response to said request signal; characterised in that

said operation execution means (2) includes, a first circuit (72a, 72b) which exclusively participates in the execution of said DMA transmission, a second circuit (71a, 71b) which exclusively participates in the execution of said predetermined macro instruction, and a third circuit (3, 4, 5, 70, 73a, 73b) which is commonly used for the execution of said DMA transmission and said predetermined macro instruction.

2. A microprocessor according to claim 1, wherein said control means includes a switching means (13) having input terminals coupled to receive said next address data and to receive the DMA address data, respectively, and an output terminal coupled to said means (12), and wherein said switching means (13) provides the DMA address data upon receipt of said request signal.

3. A microprocessor according to claim 2, wherein said control means further includes a control circuit (19) receiving said request signal, said control circuit providing at a first output terminal thereof a first control signal (192) for controlling said switching means (13), and at a second output terminal thereof a second control signal (191) for controlling said second storing means (14b).

4. A microprocessor according to claim 1, wherein said next address data that is stored in said first storing means (14a) at the time when said DMA address data is supplied to said means (12) is supplied

* C L M S *

to said means (12) after completion of said DMA transmission so as to completely execute said predetermined macro instruction.

5. A microprocessor according to claim 3, wherein said means (12) comprises a first addressing circuit (12a) and a second addressing circuit (12b),
said first addressing circuit (12a) having inputs coupled to said first means (16), and
said second addressing circuit (12b) having inputs coupled to said switching means (13).

6. A microprocessor according to claim 5, wherein said memory means (11) includes word lines (WL1, WL2), data lines having first lines (D01 to D04) and second lines (D11 to D14), memory elements (Qm) coupled to said word lines (WL1, WL2) and to said data lines (D01 to D04, D11 to D14) so that each memory element is coupled to a word line and to a data line, and output selecting means (11b) coupled to said data lines for outputting output data according to one of either data on said first lines (D01 to D04) or data on said second lines (D11 to D14),
wherein said first and second addressing circuits (12a, 12b) are coupled to said word lines (WL1, WL2) so that each word line is coupled to both said first means (12a) and said second means (12b),
wherein said output selecting means (11b) outputs the output data according to the data on the first lines (D01 to D04) when the first addressing circuit (12a) is operated, and
wherein said output selecting means (11b) outputs the output data according to the data on the second lines (D11 to D14) when the second addressing circuit (12b) is operated.

7. A microprocessor according to claim 6, wherein said output selecting means includes first switching circuits (CIV2) coupled to said first lines (D01 to D04) and second switching circuits (CIV1) coupled to said second lines (D11 to D14).

8. A microprocessor according to claim 3, wherein said request signal (REQ1, REQ2) is supplied from an external controller (62, 63) to be coupled to said microprocessor.

9. A process for use with a data processing system including an external bus (61), a microprocessor (CPU) coupled to the bus (61), a program memory (64) coupled to the bus (61) for storing a predetermined program containing a macro-instruction to be executed by the microprocessor (CPU), a peripheral controller (62, 63) coupled to the bus (61), and a data memory (65) coupled to the bus (61) for storing data to be supplied to or from the peripheral controller (62, 63), the microprocessor (CPU) including an execution unit (2) and control means (1) for controlling operation of the execution unit (2), the control means including a memory (11) which stores first micro-instructions to be executed when the microprocessor (CPU) performs the macro-instruction, and second micro-instructions to be executed when a data transfer between the peripheral controller (62, 63) and the data memory (65) is performed, the process for controlling the execution unit (2) in the microprocessor (CPU) comprising the steps of:
(a) fetching the macro-instruction from the program memory (64) to the microprocessor (1);
(b) addressing the memory (11), in response to an indication of the macro-instruction, to read one of the first micro-instructions;
(c) controlling the execution unit (2) in accordance with control data contained in the first micro-instruction obtained, said control data being operative on second and third circuits of the execution unit, with said second circuit exclusively participating in the execution of said macro-instruction and said third circuit being commonly used for the execution of said DMA transmission and said predetermined macro-instruction;
(d) accessing the memory (11), in response to address data contained in the first micro-instruction obtained, to read the next first micro-instruction from the memory (11);
(e) repeating the steps (c) and (d) until all the first micro-instructions are executed, if the peripheral controller (62, 63) does not provide to the microprocessor (CPU) a request signal (REQ1; REQ2) indicating that a data transfer have been requested;
(f) holding the address data in a register (14a) to discontinue the step (d) if the peripheral controller (62, 63) provides the request signal (REQ1; REQ2) to the microprocessor (CPU);
(g) accessing the memory (11), in response to the reception of the request signal (REQ1; REQ2), to read one of the second micro-instructions;
(h) controlling the execution unit (2), in accordance with control data contained in the second micro-instruction obtained, said control data being operative on first and third circuits of the execution unit,

* C L M S *

with said first circuit exclusively participating in the execution of said DMA transmission and said third circuit being commonly used for the execution of said DMA transmission and said predetermined macro-instruction;
(i) accessing the memory (11) in response to address data contained in the second micro-instruction obtained;
(j) repeating steps (h) and (i) until all the second micro-instructions are performed; and
(k) accessing the memory (11) by using the address data held in the register (14a) in response to completion of the data transfer and returning to step (c).

10. The process of claim 9, wherein the step (h) includes providing address signals from the microprocessor to the data memory (65) via the bus (61) in response to operation of the execution unit (2).

Revendications

1. Microprocesseur disposé sur une plaquette à semiconducteurs, comprenant :
des moyens de mémoire (11) servant à mémoriser une pluralité de micro-instructions contenant des premières micro-instructions pour l'exécution d'une macro-instruction prédéterminée, lesdites premières micro-instructions possédant une adresse de départ prédéterminée, et des secondes micro-instructions pour l'exécution d'une transmission DMA, lesdites premières micro-instructions comprenant chacune une zone d'adresse contenant des données indiquant l'adresse suivante, à laquelle est mémorisée une première micro-instruction devant être lue ultérieurement à partir desdits moyens de mémoire (11), et une zone de commande contenant des données de commande pour la commande de moyens (2) d'exécution d'opérations;
des moyens (12) accouplés auxdits moyens de mémoire (11) pour adresser les moyens de mémoire (11); et
des moyens de délivrance d'adresses accouplés auxdits moyens (12) et comprenant des premiers moyens (16) répondant à ladite macro-instruction prédéterminée pour délivrer ladite adresse de départ prédéterminée, des premiers moyens de mémoire (14a) pour mémoriser la donnée d'adresse suivante d'une première micro-instruction lue à partir desdits moyens de mémoire (11), des seconds moyens de mémoire (14b) répondant à un signal de demande pour délivrer une donnée d'adresse (DMA) indiquant une seconde micro-instruction, et des moyens de commande (13) accouplés auxdits premiers moyens de mémoire (14a) et auxdits seconds moyens de mémoire (14b) et servant à délivrer ladite donnée d'adresse DMA à la place de ladite donnée d'adresse suivante, en réponse audit signal de demande;
caractérisé en ce que
lesdits moyens (2) d'exécution d'opérations comprennent un premier circuit (72a,72b), qui participe exclusivement à l'exécution de ladite transmission DMA, un second circuit (71a,71b), qui participe exclusivement à l'exécution de ladite macro-instruction prédéterminée, et un troisième circuit (3,4,5,70,73a,73b), qui est utilisé habituellement pour l'exécution de ladite transmission DMA et de ladite macro-instruction prédéterminée.

2. Microprocesseur selon la revendication 1, dans lequel lesdits moyens de commande comprennent des moyens de commutation (13) possédant des bornes d'entrée accouplées respectivement de manière à recevoir ladite donnée d'adresse suivante et à recevoir la donnée d'adresse DMA, et une borne de sortie accouplée auxdits moyens (12), et dans laquelle lesdits moyens de commutation (13) délivrent la donnée d'adresse DMA lors de la réception dudit signal de demande.

3. Microprocesseur selon la revendication 2, dans lequel lesdits moyens de commande comprennent en outre un circuit de commande (19) recevant ledit signal de demande, ledit circuit de commande délivrant, au niveau d'une première borne de sortie, un premier signal de commande (192) pour commander lesdits moyens de commutation (13), et, sur une seconde borne de sortie, un second signal de commande (191) pour commander lesdits seconds moyens de mémoire (14b).

4. Microprocesseur selon la revendication 1, dans lequel ladite donnée d'adresse suivante est mémorisée dans lesdits premiers moyens de mémoire (14a) au moment où ladite donnée d'adresse DMA est envoyée auxdits moyens (12) après achèvement de ladite transmission DMA, de manière à exécuter complètement ladite macro-instruction prédéterminée.

5. Microprocesseur selon la revendication 3, dans lequel lesdits moyens (12) comprennent un premier

* C L M S *

circuit d'adressage (12a) et un second circuit d'adressage (12b),

ledit premier circuit d'adressage (12a) comportant des entrées accouplées auxdits premiers moyens (16), et

ledit second circuit d'adressage (12b) comportant des entrées accouplées auxdits moyens de commutation (13).

6. Microprocesseur selon la revendication 5, dans lequel lesdits moyens de mémoire (11) comprennent des lignes de transmission de mots (WL1,WL2), des lignes de transmission de données possédant des premières lignes (DO1 à DO4) et des secondes lignes (D11 à D14), des éléments de mémoire (Qm) accouplés auxdites lignes de transmission de mots (WL1,WL2) et auxdites lignes de transmission de données (D01 à D04, D11 à D14) de sorte que chaque élément de mémoire est accouplé à une ligne de transmission de mots et à une ligne de transmission de données, et des moyens (11b) de sélection de sortie accouplés auxdites lignes de transmission de données pour délivrer des données de sortie conformément à l'une des données présentes dans lesdites premières lignes (D01 à D04) ou des données présentes dans lesdites secondes lignes (D11 à D14),

lesdits premier et second circuits d'adressage (12a,12b) étant accouplés auxdites lignes de transmission de mots (WL1,WL2) de sorte que chaque ligne de transmission de mots est accouplée à la fois auxdits premiers moyens (12a) et auxdits seconds moyens (12b),

lesdits moyens de sélection de sortie (11b) délivrant les données de sortie en fonction des données présentes dans les premières lignes (D01 à D04) lorsque le premier circuit d'adressage (12a) fonctionne, et

lesdits moyens de sélection de sortie (11b) délivrant les données de sortie en fonction des données présentes dans les secondes lignes (D11 à D14) lorsque le second circuit d'adressage (12b) fonctionne.

7. Microprocesseur selon la revendication 6, dans lequel lesdits moyens de sélection de sortie comprennent des premiers circuits de commutation (CIV2) accouplés auxdites premières lignes (D01 à D04) et des seconds circuits de commutation (CIV1) accouplés auxdites secondes lignes (D11 à D14).

8. Microprocesseur selon la revendication 3, dans lequel ledit signal de demande (REQ1,REQ2) est délivré par un contrôleur extérieur (62,63) pour être envoyé audit microprocesseur.

9. Procédé destiné à être utilisé avec un système de traitement de données comprenant un bus externe (61), un microprocesseur (CPU) accouplé au bus (61), une mémoire de programme (64) accouplée au bus (61) pour la mémorisation d'un programme prédéterminé contenant une macro-instruction devant être exécutée par le microprocesseur (CPU), un contrôleur périphérique (62,63) accouplé au bus (61), et une mémoire de données (65) accouplée au bus (61) pour la mémorisation de données devant être envoyées à ou provenant du contrôleur périphérique (62,63), le microprocesseur (CPU) comprenant une unité d'exécution (2) et des moyens de commande (1) pour commander le fonctionnement de l'unité d'exécution (2), les moyens de commande comprenant une mémoire (11), qui mémorise les premières micro-instructions devant être exécutées lorsque le microprocesseur (CPU) exécute la macro-instruction, et les secondes micro-instructions devant être exécutées lorsqu'un transfert de données est exécuté entre le contrôleur périphérique (62,63) et la mémoire de données (65), le processus servant à commander l'unité d'exécution (2) dans le microprocesseur (CPU) comprenant les étapes consistant à :

(a) extraire la macro-instruction de la mémoire de programmes (64) pour l'envoyer au microprocesseur (1);

(b) adresser la mémoire (11), en réponse à une indication de la macro-instruction, pour lire l'une des premières micro-instructions;

(c) commander l'unité d'exécution (2) en fonction des données de commande contenues dans la première micro-instruction obtenue, lesdites données de commande étant à même d'agir sur des second et troisième circuits de l'unité d'exécution, ledit second circuit participant exclusivement à l'exécution de ladite macro-instruction et ledit troisième circuit étant utilisé habituellement pour l'exécution de ladite transmission DMA et de ladite macro-instruction prédéterminée;

(d) accéder à la mémoire (11), en réponse à une donnée d'adresse contenue dans la première micro-instruction obtenue, pour lire la première micro-instruction suivante à partir de la mémoire (11);

(e) répéter les étapes (c) et (d) jusqu'à ce que toutes les premières micro-instructions soient

* C L M S *

exécutées, si le contrôleur périphérique (62,63) n'envoie pas au microprocesseur (CPU) un signal de demande (REQ1; REQ2) indiquant qu'un transfert de données a été demandé;
(f) conserver les données d'adresses dans un registre (14a) pour interrompre l'étape (d) si le contrôleur périphérique (62,63) envoie le signal de demande (REQ1; REQ2) au microprocesseur (CPU);
(g) accéder à la mémoire (11), en réponse à la réception du signal de demande (REQ1; REQ2), pour lire l'une des secondes micro-instructions;
(h) commander l'unité d'exécution (2), en fonction des données de commande contenues dans la seconde micro-instruction obtenue, lesdites données de commande étant aptes à agir sur les premier et troisième circuits de l'unité d'exécution, ledit premier circuit participant exclusivement à l'exécution de ladite transmission DMA et ledit troisième circuit étant habituellement utilisé pour l'exécution de ladite transmission DMA et de ladite macro-instruction prédéterminée;
(i) accéder à la mémoire (11) en réponse aux données d'adresses contenues dans la seconde micro-instruction obtenue;
(j) répéter les étapes (h) et (i) jusqu'à ce que la totalité des secondes micro-instructions soit exécutée; et
(k) accéder à la mémoire (11) en utilisant les données d'adresses conservées dans le registre (14a) en réponse à l'achèvement du transfert des données et, revenir à l'étape (c).

10. Procédé selon la revendication 9, selon lequel l'étape (h) inclut l'envoi de signaux d'adresses du microprocesseur à la mémoire de données (65) par l'intermédiaire du bus (61) en réponse au fonctionnement de l'unité d'exécution (2).

Patentansprüche

1. Mikroprozessor auf einem Halbleiterchip, umfassend
eine Speichereinrichtung (11) zur Speicherung mehrerer Mikrobefehle einschließlich erster Mikrobefehle zur Ausführung eines vorbestimmten Makrobefehls, wobei die ersten Mikrobefehle eine vorbestimmte Anfangsadresse aufweisen, und zweiter Mikrobefehle zur Ausführung einer DMA-Übertragung, wobei jeder erste Mikrobefehl ein Adressenfeld mit einer Folgeadreßinformation, die die nächste Adresse angibt, an der ein anschließend aus der Speichereinrichtung (11) zu lesender erster Mikrobefehl gespeichert ist, sowie ein Steuerfeld mit Steuerdaten zur Steuerung einer Operations-Ausführeinrichtung (2) enthält,
eine mit der Speichereinrichtung (11) verbundene Einrichtung (12) zum Adressieren der Speichereinrichtung (11), und
eine mit der Einrichtung (12) verbundene Adressen-Bereitstelleinrichtung, die eine auf den vorbestimmten Makrobefehl ansprechende erste Einrichtung (16) zur Bereitstellung der vorbestimmten Anfangsadresse, eine erste Speichereinrichtung (14a) zur Speicherung der Folgeadreßinformation eines aus der Speichereinrichtung (11) ausgelesenen ersten Mikrobefehls, eine auf ein Anforderungssignal ansprechende zweite Speichereinrichtung (14b) zur Bereitstellung einer DMA-Adreßinformation, die einen zweiten Mikrobefehl angibt, und eine mit der ersten Speichereinrichtung (14a) und der zweiten Speichereinrichtung (14b) gekoppelte Steuereinrichtung (13) umfaßt, die bei Auftreten des Anforderungssignals anstelle der Folgeadreßinformation die DMA-Adreßinformation bereitstellt,
dadurch gekennzeichnet, daß die Operations-Ausführeinrichtung (2) eine erste Schaltung (72a, 72b), die ausschließlich an der Ausführung der DMA-Übertragung beteiligt ist, eine zweite Schaltung (71a, 71b), die ausschließlich an der Ausführung des vorbestimmten Makrobefehls beteiligt ist, und eine dritte Schaltung (3, 4, 5, 70, 73a, 73b) umfaßt, die für die Ausführung der DMA-Übertragung und des vorbestimmten Makrobefehls gemeinsam verwendet wird.

2. Mikroprozessor nach Anspruch 1, wobei die Steuereinrichtung eine Schalteinrichtung (13) mit Eingangsklemmen, die zum Empfang der Folgeadreß- bzw. der DMA-Adreßinformation angeschlossen sind, und einer mit der besagten Einrichtung (12) verbundenen Ausgangsklemme aufweist und die DMA-Adreßinformation bei Empfang des Anforderungssignals bereitstellt.

3. Mikroprozessor nach Anspruch 2, wobei die Steuereinrichtung ferner eine Steuerschaltung (19) zum Empfang des Anforderungssignals umfaßt, wobei die Steuerschaltung an einer ersten Ausgangsklemme ein erstes Steuersignal (192) zur Steuerung der Schalteinrichtung (13) und an einer zweiten Ausgangsklemme ein zweites Steuersignal (191) zur Steuerung der zweiten Speichereinrichtung (14b) liefert.

4. Mikroprozessor nach Anspruch 1, wobei die Folgeadreßinformation, die in der ersten Speichereinrichtung (14a) zu dem Zeitpunkt gespeichert ist, zu dem die DMA-Adreßinformation der besagten Einrichtung (12) zugeführt wird, nach Beendigung der DMA-Übertragung der besagten Einrichtung (12) zugeführt wird, um den vorbestimmten Makrobefehl vollständig auszuführen.

5. Mikroprozessor nach Anspruch 3, wobei die besagte Einrichtung (12) eine erste Adressierschaltung (12a) und eine zweite Adressierschaltung (12b) umfaßt,
wobei die erste Adressierschaltung (12a) an die erste Einrichtung (16) angeschlossene Eingänge und
die zweite Adressierschaltung (12b) an die Schalteinrichtung (13) angeschlossene Eingänge aufweist.

6. Mikroprozessor nach Anspruch 5, wobei die Speichereinrichtung (11) Wortleitungen (WL1, WL2), Datenleitungen mit ersten Leitungen (D01 bis D04) und zweiten Leitungen (D11 bis D14), Speicherelemente (Qm), die mit den Wortleitungen (WL1, WL2) und den Datenleitungen (D01 bis D04, D11 bis D14) derart gekoppelt sind, daß jedes Speicherelement mit einer Wortleitung und mit einer Datenleitung verbunden ist, sowie eine mit den Datenleitungen verbundene Ausgangs-Wähleinrichtung (11b) zur Ausgabe von Ausgangsdaten entsprechend entweder den Daten auf den ersten Leitungen (D01 bis D04) oder Daten auf den zweiten Leitungen (D11 bis D14) umfaßt,
wobei die erste und die zweite Adressierschaltung (12a, 12b) derart mit den Wortleitungen (WL1, WL2) gekoppelt sind, daß jede Wortleitung sowohl mit der ersten Einrichtung (12a) als auch mit der zweiten Einrichtung (12b) verbunden ist,
wobei die Ausgangs-Wähleinrichtung (11b) die Ausgangsdaten entsprechend den Daten auf den ersten Leitungen (D01 bis D04) ausgibt, wenn die erste Adressierschaltung (12a) in Betrieb ist, und
wobei die Ausgangs-Wähleinrichtung (11b) die Ausgangsdaten entsprechend den Daten auf den zweiten Leitungen (D11 bis D14) ausgibt, wenn die zweite Adressierschaltung (12b) in Betrieb ist.

7. Mikroprozessor nach Anspruch 6, wobei die Ausgangs-Wähleinrichtung an die ersten Leitungen (D01 bis D04) angeschlossene erste Schaltkreise (CIV2) sowie an die zweiten Leitungen (D11 bis D14 angeschlossene zweite Schaltkreise (CIV1) umfaßt.

8. Mikroprozessor nach Anspruch 3, wobei das Anforderungssignal (REQ1, REQ2) von einer externen Steuerung (62, 63) zur Zuführung an den Mikroprozessor geführt wird.

9. Verfahren zur Verwendung bei einem Datenverarbeitungssystem, das eine externe Sammelleitung (61), einen mit dieser verbundenen Mikroprozessor (CPU), einen mit der Sammelleitung (61) verbundenen Programmspeicher (64) zur Speicherung eines vorgegebenen Programms, das einen von dem Mikroprozessor (CPU) auszuführenden Makrobefehl enthält, eine mit der Sammelleitung (61) verbundene Peripheriesteuerung (62, 63) und einen mit der Sammelleitung (61) verbundenen Datenspeicher (65) zur Speicherung von an die Peripheriesteuerung (62, 63) bzw. von ihr zuzuführenden Daten umfaßt, wobei der Mikroprozessor (CPU) eine Ausführeinheit (2) und eine Steuereinrichtung (1) zur Steuerung der Arbeitsweise der Ausführeinheit (2) umfaßt, die Steuereinrichtung einen Speicher (11) aufweist, der erste auszuführende Mikrobefehle speichert, wenn der Mikroprozessor (CPU) den Makrobefehl ausführt, und der zweite auszuführende Mikrobefehle speichert, wenn zwischen der Peripheriesteuerung (62, 63) und dem Datenspeicher (65) eine Datenübertragung stattfindet, wobei das Verfahren zur Steuerung der Ausführeinheit (2) in dem Mikroprozessor (CPU) folgende Schritte umfaßt:
(a) Abrufen des Makrobefehls aus dem Programmspeicher (64) in den Mikroprozessor (1),
(b) Adressieren des Speichers (11) entsprechend einer Angabe des Makrobefehls, so daß einer der ersten Mikrobefehle gelesen wird,
(c) Steuern der Ausführeinrichtung (2) entsprechend Steuerdaten, die in dem ersten erhaltenen Mikrobefehl enthalten sind, wobei die Steuerdaten auf zweite und dritte Schaltungen in der Ausführeinheit einwirken, die zweite Schaltung ausschließlich an der Ausführung des Makrobefehls beteiligt ist und die dritte Schaltung für die Ausführung der DMA-Übertragung und des vorbestimmten Makrobefehls gemeinsam verwendet wird,
(d) Zugriffnahme zu dem Speicher (11) entsprechend Adreßdaten, die in dem ersten erhaltenen Mikrobefehl enthalten sind, zum Auslesen des nächsten ersten Mikrobefehls aus dem Speicher (11),
(e) Wiederholen der Schritte (c) und (d), bis sämtliche erste Mikrobefehle ausgeführt sind, falls die Peripheriesteuerung (62, 63) dem Mikroprozessor (CPU) nicht ein Anforderungssingal (REQ1; REQ2)

* C L M S *

zuführt, das die Anforderung einer Datenübertragung anzeigt,
(f) Halten der Adreßdaten in einem Register (14a) zur Unterbrechung des Schrittes (d), falls die Peripheriesteuerung (62, 63) dem Mikroprozessor (CPU) das Anforderungssignal (REQ1; REQ2) zuführt,
(g) Zugriffnahme zu dem Speicher (11) entsprechend dem Empfang des Anforderungssignals (REQ1, REQ2) zum Auslesen eines der zweiten Mikrobefehle,
(h) Steuern der Ausführeinheit (2) entsprechend Steuerdaten, die in dem zweiten erhaltenen Mikrobefehl enthalten sind, wobei die Steuerdaten auf erste und dritte Schaltungen der Ausführeinheit einwirken, die erste Schaltung ausschließlich an der Ausführung der DMA-Übertragung beteiligt ist und die dritte Schaltung für die Ausführung der DMA-Übertragung und des vorbestimmten Makrobefehls gemeinsam verwendet wird,
(i) Zugriffnahme zu dem Speicher (11) entsprechend Adreßdaten, die in dem zweiten erhaltenen Mikrobefehl enthalten sind,
(j) Wiederholen der Schritte (h) und (i), bis sämtliche zweiten Mikrobefehle ausgeführt sind, und
(k) Zugriffnahme zu dem Speicher (11) unter Verwendung der in dem Register (14a) gehaltenen Adreßdaten bei Beendigung der Datenübertragung, und Rückkehr zum Schritt (c).

10. Verfahren nach Anspruch 9, wobei zu dem Schritt (h) die Bereitstellung von Adressensignalen von dem Mikroprozessor über die Sammelleitung (61) an den Datenspeicher (65) gehört, wenn die Ausführeinheit (2) in Betrieb ist.