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"A playback equalizer".

The present invention relates to a playback equalizer for providing compensation for a playback signal from a magnetic tape playback head.

Referring to Figure 1 of the accompanying drawings, the overall recording/playback frequency characteristics l_{12} deviate from the ideal characteristics l_{11} due to losses during recording (such as eddy-current loss in the recording head, losses from demagnetization, and tape thickness loss) and losses during playback (loss due to the clearance between the tape and the head, eddy-current loss in the reproducing head, and gap loss in the reproducing head). The overall frequency characteristics l_{12} have a peak response at a frequency of about 5KHz.

In order to flatten the frequency characteristics of a circuit having peaky response, a considerable degree of frequency compensation is necessary in the recording and playback circuits. The operation of compensating frequencies is called equalization, and a circuit for this operation is called an equalizer.

Taking the signal-to-noise ratio and distortion into consideration, the high-frequency region is compensated during recording, and the low-frequency region is compensated during playback.

5 In order to vary the amount of compensation depending upon the speed of the tape, the kind of tape, and the construction and performance of the head, have to be taken into account. With a view to obtaining compatibility among a variety of magnetic recording/
10 reproducing apparatus, normal playback compensation characteristics have been determined for each tape speed. Figure 2 of the accompanying drawings shows examples of recording and playback compensation characteristics for tape speeds of 19 cm/sec and
15 9.5 cm/sec.

The normal playback compensation characteristics are determined by two time constants T_1 and T_2 of a circuit which is made up of a combination of a group of capacitors and a group
20 of resistors. Table 1 illustrates principal standard normal playback compensation characteristics.

Table 1

Normal playback compensation characteristics

Tape speed	38		19		9.5		4.8	
Time constant	T_1	T_2	T_1	T_2	T_1	T_2	T_1	T_2
BTS	3180	35	3180	50	-	-	-	-
CCIR	-	35	-	70	-	-	-	-
DIN	-	35	-	70	-	-	-	-
	-	-	3180	50	3180	90	3180	120
IEC	-	35	-	70	3180	90	1590	120
JIS	-	-	3180	50	3180	90	-	-
NAB	3180	50	3180	50	3180	90	3180	90
RIAA	-	-	3180	50	3180	90	1590	120

Tape speed (cm/sec), time constant (microseconds)

In the field of magnetic tape recording/
 playback apparatus, not only the open reel-type and
 cassette-type apparatus having different tape speeds
 5 have been developed, but also normal tapes, chrome
 tapes and metal tapes having different characteristics
 have been developed.

Even in the cassette type magnetic tape
 recording/playback apparatus in which the standard
 20 tape speed is sometimes run at half speed or double
 speed. Therefore, playback compensation

characteristics are required for the magnetic tape playback equalizer to respond to various tape speeds and various kinds of magnetic tape.

5 Figure 3 of the accompanying drawings shows playback compensation characteristics suited for this sort of magnetic tape playback equalizer, in which the gain of playback compensation characteristics is about 40 dB at a frequency f_1 of 50 Hz which corresponds to a time constant T_1 of 3180 microseconds, and the gain
10 decreases by 20 dB per octave in the frequency bands higher than f_1 . When any one of the frequencies f_{21} , f_{22} , f_{23} , f_{24} , f_{25} and f_{26} corresponding to the time constants of 35 μ S, 50 μ S, 70 μ S, 120 μ S and 200 μ S, is selected, the gain assumes flat characteristics
15 in the frequency band higher than the selected frequency.

 In the conventional magnetic tape playback equalizer, a negative feedback circuit is constructed based upon a negative feedback-type amplifier circuit
20 which is made up of a combination of a group of capacitors and a group of resistors. To change the playback compensation characteristics in response to the tape speed and the kind of tape, the resistances of the resistor group in the negative feedback circuit
25 must be changed. Therefore, it was not possible to form the negative feedback circuit for conventional

playback equalizer in a monolithic semiconductor integrated circuit.

A system has been proposed in which the time constant T_2 at a high frequency f_2 in the playback compensation characteristics is specified by means of a group of semiconductor diffused resistors and a group of semiconductor switching elements formed in a monolithic semiconductor integrated circuit and by a capacitor array outside the monolithic semiconductor integrated circuit. As is well known, the resistance of diffused resistors formed in a monolithic semiconductor integrated circuit have errors of $\pm 20\%$ that stem from the process for manufacturing the integrated circuits. This fact causes the time constant T_2 at a high frequency f_2 in the playback compensation characteristics to vary greatly, so a system of this type has not been put into practice.

According to the present invention there is provided a playback equalizer for providing compensation for a playback signal from a magnetic tape playback head including:

20 (a) an integrated circuit having an input terminal and an output terminal;

(b) a main path in said integrated circuit having a first end and a second end, said first end being connected to said input terminal and supplied with said playback
25 signal;

(c) a side path in said integrated circuit having a first end and a second end, said first end being connected to said input terminal;

(d) a low-pass filter including a first capacitor

associated with said main path, said capacitor being located outside said integrated circuit and connected thereto through a first external terminal, said low-pass filter permitting the transmission of a signal which has a first component of flat frequency characteristic below a predetermined first frequency as well as a second component of decreasing frequency characteristic above said predetermined first frequency to said second end;

(e) variable gain means arranged between said first end and said second end of said side path, said variable gain means having substantially flat frequency characteristic over a predetermined frequency range and the gain which is controllably varied by external units through a second external terminal; and

(f) an analog adder in said integrated circuit connected between said output terminal and said second ends of said main and side paths, said adder including means for adding in an analog manner a signal at said second end of said main path and a signal at said second end of said side path and means for transmitting the added signal to the output terminal, which signal has a first component of flat frequency characteristic below said predetermined first frequency, a second component of decreasing frequency characteristic between said predetermined first frequency and a predetermined second frequency, and a third component of flat frequency characteristic above said predetermined second frequency, said predetermined second frequency being adjusted by said decreasing frequency characteristic of said low-pass filter and said gain of said variable gain means.

The present invention will now be described in greater detail with reference to the remaining figures of the accompanying drawings, wherein:

Figure 4 is a circuit diagram of a one preferred
5 form of playback equalizer;

Figure 5 is a circuit diagram of a second embodiment of a playback equalizer;

Figures 6 and 7 are circuit diagrams of a third embodiment of a playback equalizer; and

10 Figure 8 is a circuit diagram of a fourth embodiment of a playback equalizer.

Referring to the first embodiment of a playback equalizer shown in Figure 4, it should be noted that parts surrounded by a broken line IC are formed in a monolithic
15 semiconductor integrated circuit. Numerals in a circle indicate terminal numbers of the integrated circuit.

A playback signal V_{in} from a recording/playback head (not shown) is transmitted to a first terminal, and then to a main path $1_m-1'_m$ and a side path $1_s-1'_s$ of a
20 playback equalizer.

The first terminal is connected to the input terminal of a first amplifier A_1 which has substantially flat frequency characteristic and whose output terminal is connected to the input terminal of a first circuit BF1
25 (such as an emitter-follower circuit) having a high input impedance via a low-pass filter LPF which determines the frequency characteristics.

The low-pass filter LPF consists of an electronic

impedance device R_1 formed in an integrated circuit and a first capacitor C_1 located outside the integrated circuit. The resistance of the electronic impedance device R_1 can be freely changed by changing the resistance of an external resistor R_{100} connected to an eighth terminal. The voltage or current at the eighth terminal can be changed, whereby the resistance of the electronic impedance device R_1 can be accurately adjusted relying upon the change in the quantity of electricity.

A time constant T_1 of 3180 microseconds (i.e., frequency f_1 of 50 Hz) in the playback compensation characteristics of Fig. 3 can be established by setting the capacitance of the first capacitor C_1 to be, for example, 0.047 μ F, and setting the resistance of the electronic impedance device R_1 to be 67.659 Kohms.

A voltage gain of about 40 dB can be maintained in the amount of the signal transmitted through the low-pass filter LPF, i.e., flat characteristics can be maintained in a frequency band lower than the frequency f_1 of 50 Hz. The gain decreases by 20 dB per octave in the frequency bands higher than the frequency f_1 .

A signal transmitted from the low-pass filter LPF is produced at the output terminal of the first buffer circuit BF1 at the end ϕ'_m of the main path with low

output impedance; and then fed to an analog adder ASC.

Input terminals of a plurality of amplifiers A_{21} , A_{22} , A_{23} , A_{24} , A_{25} and A_{26} having substantially flat frequency characteristics are connected to the first terminal. Their output terminals are connected to an input terminal of a second buffer circuit BF2 (such as emitter-follower circuit) having a high input impedance via electronic switching devices SW_{21} , SW_{22} , SW_{23} , SW_{24} , SW_{25} and SW_{26} .

The amplifiers A_{21} , A_{22} , A_{23} , A_{24} , A_{25} and A_{26} have voltage gains of about 15.5 dB, 11 dB, 8.5 dB, 6 dB, 3.5 dB and 0.5 dB, respectively.

The control input terminal of an electronic switch control circuit ESC is connected to a third terminal which is connected a group of electric contacts C_1 , C_2 , C_3 , C_4 , C_5 and C_6 outside the integrated circuit and to a group of external resistors R_{11} , R_{12} , R_{13} , R_{14} , R_{15} and R_{16} . The external resistors R_{11} to R_{16} have different resistances.

When the electric contact C_1 is closed, only the electronic switching device SW_{21} is closed by the electronic switch control circuit ESC. Therefore, the input signal fed to the amplifier A_{21} at the starting end ℓ_s of the side path is amplified in accordance with the voltage gain (15.5 dB) of the amplifier A_{21} , and is

then transmitted to the input terminal of the second buffer circuit BF2 (such as an emitter-follower circuit), which has a high impedance.

When the electric contact C_2 is closed, only the
5 electric switching device SW_{22} is closed, and the input signal at the starting end θ_s of the side path is amplified in accordance with the voltage gain (11 dB) specific to the amplifier A_{22} .

Thereafter, when any one of the electric contacts
10 C_3 to C_6 is closed, the corresponding electronic switching device is closed among the electronic switching devices SW_{23} to SW_{26} , and the input signal at the starting end θ_s of the side path is amplified in accordance with the voltage gain specific to the corresponding
15 amplifier among the amplifiers A_{23} to A_{26} .

The output signal of any one of the amplifiers A_{21} to A_{26} is produced at the output terminal of the second buffer circuit BF2 at the end θ'_s of the side path with low output impedance, and is fed to the analog adder
20 ASC.

The analog adder ASC consists of semiconductor diffused transistors R_2 and R_3 which have an equal resistance of, for example, 12 kilohms, and a third buffer circuit BF3. The third buffer circuit BF3
25 consists, for example, of an emitter-follower circuit which

has a high input impedance and a low output impedance.

The analog adder circuit ASC performs analog addition of the signal voltage at the end $\varnothing'_m$ of the main path and the signal voltage at the end $\varnothing'_s$ of the side path, and sends the added signal to the second terminal.

Here, attention should be paid to the fact that the voltage gains of the amplifiers A_1 , A_{21} , A_{22} , A_{23} , A_{24} , A_{25} and A_{26} are set by resistance ratios of the semiconductor diffused resistors in the monolithic semiconductor integrated circuits, and the resistance ratios have very small errors. The voltage gains of amplifiers A_1 and A_{21} to A_{26} can be set by the resistance ratios of semiconductor resistors formed by ion implantation. In this case too, the resistance ratios have very small errors. As a conclusion, it is important to determine the voltage gains of the amplifiers A_1 and A_{21} to A_{26} based upon the resistance ratios of semiconductor resistors which deviated little in the integrated circuit manufacturing process.

The first embodiment shown in Figure 4 is advantageous over known systems for the following reasons:-

(1) The playback compensation characteristics at frequencies lower than the frequency f_1 of 50 Hz are

substantially determined by the voltage gain of the amplifier A_1 .

(2) The frequency f_1 of 50 Hz is accurately set by the capacitance of the first capacitor C_1 and the resistance of the adjustable electronic impedance device R_1 .

(3) At frequencies higher than the frequency f_1 of 50 Hz, the frequency characteristics of -20 dB/octave are exclusively determined by the RC type low-pass filter LPF.

(4) Since the voltage gains of the amplifiers A_{21} to A_{26} are accurately determined by the resistance ratios of semiconductor resistors in the monolithic semiconductor integrated circuit, and on account of the above-mentioned reasons (1) to (3), it is possible to accurately adjust the frequencies f_{21} (796.1 Hz), f_{22} (1.3269 KHz), f_{23} (1.7692 KHz), f_{24} (2.2747 KHz), f_{25} (3.1847 KHz) and f_{26} (4.5495 KHz) that correspond to time constants T_1 of 200 μ S, 120 μ S, 90 μ S, 70 μ S, 50 μ S and 35 μ S, as shown in Fig. 3.

Referring to the second embodiment of a playback equalizer shown in Figure 5, it should be noted that the same positions as those of the first embodiment shown in

Fig. 4 are denoted by the same reference symbols or

numerals, and their description is omitted here.

In Fig. 5, the amplifiers A_{21} , A_{22} , A_{23} , A_{24} , A_{25} and A_{26} employed in the embodiment of Fig. 4 are replaced by a voltage controlled variable gain circuit VCA, and the group of external resistors R_{11} , R_{12} , R_{13} , R_{14} , R_{15} and R_{16} employed in the embodiment of Fig. 4 is replaced by control voltages V_1 , V_2 , V_3 , V_4 , V_5 and V_6 having different voltage levels. Further, the embodiment of Fig. 5 does not employ the electronic switch control circuit ESC that was used in the embodiment of Fig. 4.

The voltage controlled variable gain circuit VCA consists of an input resistor R_{IN} , an operational amplifier A_{OP} , level-shifting batteries V_{B1} and V_{B2} , NPN-type transistors Q_1 and Q_3 , PNP-type transistors Q_2 and Q_4 , and a load resistor R_L . The inverting input terminal (-) of the operational amplifier A_{OP} is connected to collectors of the transistors Q_2 , Q_4 and is further connected to an input terminal T_{IN} (starting end θ_s of the side path) via the input resistor R_{IN} , and its non-inverting input terminal (+) is earthed. The output level of the operational amplifier A_{OP} is shifted by the batteries V_{B1} and V_{B2} , and the thus shifted two voltages are applied to the emitters (connection point T_1) of the PNP-type transistors Q_2 , Q_4 , and the emitters (connection point T_3) of the NPN-type

transistors Q_1 , Q_3 , respectively.

The bases (connection point T_2) of the PNP-type transistor Q_2 and the NPN-type transistor Q_3 are connected to earth. When a

5 control voltage V_C for controlling the gain is applied to the bases (connection point T_4) of the PNP-type transistor Q_4 and the NPN-type transistor Q_1 , a variable output voltage V_{OUT} is produced across the load resistor R_L , as given by,

10
$$i_{IN} = \frac{V_{in}}{R_{IN}} \quad \dots (1)$$

$$\frac{i_{OUT}}{i_{IN}} = \exp \frac{q(-V_C)}{KT} \quad \dots (2)$$

$$V_{OUT} = R_L \cdot i_{OUT} \quad \dots (3)$$

By suitably setting the voltage levels of the control voltages V_1 to V_6 , the voltage gain of the voltage
15 controlled variable gain circuit VCA can be set to suitable values. Accordingly, it is possible to accurately set time constants T_2 of 200 μS , 120 μS , 90 μS , 70 μS , 50 μS and 35 μS in the playback compensation characteristics of Fig. 3.

20 The voltage controlled variable gain circuit VCA is already widely known. For details, reference should

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be made to British Patent Specification No. 2,053,598 entitled "Signal Transmission Circuit".

Referring to the third embodiment of a playback equalizer shown in Figure 6, it should be noted that the same positions as those of the second embodiment shown in Figure 5 are denoted by the same reference symbols or numerals, and their description is omitted.

In the embodiment of Figure 6, the low-pass filter LPF consisting of electronic impedance device R_1 and a first capacitor C_1 employed in the embodiments of Figures 4 and 5 is replaced by a voltage-current converter V-Iconv and a low-pass filter LPF' which consists of an external resistor R_{101} and a first capacitor C_1 . Further, the eighth terminal and the external resistor R_{100} are omitted.

In the low-pass filter LPF', if the capacitance of the first capacitor C_1 is set to, for example 0.047 μ F and the resistance of the external resistor R_{101} is set to 67.659 Kohms, a time constant of 3180 μ S (at the frequency f_1 of 50 Hz) can be obtained in the playback compensation characteristics of Figure 3.

A voltage gain with flat frequency characteristics at frequencies lower than the frequency f_1 of 50 Hz can be set on the main path $\mathcal{L}_m$ by the voltage gain of the first amplifier A_1 , by the converting rate of the voltage-current converter V-I_{conv}, and by the resistance of the external resistor R_{101} in the low-pass filter LPF'.

A fourth buffer circuit BF4 (such as an emitter-follower circuit) and a semiconductor diffused resistor R_4 are inserted in the side path $\mathcal{L}_s$.

An electronic impedance device EID is connected to the point where the semiconductor diffused resistor R_4 is connected to the input terminal of the second buffer circuit BF2.

The electronic impedance device EID consists of a voltage-current converter 3 having a high input impedance, a variable gain current amplifier 4, a variable constant current source 6, and a constant current source 7. The voltage-current converter 3 having a high input impedance consists of PNP-type transistors Q_1 , Q_2 , and semiconductor diffused resistors R_{21} , R_{22} . The variable gain current amplifier 4 consists of diodes D_1 , D_2 , NPN-type transistors Q_3 , Q_4 , PNP-type transistors Q_5 , Q_6 , Q_7 , and semiconductor diffused resistors R_{23} , R_{24} . The variable constant current source 6 consists of an

NPN-type transistor Q_9 , and the constant current source 7 consists of a PNP-type transistor Q_{10} .

For details of the electronic impedance device EID, reference should be made to U.S. Patent
5 No. 4,220,875.

Cathodes of the diodes D_1 , D_2 have applied thereto a bias voltage V_{bias} determined by the semiconductor diffused resistors R_{25} , R_{26} and by the base-emitter forward voltage of the transistor Q_8 .

10 The input impedance Z_{in} of the electronic impedance device EID at the point where the base of the transistor Q_2 is connected to collectors of the transistors Q_3 , Q_5 can be changed by varying the value of the constant current which flows into the
15 collector-emitter path of transistor Q_9 which serves as the variable constant current source 6.

A bias circuit BC consists of semiconductor diffused resistors R_{27} , R_{28} , R_{29} , R_{30} , transistors Q_{11} , Q_{12} , diodes D_3 , D_4 , and a zener diode ZD, and
20 produces various bias voltages.

The point where resistors R_{27} and R_{28} are connected together is connected to earth via an external capacitance C_2 and a seventh terminal. Further, a reference voltage V_{REF} generated at
25 this connection _____

point is fed to the low-pass filter LPF' and to the electronic impedance device EID.

A constant voltage supplied from the emitter of transistor Q_{11} in the bias circuit BC is applied to the base of the transistor Q_9 which works as the variable constant current source 6, and the emitter of transistor Q_9 is connected via a third terminal to a group of electric contacts C_1, C_2, C_3, C_4, C_5 and C_6 , and a group of external resistors $R_{11}, R_{12}, R_{13}, R_{14}, R_{15}$ and R_{16} .

When any one of electric contacts C_1 to C_6 , is closed, the corresponding resistor among the external resistors R_{11} to R_{16} is connected to the emitter of the transistor Q_9 which serves as the variable constant current source 6, thereby changing the value of the constant current flowing into the collector-emitter path of transistor Q_9 .

Thus, the gain on the side path θ_s is determined by the resistance of the semiconductor diffused resistor R_4 and by the input impedance Z_{in} of the electronic impedance device EID, and so it is possible to set time constants T_2 of 200 μS , 120 μS , 90 μS , 70 μS , 50 μS and 35 μS in the playback compensation characteristics of Fig. 3.

On the other hand, when the resistors R_{21} and R_{22} have an equal resistance, the input impedance Z_{in} of

the electronic impedance device EID is given by the following equations:

$$Z_{in} = \frac{r_{e2} + R_{22}}{r_{d2}} \cdot r_{e4} \quad \dots (4)$$

$$r_{e2} = r_{d2} = \frac{KT}{qI_o} \quad \dots (5)$$

$$r_{e4} = \frac{KT}{qI_c} \quad \dots (6)$$

where r_{e2} denotes the dynamic resistance at the base-emitter junction of transistor Q_2 ;

r_{d2} denotes the dynamic resistance of diode D_2 ;

r_{e4} denotes the dynamic resistance at the base-emitter junction of transistor Q_4 ;

K denotes Boltzmann's constant;

T denotes absolute temperature;

q denotes the electric charge of an electron;

I_o denotes a value of one-half the constant current flowing into the collector-emitter path of the transistor Q_{10} ; and

I_c denotes a value one-half of the constant current flowing into the collector-emitter path of transistor Q_9 .

The following equation can be derived from the above equations (4), (5) and (6).

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$$Z_{in} = \frac{\frac{KT}{qI_o} + R_{22}}{\frac{KT}{qI_o}} \cdot \frac{KT}{qI_c} \dots (7)$$

If the constant current I_o is set at 250 μA , the dynamic resistance r_{d2} ($=KT/qI_o$) become about 100 ohms, since KT/q for the semiconductor diode is about 100 ohms, for example, 3 Kohms, the dynamic resistance r_{e2} becomes negligibly small compared with the diffused resistor R_{22} . Therefore, the equation (7) can be written approximately as follows:

current I_o is set at 250 μA , r_{d2} ($=KT/qI_o$) become about 100 ohms, since KT/q for the semiconductor diode is about 100 ohms, for example, 3 Kohms, the dynamic resistance r_{e2} becomes negligibly small compared with the diffused resistor R_{22} . Therefore, the equation (7) can be written approximately as follows:

$$Z_{in} \approx R_{22} \cdot \frac{I_o}{I_c} \dots (8)$$

The potential differences between both ends of the diode D_3 and the diode D_4 , and the potential differences between the bases and the emitters of transistors Q_9 and Q_{11} become substantially equal to the forward voltage V_F at the PN junction. Therefore, the constant current $2I_o$ which flows into the collector-emitter path of transistor Q_{10} serving as the constant-current source 7 is given by the following equation (9), and the constant current $2I_c$ which flows into the collector-emitter path of transistor Q_9 serving as the variable constant-current source 6, when the electric contact C_1 is closed, is given by the equation (10).

$$2I_o = \frac{V_Z - V_F}{R_{30}} \quad \dots (9)$$

$$2I_c = \frac{V_Z - V_F}{R_{11}^*} \quad \dots (10)$$

where V_Z denotes the Zener voltage of the Zener diode ZD_1 .

By inserting equations (9) and (10) into equation (8), the following equation can be obtained,

$$Z_{in} = \frac{R_{22}}{R_{30}} \cdot R_{11}^* \quad \dots (11)$$

As will be obvious from the equation (11), the semiconductor diffused resistors R_{22} and R_{30} have equal temperature dependency and equal deviation since they are produced by the same manufacturing process.

Moreover, the resistance R_{11}^* of the external resistor R_{11} can be accurately given any value, with very little temperature dependency. Accordingly, the temperature dependency and error in the input impedance Z_{in} can be reduced to very small values.

Fig. 7 shows the circuit of Fig. 6 in detail. In Fig. 7, the same portions as those of the above-mentioned embodiments are denoted by the same reference symbols

or reference numerals, and their details are omitted.

The first amplifier A_1 consists of NPN-type transistors Q_{31} and Q_{32} which are differentially connected, PNP-type transistors Q_{34} and Q_{35} which form a current mirror, an emitter-follower NPN-type transistor Q_{36} , an NPN-type transistor Q_{37} and a PNP-type transistor Q_{38} which constitute a push-pull amplifier circuit, bias diodes D_5 and D_6 , constant current sources CS_1 , CS_2 , and CS_3 , and semiconductor diffused resistors R_{31} and R_{32} which form a negative feedback circuit. The voltage gain of the first amplifier A_1 is determined by the ratio of the resistances of semiconductor diffused resistors R_{31} and R_{32} . Therefore, error in the voltage gain can be made very small.

The voltage-current converter V-Iconv includes PNP-type transistors Q_{39} , Q_{40} and Q_{41} which form a first current mirror, and NPN-type transistors Q_{42} , Q_{43} and Q_{44} which form a second current mirror. The electric current which flows into the first current mirror is determined by the current which flows into the collector of NPN-type transistor Q_{37} , and the current which flows into the second current mirror is determined by the current which flows into the collector of PNP-type transistor Q_{38} .

The first, second, third and fourth buffer circuits

BF1, BF2, BF3 and BF4 are made up of transistors Q_{47} , Q_{48} , Q_{49} , Q_{50} , Q_{51} , Q_{52} , Q_{53} , Q_{54} , and constant current sources CS_4 , CS_5 , CS_6 , CS_7 and CS_8 .

Referring to the fourth embodiment of a
5 playback equalizer shown in Figure 8, it should
be noted that the same positions as those of
the third embodiment shown in Figures 6 and 7
are denoted by the same
reference symbols or numerals, and their details are
10 not described here.

The embodiment of Fig. 8 does not possess the fourth
buffer circuit BF4 and the semiconductor diffused
resistor R_4 that were employed in the embodiment of
Figs. 6 and 7. Instead, the first current mirror of
15 the voltage current converter V-Iconv further includes
a PNP-type transistor Q_{45} , and the second current mirror
includes an NPN-type transistor Q_{46} , the collectors
of the two transistors Q_{45} and Q_{46} being connected to
the electronic impedance device EID.

20 When a playback signal voltage V_{in} is applied to
the first terminal, the amplified signal voltage
 V_{37-38} produced across the emitters of transistor Q_{37}
and transistor Q_{38} of the first amplifier A_1 is given
by the following equation

$$V_{37-38} = \frac{R_{31} + R_{32}}{R_{32}} \cdot V_{in} \quad \dots (12)$$

5 The signal current I_{41-44} obtained from the collectors of transistors Q_{41} , Q_{42} in the voltage-current converter V-Iconv, and a signal current I_{45-46} obtained from the collectors of transistors Q_{45} , Q_{46} , are given by the following equation

$$10 \quad I_{41-44} = I_{45-46} = \frac{V_{37-38}}{R_{31} + R_{32}} = \frac{V_{in}}{R_{32}} \quad \dots (13)$$

The signal voltage $V_{LPF'}$ produced in the low-pass filter LPF' at frequencies lower than the frequency f_1 of 50 Hz, is given by the equation

$$15 \quad V_{LPF'} = R_{101} \cdot I_{41-44} = \frac{R_{101}}{R_{32}} \cdot V_{in} \quad \dots (14)$$

And the signal voltage V_{EID} produced in the electronic impedance device EID is given by the equation

$$20 \quad V_{EID} = Z_{in} \cdot I_{45-46} = \frac{R_{22} \cdot R_{11}}{R_{30} \cdot R_{32}} \cdot V_{in} \quad \dots (15)$$

As will be obvious from the above equations (14) and (15), the semiconductor diffused resistors R_{22} , R_{30} and R_{32} have equal temperature dependency and equal

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deviation, since they are produced by the same manufacturing process. Further, resistances R_{101}^* and R_{11}^* of the external resistors R_{101} and R_{11} are given accurate values with very little temperature dependency.

5 Thus, the temperature dependency of the two signal voltages $V_{LPF'}$ and V_{EID} resembles the deviation caused by the manufacturing process.

The fourth embodiment shown in Figure 8 is advantageous over known systems for the following reasons:-

10 (1) A signal voltage $V_{LPF'}$ produced in the low-pass filter LPF' and a signal voltage V_{EID} produced in the electronic impedance device EID are determined by the ratio of an external resistance to the semiconductor diffused resistance. Therefore, playback compensation
15 characteristics at frequencies lower than the frequency f_1 of 50 Hz and playback compensation characteristics at frequencies higher than the frequency f_2 which corresponds to a time constant T_2 , have a tendency that resembles the tendency of deviation dependent
20 upon the manufacturing process.

(2) The frequency f_1 of 50 Hz is precisely set by the capacitance of the first capacitor C_1 and the resistance of external resistor R_{101} .

25 (3) At frequencies higher than the frequency f_1 of 50 Hz, frequency characteristics of - 20 dB/octave are exclusively defined by the RC-type low-pass filter LPF' .



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CLAIMS.

1. A playback equalizer for providing compensation for a playback signal from a magnetic tape playback head including:

(a) an integrated circuit having an input terminal
5 and an output terminal;

(b) a main path in said integrated circuit having a first end and a second end, said first end being connected to said input terminal and supplied with said playback signal;

(c) a side path in said integrated circuit having a
10 first end and a second end, said first end being connected to said input terminal;

(d) a low-pass filter including a first capacitor associated with said main path, said capacitor being located outside said integrated circuit and connected thereto
15 through a first external terminal, said low-pass filter permitting the transmission of a signal which has a first component of flat frequency characteristic below a predetermined first frequency as well as a second component of decreasing frequency characteristic above said predetermined
20 first frequency to said second end;

(e) variable gain means arranged between said first end and said second end of said side path, said variable gain means having substantially flat frequency characteristic over a predetermined frequency range and the gain
25 which is controllably varied by external units through a second external terminal; and

(43)



(f) an analog adder in said integrated circuit connected between said output terminal and said second ends of said main and side paths, said adder including means for adding in an analog manner a signal at said second end of 5 said main path and a signal at said second end of said side path and means for transmitting the added signal to the output terminal, which signal has a first component of flat frequency characteristic below said predetermined first frequency, a second component of decreasing frequency 10 characteristic between said predetermined first frequency and a predetermined second frequency, and a third component of flat frequency characteristic above said predetermined second frequency, said predetermined second frequency being adjusted by said decreasing frequency characteristic 15 of said low-pass filter and said gain of said variable gain means.

2. A playback equalizer according to claim 1, wherein said variable gain means comprises a plurality of amplifiers having different gains from one another and switching means 20 operated from said external units which determine which one of the amplifiers is to be selected to provide an output to said adder.

3. A playback equalizer according to claim 1, wherein said external units comprise a plurality of control voltages 25 having dissimilar voltage levels, and said variable gain means is a voltage controlled variable gain circuit whose gain is varied in response to said plurality of control voltage.



4. A playback equalizer according to claim 1, wherein said external units comprise a plurality of resistors having different resistances, and said variable gain means is an electronic impedance device
- 5 whose input impedance changes in response to said plurality of resistors.
5. A playback equalizer according to claim 4, wherein said main path is provided with a first amplifier whose gain is set according to a ratio of semiconductor
- 10 resistances in an integrated circuit.
6. A playback equalizer according to claim 5, wherein said low-pass filter includes a first resistor located outside the integrated circuit and connected to said first capacitor, wherein a voltage-current
- 15 converter is coupled to the output of said first amplifier in order to convert an output voltage from said first amplifier into an output signal current, and wherein said first capacitor and said first resistor are driven by the output signal current of said voltage-current converter.
- 20 7. A playback equalizer according to claim 1, wherein said low-pass filter includes an electronic impedance device formed in the integrated circuit, the resistance of said electronic impedance device being changed in response to first control means, said
- 25 predetermined first frequency being established by setting the capacitance of said first capacitor and the resistance of said electronic impedance device.



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8. A playback equalizer for providing compensation for a playback signal from a magnetic tape playback head constructed substantially as herein described with reference to and as illustrated in Figure 4, or Figure 5, or Figures 6 and 7, or Figure 8 of the accompanying drawings.
