

Description

This invention relates to a voltage controlled oscillator circuit formed in an integrated circuit configuration for use in a frequency synthesizer of phase-locked loop form.

Conventionally, a voltage controlled oscillator (VCO) whose output frequency varies in response to a control voltage is constructed as shown in Fig. 17. (Fig. 17 corresponds to Fig. 3 of Japanese Patent Disclosure No. 59-62215)

In Fig. 17, 71 denotes an input node for control voltage V_{in} , 72 an input N-channel transistor, and 73 and 74 load P-channel transistors constituting current mirror circuit 75. P-channel transistor 76 and N-channel transistor 77 are combined to constitute first CMOS inverter 78, and first capacitor 80 is connected between output node 79 of inverter 78 and the ground terminal. Further, P-channel transistor 81 and N-channel transistor 82 are combined to constitute second CMOS inverter 83, and second capacitor 85 is connected between output node 84 of inverter 83 and the ground terminal.

Output nodes 79 and 84 of CMOS inverters 78 and 83 are respectively connected to input terminals of voltage comparators 86 and 87 whose output terminals are connected to set input terminal S and reset input terminal R of RS flip-flop circuit 88. Set output terminal Q and reset output terminal $\bar{Q}$ of flip-flop circuit 88 are respectively connected to first and second CMOS inverters 78 and 83, and the output from reset output terminal $\bar{Q}$ is inverted by means of inverter 89 and derived out as output voltage V_{out} .

The operation of the above VCO is briefly explained. Current is supplied to input transistor 72 in response to control voltage V_{in} , and at this time, current I of the same amount is supplied from output transistor 74 of current mirror circuit 75 to two CMOS inverters 78 and 83. Assume that, in the initial condition, output terminal Q of flip-flop circuit 88 is set at low level "L" and output terminal $\bar{Q}$ is set at high level "H". Then, transistors 76 and 82 of two CMOS inverters 78 and 83 are turned on and transistors 77 and 81 are turned off. In this condition, first capacitor 80 is charged by current I via transistor 76 which is now set in the conductive state.

When, in this charging operation, the terminal voltage of capacitor 80 exceeds threshold voltage V_{th1} of voltage comparator 86, the output thereof becomes high. Then, outputs Q and $\bar{Q}$ of flip-flop circuit 88 are inverted to high and low levels, respectively, thereby setting transistors 76 and 82 of two CMOS inverters 78 and 83 nonconductive and transistors 77 and 81 conductive. As a result, second capacitor 85 is charged via transistor 81 is turned on by current I. At this time, charges of previously charged capacitor 80 are discharged to the ground terminal via transistor 77 which is now set conductive.

When the terminal voltage of second capacitor 85 which is now being charged exceeds threshold voltage V_{th2} of comparator 87, the output thereof becomes high. As a result, outputs Q and $\bar{Q}$ of flip-flop circuit 88 are inverted to low and high, respectively, thereby setting transistors 76 and 82 conductive and setting transistors 77 and 81 nonconductive as described before. By repeatedly effecting the same operation, oscillator output voltage V_{out} can be derived from the output terminal of inverter 89, and frequency f of the oscillator output voltage is obtained as follows:

$$f = \frac{I}{2C \cdot V_{ref}} \quad \dots (1)$$

where C is a capacitance of capacitors 80 and 85, and V_{ref} is threshold voltage V_{th1} or V_{th2} of voltage comparator 86 or 87.

When the conventional VCO is formed on an IC chip, the gate length, gate threshold voltage and gate oxide film thickness of the transistors will fluctuate depending on variation in the manufacturing conditions (process parameters). Therefore, I, C and V_{ref} in equation (1) may significantly vary, causing the oscillation center frequency to widely fluctuate. Thus, the characteristics of a phase-locked loop (PLL) system using the VCO may be degraded, lowering the manufacturing yield.

This invention has been made to solve the problem that the oscillation center frequency is widely changed with variation in the manufacturing condition and the manufacturing yield of applied system products is lowered.

An object of this invention is to provide a voltage controlled oscillator circuit whose oscillation center frequency can be freely set without receiving any influence due to variation in the manufacturing condition.

A voltage controlled oscillator circuit of this invention comprises a phase-locked loop section which includes first delay means having cascade-connected m-stage delay sections whose delay times are controlled by a control signal, for delaying a reference frequency signal; phase difference voltage generating means for generating a phase difference voltage corresponding to a phase difference between a

signal delayed by a predetermined period (e.g., one half the period thereof) and the reference frequency signal; and first control signal generating means for generating the control signal for determining the signal delay times of the respective delay sections of the first delay means based on a reference voltage and the phase difference voltage; and a voltage controlled oscillator section which includes second delay means including cascade-connected n -stage delay sections having the structure equivalent to that of the delay sections of the first delay means, wherein the output of the second delay means is fed back to the input terminal thereof so that a ring oscillator is constructed; and second control signal generating means for generating a control signal for determining the signal delay times of the respective delay sections of the second delay means based on a control voltage for controlling the output frequency and the phase difference voltage.

Each of the delay sections of the first and second delay means includes a first transmission gate; an inverter supplied with the output of the first transmission gate; a second transmission gate supplied with the output of the inverter; and an inverter supplied with the output of the second transmission gate. Each of the first and second control signal generating means includes a first transistor of a first conductivity type whose source-drain path is connected between a first voltage terminal and a first output node and whose gate is supplied with the phase difference voltage; a second transistor of the first conductivity type whose source-drain path is connected between the first voltage terminal and the first output node and whose gate is connected to the first output node; and a third transistor of a second conductivity type whose source-drain path is connected between a second voltage terminal and the first output node and whose gate is supplied with either the reference voltage or the control voltage. Signals of the first output nodes of the first and second control signal generating means are supplied to the first and second transmission gates of each of the delay sections of the first and second delay means.

The center frequency of the oscillator frequency can be determined by controlling the delay time of the second delay means constituting the ring oscillator in the voltage controlled oscillator circuit. Since the delay time can be precisely controlled by means of the phase-locked loop section, a stable center frequency which is independent of variation in the manufacturing condition can be obtained. Further, the band width of the center frequency can be freely set by changing the reference frequency signal or the ratio of the number (m) of delay sections of the first delay means to that (n) of delay sections of the second delay means.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing the whole construction of a voltage controlled oscillator circuit according to one embodiment of this invention;

Fig. 2 is a current diagram showing the detail construction of the one-stage section of a variable delay circuit shown in Fig. 1;

Fig. 3 is a circuit diagram showing the detail construction of a phase comparator and a charge pump circuit shown in Fig. 1;

Figs. 4A and 4B are circuit diagrams showing the detail construction of a low-pass filter shown in Fig. 1;

Fig. 5 is a circuit diagram showing the detail construction of a level conversion circuit shown in Fig. 1;

Figs. 6 to 8 are timing charts showing the operation of a PLL section shown in Fig. 1;

Fig. 9 is a characteristic diagram of the level conversion circuit of Fig. 5;

Fig. 10 is a circuit diagram showing another detail construction of a level conversion circuit shown in Fig. 1;

Fig. 11 is a characteristic diagram of the level conversion circuit of Fig. 10;

Figs. 12 and 13 are circuit diagrams each showing still another detail construction of a level conversion circuit shown in Fig. 1;

Fig. 14 is a current diagram showing another detail construction of the one-stage section of the variable delay circuit shown in Fig. 1;

Figs. 15 and 16 are circuit diagrams showing the level conversion circuit of Fig. 1 in a case where the variable delay circuit of Fig. 14 is used;

Fig. 17 is a circuit diagram showing the conventional voltage controlled circuit; and

Fig. 18 is a block diagram showing the construction of a PLL frequency synthesizer type tuning system in which PLL section 1 and VCO section 2 shown in Fig. 1 are used for the local oscillation section of a super heterodyne tuner.

There will now be described an embodiment of this invention with reference to the accompanying drawings.

Fig. 1 is a block diagram showing the whole construction of a voltage controlled oscillator circuit according to one embodiment of this invention. In Fig. 1, 1 denotes a PLL section, and 2 denotes a VCO

section. PLL section 1 is supplied with reference frequency signal F_{ref} and reference voltage V_{ref} and controls the feedback operation so as to set the delay time of delay circuit 3 in the loop to a constant value, for example, one half period T of reference frequency signal F_{ref} .

VCO section 2 is supplied with control voltage V_{cont} and output voltage V_{off} of low-pass filter 7 of the phase-locked loop of PLL section 1, and oscillation frequency F_{VCO} is determined by controlling the delay time of the ring oscillator circuit using delay circuit 10 based on the received control voltage (V_{cont}) and output voltage (V_{off}).

In PLL section 1, reference frequency signal F_{ref} is supplied to the first input terminals of first variable delay circuit 3 and phase comparator 4. Output DO of first variable delay circuit 3 is input to the other input terminal of phase comparator 4 via inverter 5. Phase comparator 4 compares the phases of the two input signals and controls first output CP or second output DP according to the comparison result.

Two outputs CP and DP are supplied to charge pump circuit 6. The output of charge pump circuit 6 is supplied to low-pass filter (LPF) 7 whose output voltage V_{off} is supplied together with reference voltage V_{ref} to first level conversion circuit 8. First level conversion circuit 8 controls the voltage level of output PV according to the two input voltage levels, and output voltage PV is supplied as a delay time control signal to variable delay circuit 3.

In VCO section 2, output voltage V_{off} of low-pass filter 7 and control voltage V_{cont} are supplied to second level conversion circuit 9. Like first level conversion circuit 8, second level conversion circuit 9 controls the voltage level of output PV according to the two input voltage levels. Output voltage PV is supplied as a delay time control signal to second variable delay circuit 10.

Inverter 11 is connected between the input and output terminals of second variable delay circuit 10 to constitute a ring oscillator circuit. Second level conversion circuit 9, second variable delay circuit 10 and inverter 11 are formed with substantially the same constructions as first level conversion circuit 8, first variable delay circuit 3 and inverter 5.

For example, each of variable delay circuits 3 and 10 is constituted by cascade-connecting a desired number of basic circuits each having the structure shown in Fig. 2. Variable delay circuit 3 is formed of m -stage cascade-connected basic circuits and variable delay circuit 10 is formed of n -stage cascade-connected basic circuits in this example.

An input signal is serially supplied via first transfer gate 21 of a P-channel transistor, inverter 22, second transfer gate 23 of a P-channel transistor and inverter 24, and then output. The gates of first and second transfer gates 21 and 23 are supplied with delay time control signal PV. That is, the resistance components of first and second transfer gates 21 and 23 are changed according to delay time control signal PV to change the delay time of each basic circuit.

Fig. 3 is a circuit diagram showing the detail construction of phase comparator 4 and charge pump circuit 6. In phase comparator 4, reference frequency signal F_{ref} is supplied as a clock signal to D-type flip-flop 31. Likewise, output NDO of inverter 5 in Fig. 1 is supplied as a clock signal to D-type flip-flop 32. Q outputs of flip-flops 31 and 32 are supplied to AND gate 33 whose output is in turn supplied as a reset signal to flip-flops 31 and 32.

Output Q of flip-flop 31 is supplied as first output CP via inverter 34, and output Q of flip-flop 32 is supplied as output DP.

Charge pump circuit 6 includes P-channel transistor 35 and N-channel transistor 36 series-connected between power source voltage terminal V_{cc} and the ground terminal. The gates of transistors 35 and 36 are respectively supplied with first output CP and second output DP of phase comparator 4.

As shown in Fig. 4A, for example, low-pass filter 7 includes resistors 41 and 42 and capacitor 43. It is also possible to constitute low-pass filter 7 by resistors 44, 45, and 46 and capacitors 47 and 48 as shown in Fig. 4B.

As shown in Fig. 5, for example, each of first and second level conversion circuits 8 and 9 is constituted by two P-channel transistors 51 and 52 and one N-channel transistor 53.

The source-drain path of P-channel transistor 51 is connected between power source voltage terminal V_{cc} and node 54 from which voltage PV is derived, and the gate of transistor 51 is supplied with output voltage V_{off} of low-pass filter 7.

The source-drain path of P-channel transistor 52 is connected between power source voltage terminal V_{cc} and node 54, and the gate of transistor 52 is connected to node 54. The source-drain path of N-channel transistor 53 is connected between node 54 and the ground terminal.

In the case of first level conversion circuit 8, the gate of transistor 53 is supplied with reference voltage V_{ref} , and in the case of second level conversion circuit 9, the gate of transistor 53 is supplied with control voltage V_{cont} .

There will now be described the operation of PLL circuit section 1 of Fig. 1.

As shown in the timing chart of Fig. 6, first output CP of phase comparator 4 is set at a high level ("H") when the delay time of variable delay circuit 3 including the delay time of inverter 5 is shorter than $T/2$ (T is a period of reference frequency signal F_{ref}). At this time, second output DP of phase comparator 4 is kept at a high level in a period by which the delay time is shorter than $T/2$. The high level portion of second output DP is supplied as a discharging pulse to charge pump circuit 6.

In charge pump circuit 6, N-channel transistor 36 of Fig. 3 is set conductive in the high level period of output DP, thereby discharging output 37. As a result, output voltage V_{off} of low-pass filter 7 is lowered. In this case, if reference voltage V_{ref} is kept constant at a voltage equal to half power source voltage V_{cc} , output voltage PV of level conversion circuit 8 will rise.

Assume now that output voltage V_{off} of low-pass filter 7 is supplied to the gate of P-channel transistor 51 and reference voltage V_{ref} is supplied to the gate of N-channel transistor 53. Then, a current flowing into P-channel transistor 51 increases when voltage V_{off} is lowered as described above, and thus voltage PV of node 54 rises. As a result, the resistance components of transfer gates 21 and 23 of each of the basic circuits in first variable delay circuit 3 of Fig. 2 increase, thereby increasing the delay time of variable delay circuit 3.

In contrast with the above case, when the delay time of variable delay circuit 3 including the delay time of inverter 5 is longer than $T/2$ (T is a period of reference frequency signal F_{ref}) as shown in the timing chart of Fig. 7, second output DP of phase comparator 4 is set at a low level ("L"). At this time, first output CP of phase comparator 4 is kept at a low level in a period by which the delay time is longer than $T/2$. The low level portion of first output CP is supplied as a charging pulse to charge pump circuit 6.

In charge pump circuit 6, P-channel transistor 35 of Fig. 3 is set conductive in the low level period of output CP, thereby charging output 37. As a result, output voltage V_{off} of low-pass filter 7 is raised. Thus, in this case, voltage PV of node 54 is lowered. As a result, the resistance components of transfer gates 21 and 23 of each of the basic circuits in first variable delay circuit 3 of Fig. 2 decrease, thereby reducing the delay time of variable delay circuit 3.

When the delay time of first variable delay circuit 3 is set equal to $T/2$ as shown in the timing chart of Fig. 8 and the PLL loop is set into the stable condition, outputs CP and DP of phase comparator 4 are respectively set at constant levels of "H" and "L". At this time, output PV of first level conversion circuit 8 is set at a constant potential level and the delay time of first variable delay circuit 3 is kept constant.

By performing the above operation, the delay time of variable delay circuit 3 can be precisely controlled.

In VCO section 2, if control voltage V_{cont} is set at the same level as reference voltage V_{ref} , the same inputs as those supplied to first level conversion circuit 8 of PLL section 1 are supplied to second level conversion circuit 9. As a result, the delay time of each basic circuit in second variable delay circuit 10 becomes equal to that of each basic circuit in first variable delay circuit 3 of PLL section 1.

In this case, delay time t for each stage of the basic circuit in first variable delay circuit 3 can be expressed as follows:

$$t = \frac{1}{F_{ref}} \times \frac{1}{2} \times \frac{1}{m} \dots (2)$$

Further, oscillation frequency F_{VCO} of the ring oscillator circuit formed of second variable delay circuit 10 and inverter 11 of VCO section 2 can be expressed as follows:

$$F_{VCO} = \frac{1}{t} \times \frac{1}{n} \times \frac{1}{2} = \frac{1}{2nt} \dots (3)$$

The following equation can be obtained by substituting equation (3) into equation (2).

$$F_{VCO} = \left(\frac{n}{m}\right) F_{ref} \quad (4)$$

In this way, oscillation frequency F_{VCO} of the ring oscillator circuit of VCO section 2 can be determined only by a ratio of the values of n and m and reference frequency signal F_{ref} . Therefore, the oscillation output with the stable center frequency can be obtained without receiving influence of variation in the manufacturing condition. Further, output PV of level conversion circuit 9 can be controlled by adequately changing the level of control voltage V_{cont} . Therefore, the delay time of variable circuit 10 can be changed

so as to control oscillation frequency F_{VCO} .

Fig. 9 shows an example of the characteristic of oscillation frequency signal F_{VCO} (Hz) with respect to control voltage V_{cont} (V). In Fig. 9, values V_{tha} , V_{thb} and V_{thc} of control voltage V_{cont} at which characteristic curves a, b, and c start to rise are threshold voltages of N-channel transistor 53 in the level conversion circuit of Fig. 5. That is, variation in the threshold voltage of transistor 53 affects oscillation frequency signal F_{VCO} as fluctuation in the manufacturing condition, and in general, the variation range is approx. 0.6 V.

The above characteristic can be obtained as follows. First, output voltage V_{off} of low-pass filter 7 is applied to the gate of P-channel transistor 51 and control voltage V_{cont} is applied to the gate of N-channel transistor 53 of Fig. 5 in second level conversion circuit 9 of VCO section 2. In this case, transistor 53 is kept nonconductive before control voltage V_{cont} exceeds the threshold voltage of transistor 53.

At this time, assume that transistor 51 supplied with voltage V_{off} is set in the conductive state. Then, transistor 52 is turned on if the potential difference between the gate and source thereof is larger than the threshold voltage of the P-channel transistor. However, voltage PV of output node 54 is set at the V_{CC} level by means of transistor 51 which is set in the conductive state. Therefore, the transfer gates (21, 23 in Fig. 2) in each basic circuit of variable second delay circuit 10 are turned off by output voltage PV . As a result, the ring oscillator circuit including second variable delay circuit 10 and inverter 11 will not oscillate. Therefore, as shown in Fig. 9, oscillation frequency signal F_{VCO} becomes 0 (Hz). When control voltage V_{cont} has exceeded the threshold voltage of transistor 53, characteristic curves a, b, and c start to rise. Each of characteristic curves a, b, and c passes center frequency F_c at which $V_{cont} = V_{ref}$.

As described above, with the level conversion circuit having the construction of Fig. 5, a characteristic curve of oscillator frequency signal F_{VCO} can be obtained which is first kept at a frequency of 0 Hz, starts to increase when V_{cont} has exceeded the threshold voltage of transistor 53, and then passes preset center frequency F_c .

Assume now that V_{CC} is 5 (V), V_{ref} is 2.5 (V), and threshold voltage V_{th} of N-channel transistor 53 is 1.2 (V), and F_{VCO} is set to 10 (MHz) when $V_{cont} = V_{ref} = 2.5$ (V). Then, it is possible to realize a VCO circuit which has a variable frequency range of 0 to 10 (MHz) with respect to the range of V_{cont} from 0 to 2.5 (V).

In a case where the level conversion circuit of Fig. 5 is used as level conversion circuits 8 and 9 in Fig. 1, the F_{VCO} characteristic curve starts to abruptly rise when V_{cont} shown by the characteristic diagram of Fig. 9 has exceeded the threshold voltage of transistor 53. That is, the inclination of each of characteristic curves a, b, and c becomes steeper and $\Delta F_{VCO}/\Delta V_{cont}$ becomes relatively large. As a result, noise introduced from the exterior into the VCO circuit of Fig. 1 may cause ΔF_{VCO} to significantly vary for a small amount of variation in ΔV_{cont} , so that the oscillation frequency may fluctuate. Further, the variable range of V_{cont} is narrowed by threshold voltage V_{thN} of the N-channel transistor with respect to the ground voltage.

In such a case, a circuit shown in Fig. 10 may be used as first and second level conversion circuits 8 and 9 to solve the above problem. That is, the level conversion circuit of Fig. 10 further includes N-channel transistor 55 whose source-drain path is connected between node 54 and the ground terminal and whose gate is supplied with constant voltage $E1$. In this case, constant voltage $E1$ is set higher than the threshold voltage of N-channel transistor 55, and transistor 55 is normally kept in the conductive state.

Since, in the level conversion circuit, transistor 55 is normally kept in the conductive state, voltage PV tends to change from V_{CC} towards the ground voltage, and is set to a stable voltage level determined by transistors 51, 52, 53 and 55. Therefore, the characteristic of oscillation frequency signal F_{VCO} (Hz) with respect to control voltage V_{cont} (V) becomes gentle as shown by characteristic curves a, b, and c in Fig. 11 when the size of transistor 55 is increased. Further, the variable range of V_{cont} can be widened to the ground voltage.

Fig. 12 is a circuit diagram showing the detail construction of the first and second level conversion circuits used in the VCO circuit in the above embodiment. In the case of the circuit of Fig. 12, the gate of N-channel transistor 55 in the circuit of Fig. 10 is not connected to receive constant voltage $E1$ but is connected to the drain thereof or output node 54 for voltage PV . When the gate of transistor 55 is supplied with substantially constant voltage $E1$ as shown in Fig. 10, a current flowing into transistor 55 becomes constant and transistor 55 functions as a constant current source. In contrast, when the gate of transistor 55 is connected to the drain thereof as shown in Fig. 12, transistor 55 is normally kept in the conductive state and substantially the same characteristic as in the case of Fig. 11 can be obtained.

Fig. 13 is a circuit diagram showing the detail construction of first and second level conversion circuits 8 and 9 used in the VCO circuit of the above embodiment. In the case of the circuit of Fig. 13, the gate of P-channel transistor 52 in the circuit of Fig. 5 is not connected to output node 54 for voltage PV but is connected to receive constant voltage $E2$. With this connection, transistor 52 is used as a constant current

load. Also, in this example, the same characteristic as shown in Fig. 9 can be obtained.

Fig. 14 is a circuit diagram showing another construction of the basic circuit used in each of variable delay circuits 3 and 10. In the basic circuit of Fig. 14, an input signal is serially supplied via first CMOS transfer gate 25 formed of P-channel and N-channel transistors, inverter 22, second CMOS transfer gate 26 formed of P-channel and N-channel transistors, and inverter 24 and is then output. The gates of the P-channel transistors of first and second CMOS transfer gates 25 and 26 are supplied with delay time control signal PV, and the gates of the N-channel transistors are supplied with another delay time control signal NV.

The voltage level of delay time control signal NV is set to be higher or lower according as the voltage level of delay time control signal PV becomes lower or higher, respectively.

Fig. 15 is a circuit diagram showing the detail construction of first and second level conversion circuits 8 and 9 in the case where variable delay circuits 3 and 10 are constituted by the basic circuits shown in Fig. 14.

The circuit of Fig. 15 is constituted by additionally providing P-channel transistor 56 and N-channel transistor 57 in the circuit of Fig. 5. The source-drain path of P-channel transistor 56 is connected between power source voltage Vcc and output node 58 for delay time control signal NV, and the gate thereof is connected to output node 54 for signal PV. Likewise, the source-drain path of N-channel transistor 57 is connected between output node 58 for signal NV and the ground terminal, and the gate thereof is connected to output node 58 for signal NV. Thus, transistors 56 and 57 are combined to constitute an inverter for inverting signal PV so that output voltage NV thereof will vary in a direction opposite to that of variation in input signal PV.

In the level conversion circuit of Fig. 15, the amount of variation in signal NV with respect to the amount of variation in control voltage Vcont or reference voltage Vref supplied to the gate of transistor 53 tends to decrease. Therefore, a difference will occur between the amounts of variation in signals PV and NV for the same amount of variation in reference voltage Vref or control voltage Vcont. As a result, the amount of variation in the gate voltage of the N-channel transistors of first and second CMOS transfer gates 25 and 26 of the basic circuit shown in Fig. 14 becomes small. Therefore, the amount of variation in the delay time of the basic circuit becomes smaller so that the controllability of the oscillation frequency may be degraded.

If the difference between the amounts of variation in signals PV and NV may cause serious problems, it is preferable to use a level conversion circuit with the construction shown in Fig. 16 instead of the level conversion circuit shown in Fig. 15. In the level conversion circuit of Fig. 16, in order to compensate for the reduction in the amounts of variation in signal NV, N-channel transistor 59, P-channel transistor 60 and N-channel transistor 61 are additionally provided in the circuit of Fig. 15.

The source-drain path of transistor 59 is connected between output node 58 for signal NV and the ground terminal. The source-drain path of transistor 60 is connected between power source voltage terminal Vcc and gate node 62 of transistor 59, and the gate thereof is connected to node 62. Further, the source-drain path of transistor 61 is connected between node 62 and the ground terminal, and the gate thereof is connected to receive reference voltage Vref or control voltage Vcont.

With the above level conversion circuit, when reference voltage Vref or control voltage Vcont rises, PV is lowered and NV is raised. At this time, a voltage of node 62 is lowered by means of an inverter formed of transistors 60 and 61. As a result, a current flowing into transistor 59 decreases. In this way, transistor 59 functions to raise NV so as to compensate for reduction in the amount of variation in NV.

The voltage controlled oscillation circuit according to the above embodiment is constituted by MOS transistors, but it is also possible to a voltage controlled oscillation circuit by use of bipolar transistors.

Fig. 18 shows a PLL frequency synthesizer type tuning system including a voltage controlled oscillation circuit according to this invention. In the system of Fig. 18, PLL section 1 and VCO section 2 of Fig. 1 are used in the local oscillator of a super heterodyne type tuner. The construction of PLL section 1 and VCO section 2 may be the same as that of Fig. 1.

In Fig. 18, UHF or VHF television input signal Fin is input to super heterodyne tuner 101. In tuner 101, the frequency of input signal Fin is lowered (or divided) by means of a prescaler to obtain a high frequency signal of a desired frequency, if necessary. The high frequency signal is frequency-converted to intermediate frequency signal PIF of a preset frequency, using a beat between the high frequency signal and oscillation output Fvco of VCO section 2.

Control voltage Vcont for determining the oscillation frequency of VCO section 2 can be derived from band switching driver 102 and selectively set according to data Vcont from microcomputer (MPU) 200.

Reference frequency signal Fref supplied from tuner 101 is input to PLL section 1, and output Voff of PLL section 1 is supplied to VCO section 2 via an LPF circuit. (In Fig. 18, since an LPF is separately provided outside PLL section 1, PLL 7 in Fig. 1 can be omitted). Reference voltage Vref supplied to PLL section 1 can be obtained by D/A converting data Vref from MPU 200.

That is, when the user depresses a preset key of key matrix 201 to specify a desired reception channel, LED display 202 displays the reception channel. When the channel specification is input to MPU 200, MPU 200 supplies data Vref and Vcont corresponding to the specified reception channel to PLL section 1 and band switching driver 102, according to the program and data stored in memory 203.

For example, the channel specification may be effected by using a combination of remote control transmitter 204 and remote control receiver 205. The results of various specification by the remote control are supplied to on-screen display driver 206. Then, the RGB circuit of a CRT (not shown) is driven by means of driver 206, and the result of color adjustment or reception channel specified by the remote control is displayed on the CRT.

Tuner 101, switching driver 102, PLL section 1, LPF and the like are integrally formed as tuner pack 100 and can be manufactured and adjusted independently from the circuit of MPU 200.

As described above, according to this invention, the center frequency of the oscillation frequency can be determined by controlling the delay time of the variable delay circuit. Since the delay time can be precisely controlled by means of the phase-locked loop, a stable center frequency can be obtained without receiving any influence due to fluctuation in the manufacturing condition. Further, since the delay time is changed by the reference frequency signal, the center frequency can be freely set to a desired value and the frequency band of the oscillation frequency can also be freely set.

Claims

1. A voltage controlled oscillator circuit comprising:

a PLL section (1) for supplying a deviation signal (Voff) according to a received reference frequency signal (Fref) and a received reference voltage (Vref); and a VCO section (2) for supplying an oscillation output (Fvco) according to the deviation signal (Voff) and received control voltage (Vcont);

said PLL section (1) comprising:

first delay means (3, 5) for delaying the reference frequency signal (Fref) according to a preset first delay control signal (PV from 8) and outputting a delay signal (ND0);

phase difference detection means (4, 6, 7) for comparing the phase of the reference frequency signal (Fref) with that of the delay signal (ND0) and outputting the deviation signal (Voff) based on the phase difference; and

first delay control means (8) for outputting the first delay control signal (PV from 8) having a signal level corresponding to the preset reference voltage (Vref) and the deviation signal (Voff).

2. A circuit according to claim 1, characterized in that the delay time caused by said first delay means (3, 5) is selected to substantially one-half the period of the reference frequency signal (Fref).

3. A circuit according to claim 1, characterized in that said VCO section (2) includes:

second delay control means (9) for outputting a second delay control signal (PV from 9) producing a signal level corresponding to the control voltage (Vcont) and the deviation signal (Voff); and

second delay means (10, 11) for cyclically delaying the oscillation output (Fvco) according to the second delay control signal (PV from 9) and generating the oscillation output (Fvco).

4. A circuit according to claim 1, characterized in that said first delay means (3, 5) includes:

a plurality of transmission gates (21, 23); and a plurality of inverters (22, 24) alternately series-connected to said plurality of transmission gates (21, 23); and

the first delay control signal (PV from 8) is used as gate inputs of said plurality of transmission gates (21, 23).

5. A circuit according to claim 3, characterized in that said second delay means (10, 11) includes:

a plurality of transmission gates (21, 23); and a plurality of inverters (22, 24) alternately series-connected to said plurality of transmission gates (21, 23); and

the second delay control signal (PV from 9) is used as gate inputs of said plurality of transmission gates (21, 23).

6. A circuit according to claim 1, characterized in that said first delay means (3, 5) includes:

a plurality of CMOS transmission gates (25, 26); and a plurality of inverters (22, 24) alternately series-connected to said plurality of CMOS transmission gates (25, 26); and

the first delay control signal (PV from 8) is used as gate inputs of one channel (P) type gates of

That is, when the user depresses a preset key of key matrix 201 to specify a desired reception channel, LED display 202 displays the reception channel. When the channel specification is input to MPU 200, MPU 200 supplies data Vref and Vcont corresponding to the specified reception channel to PLL section 1 and band switching driver 102, according to the program and data stored in memory 203.

5 For example, the channel specification may be effected by using a combination of remote control transmitter 204 and remote control receiver 205. The results of various specification by the remote control are supplied to on-screen display driver 206. Then, the RGB circuit of a CRT (not shown) is driven by means of driver 206, and the result of color adjustment or reception channel specified by the remote control is displayed on the CRT.

10 Tuner 101, switching driver 102, PLL section 1, LPF and the like are integrally formed as tuner pack 100 and can be manufactured and adjusted independently from the circuit of MPU 200.

As described above, according to this invention, the center frequency of the oscillation frequency can be determined by controlling the delay time of the variable delay circuit. Since the delay time can be precisely controlled by means of the phase-locked loop, a stable center frequency can be obtained without
15 receiving any influence due to fluctuation in the manufacturing condition. Further, since the delay time is changed by the reference frequency signal, the center frequency can be freely set to a desired value and the frequency band of the oscillation frequency can also be freely set.

Claims

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1. A voltage controlled oscillator circuit comprising:
 - a PLL section (1) for supplying a deviation signal (Voff) according to a received reference frequency signal (Fref) and a received reference voltage (Vref); and a VCO section (2) for supplying an oscillation output (Fvco) according to the deviation signal (Voff) and received control voltage (Vcont);
 - 25 said PLL section (1) comprising:
 - first delay means (3, 5) for delaying the reference frequency signal (Fref) according to a preset first delay control signal (PV from 8) and outputting a delay signal (ND0);
 - phase difference detection means (4, 6, 7) for comparing the phase of the reference frequency signal (Fref) with that of the delay signal (ND0) and outputting the deviation signal (Voff) based on the phase difference; and
 - 30 first delay control means (8) for outputting the first delay control signal (PV from 8) having a signal level corresponding to the preset reference voltage (Vref) and the deviation signal (Voff).
 2. A circuit according to claim 1, characterized in that the delay time caused by said first delay means (3, 5) is selected to substantially one-half the period of the reference frequency signal (Fref).
 - 35 3. A circuit according to claim 1, characterized in that said VCO section (2) includes:
 - second delay control means (9) for outputting a second delay control signal (PV from 9) producing a signal level corresponding to the control voltage (Vcont) and the deviation signal (Voff); and
 - 40 second delay means (10, 11) for cyclically delaying the oscillation output (Fvco) according to the second delay control signal (PV from 9) and generating the oscillation output (Fvco).
 4. A circuit according to claim 1, characterized in that said first delay means (3, 5) includes:
 - 45 a plurality of transmission gates (21, 23); and a plurality of inverters (22, 24) alternately series-connected to said plurality of transmission gates (21, 23); and
 - the first delay control signal (PV from 8) is used as gate inputs of said plurality of transmission gates (21, 23).
 5. A circuit according to claim 3, characterized in that said second delay means (10, 11) includes:
 - 50 a plurality of transmission gates (21, 23); and a plurality of inverters (22, 24) alternately series-connected to said plurality of transmission gates (21, 23); and
 - the second delay control signal (PV from 9) is used as gate inputs of said plurality of transmission gates (21, 23).
 - 55 6. A circuit according to claim 1, characterized in that said first delay means (3, 5) includes:
 - a plurality of CMOS transmission gates (25, 26); and a plurality of inverters (22, 24) alternately series-connected to said plurality of CMOS transmission gates (25, 26); and
 - the first delay control signal (PV from 8) is used as gate inputs of one channel (P) type gates of



said plurality of CMOS transmission gates (25, 26) and an inverted signal (NV) of the first delay control signal (PV from 8) is used as gate inputs of the other channel (N) type gates of said plurality of CMOS transmission gates (25, 26).

- 5 7. A circuit according to claim 3, characterized in that said second delay means (10, 11) includes:
 a plurality of CMOS transmission gates (25, 26); and a plurality of inverters (22, 24) alternately series-connected to said plurality of CMOS transmission gates (25, 26); and
 the second delay control signal (PV from 9) is used as gate inputs of one channel (P) type gates of said plurality of CMOS transmission gates (25, 26) and an inverted signal (NV) of the second delay control signal (PV from 9) is used as gate inputs of the other channel (N) type gates of said plurality of CMOS transmission gates (25, 26).
- 10
8. A circuit according claim 1, characterized in that said phase difference detecting means (4, 6, 7) includes:
 15 a first D-type flip-flop (31) clocked by the reference frequency signal (Fref);
 a second D-type flip-flop (32) clocked by the delay signal (ND0);
 means (33) for resetting said first and second D-type flip-flops (31, 32) according to the logical product of Q outputs of said first and second D-type flip-flops (31, 32);
 a first transistor (35) of a first conductivity type (P) driven by an inverted signal (CP) of the Q output of said first D-type flip-flop (31);
 20 a second transistor (36) of a second conductivity type (N) driven by the Q output signal (DP) of said second D-type flip-flop (32); and
 means (7) for deriving the deviation signal (Voff) from a signal (37) which is obtained by combining outputs of said first and second transistors (35, 36).
- 25
9. A circuit according to claim 8, characterized in that said deriving means (7) includes a low-pass filter (Fig. 4) for filtering the combined signal (37) to output the deviation signal (Voff).
10. A circuit according to claim 1, characterized in that said first delay control means (8) includes:
 30 a first MOS transistor (51) of a first conductivity type (P) having a gate supplied with the deviation signal (Voff), a source connected to a first power source circuit (Vcc) and a drain for outputting the first delay control signal (PV from 8);
 a second MOS transistor (52) of the first conductivity type (P) having a source connected to said first power source circuit (Vcc) and a drain and a gate connected to the drain of said first MOS transistor (51); and
 35 a third MOS transistor (53) of a second conductivity type (N) having a gate supplied with the reference voltage (Vref), a source connected to a second power source circuit (Vss) and a drain connected to the drain of said first MOS transistor (51).

40 Patentansprüche

1. Eine spannungsgesteuerte Oszillatorschaltung, umfassend:
 einen PLL-Abschnitt (1) zum Zuführen eines Abweichungssignals (Vaus) gemäß eines empfangenen Referenzfrequenzsignals (Fref) und einer empfangenen Referenzspannung (Vref); und einen VCO-Abschnitt (2) zum Zuführen eines Oszillationsausgangs (Fvco) gemäß dem Abweichungssignal (Vaus) und einer empfangenen Steuerspannung (Vcont);
 wobei der PLL-Abschnitt (1) umfaßt:
 eine erste Verzögerungseinrichtung (3, 5) zum Verzögern des Referenzfrequenzsignals (Fref) gemäß einem voreingestellten ersten Verzögerungssteuersignal (PV von 8) und zum Ausgeben eines Verzögerungssignals (NDO);
 50 eine Phasendifferenz-Erfassungseinrichtung (4, 6, 7) zum Vergleichen der Phase des Referenzfrequenzsignals (Fref) mit derjenigen des Verzögerungssignals (NDO) und zum Ausgeben des Abweichungssignals (Vaus) auf der Grundlage der Phasendifferenz; und
 eine erste Verzögerungssteuereinrichtung (8) zum Ausgeben des ersten Verzögerungssteuersignals (PV von 8) mit einem Signalpegel entsprechend der voreingestellten Referenzspannung (Vref) und des Abweichungssignals (Vaus).
- 55



2. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die von der ersten Verzögerungseinrichtung (3, 5) verursachte Verzögerungszeit als im wesentlichen eine halbe Periode des Referenzfrequenzsignals (Fref) gewählt wird.
- 5 3. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß der VCO-Abschnitt (2) umfaßt:
eine zweite Verzögerungssteuereinrichtung (9) zum Ausgeben eines zweiten Verzögerungssteuersignals (PV von 9), welches einen Signalpegel entsprechend der Steuerspannung (Vcont) und des Abweichungssignals (Vaus) erzeugt; und
eine zweite Verzögerungseinrichtung (10, 11) zum zyklischen Verzögern des Oszillationsausgangs (Fvco) gemäß des zweiten Verzögerungssteuersignals (PV von 9) und zum Erzeugen des Oszillationsausgangs (Fvco).
- 10 4. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die erste Verzögerungseinrichtung (3, 5) umfaßt:
15 eine Vielzahl von TransfERGattern (21, 23); und eine Vielzahl von Invertern (22, 24), die alternierend mit der Vielzahl von TransfERGattern (21, 23) verbunden sind; und
daß das erste Verzögerungssteuersignal (PV von 8) als Gatter-Eingänge der Vielzahl von TranfERGattern (21, 23) verwendet wird.
- 20 5. Eine Schaltung nach Anspruch 3, dadurch gekennzeichnet, daß die zweite Verzögerungseinrichtung (10, 11) umfaßt:
eine Vielzahl von TransfERGattern (21, 23); und eine Vielzahl von Invertern (22, 24), die alternierend zu der Vielzahl der TransfERGatter (21, 23) in Reihe geschaltet sind; und
25 daß das zweite Verzögerungssteuersignal (PV von 9) als Gatter-Eingänge der Vielzahl von TransfERGattern (21, 23) verwendet wird.
6. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die erste Verzögerungseinrichtung (3, 5) umfaßt:
30 eine Vielzahl von CMOS-TransfERGattern (25, 26); und eine Vielzahl von Invertern (22, 24), die alternierend mit der Vielzahl von CMOS-TransfERGattern (25, 26) in Reihe geschaltet sind; und
daß das erste Verzögerungssteuersignal (PV von 8) als Gatter-Eingänge von Gattern eines Kanaltyps (P) der Vielzahl von CMOS-TransfERGattern (25, 26) und ein invertiertes Signal (NV) des ersten Verzögerungssteuersignals (PV von 8) als Gatter-Eingänge der Gatter eines anderen Kanal-Typs (N) der Vielzahl von CMOS-TransfERGattern (25, 26) verwendet wird.
- 35 7. Eine Schaltung nach Anspruch 3, dadurch gekennzeichnet, daß die zweite Verzögerungseinrichtung (10, 11) umfaßt:
eine Vielzahl von CMOS-TransfERGattern (25, 26); und eine Vielzahl von Invertern (22, 24), die mit der Vielzahl von CMOS-TransfERGattern (25, 26) alternierend in Reihe geschaltet sind; und
40 daß das zweite Verzögerungssteuersignal (PV von 9) als Gatter-Eingänge von Gattern eines Kanaltyps (P) der Vielzahl von CMOS-TransfERGattern (25, 26) und ein invertiertes Signal (NV) des zweiten Verzögerungssteuersignals (PV von 9) als Gatter-Eingänge von Gattern des anderen Kanaltyps (N) der Vielzahl von CMOS-TransfERGattern (25, 26) verwendet wird.
- 45 8. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Phasendifferenz-Erfassungseinrichtung (4, 6, 7) umfaßt:
ein erstes D-Typ-Flip-Flop (31), welches durch das Referenzfrequenzsignal (Fref) getaktet wird;
ein zweites D-Typ-Flip-Flop 32, welches durch das Verzögerungssignal (NDO) getaktet wird;
eine Einrichtung (33) zum Zurücksetzen der ersten und zweiten D-Flip-Flops (31, 32) entsprechend
50 dem logischen Produkt von Q-Ausgängen der ersten und zweiten D-Typ-Flip-Flops (31, 32);
einen ersten Transistor (35) eines ersten Leitfähigkeitstyps (P), der von einem invertierten Signal (CP) des Q-Ausgangs des ersten D-Typ-Flip-Flops (31) angesteuert wird;
einen zweiten Transistor (36) eines zweiten Leitfähigkeitstyps (N), der von dem Q-Ausgangssignal (DP) des zweiten D-Typ-Flip-Flops (32) angesteuert wird; und
55 eine Einrichtung (7) zum Ableiten des Abweichungssignals (Vaus) aus einem Signal (37), welches durch Kombination von Ausgängen der ersten und zweiten Transistoren (35, 36) erhalten wird.



9. Eine Schaltung nach Anspruch 8, dadurch gekennzeichnet, daß die Ableitungseinrichtung (7) ein Tiefpaßfilter (Fig. 4) zur Filterung des kombinierten Signals (37) umfaßt, um das Abweichungssignal (Vaus) auszugeben.

- 5 10. Eine Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die erste Verzögerungssteuereinrichtung (8) umfaßt:
 einen ersten MOS-Transistor (51) eines ersten Leitfähigkeitstyps (P) mit einem Gate, dem das Abweichungssignal (Vaus) zugeführt wird, einer an eine erste Energiequellschaltung (Vcc) angeschlossenen Source und einer Drain zum Ausgeben des ersten Verzögerungssteuersignals (PV von 8);
 10 einen zweiten MOS-Transistor (52) des ersten Leitfähigkeitstyps (P) mit einer Source, die an die erste Energiequellschaltung (Vcc) angeschlossen ist und einer Drain und einem Gate, die an die Drain des ersten MOS-Transistors (51) angeschlossen sind; und
 einen dritten MOS-Transistor (53) eines zweiten Leitfähigkeitstyps (N) mit einem Gate, dem die Referenzspannung (Vref) zugeführt wird, einer Source, die mit einer zweiten Energiequellschaltung (Vss) verbunden ist und einer Drain, die mit der Drain des ersten MOS-Transistors (51) verbunden ist.
 15

Revendications

1. Circuit d'oscillateur commandé en tension comprenant :

20 une section de boucle à verrouillage de phase (PLL) (1) pour appliquer un signal de déviation (Voff) en fonction d'un signal de fréquence de référence reçu (Fref) et d'une tension de référence reçue (Vref) ; et une section d'oscillateur commandé en tension (VCO) (2) pour appliquer une sortie d'oscillation (Fvoc) en fonction du signal de déviation (Voff) et d'une tension de commande reçue (Vcont) ;

25 ladite section PLL (1) comprenant :

un premier moyen de retard (3, 5) pour retarder le signal de référence (Fref) en fonction d'un premier signal de commande de retard pré-établi (PV depuis 8) et pour émettre en sortie un signal de retard (NDO) ;

30 un moyen de détection de différence de phase (4, 6, 7) pour comparer la phase du signal de fréquence de référence (Fref) à celle du signal de retard (NDO) et pour émettre en sortie le signal de déviation (Voff) sur la base de la différence de phase ; et

un premier moyen de commande de retard (8) pour émettre en sortie le premier signal de commande de retard (PV depuis 8) présentant un niveau de signal correspondant à la tension de référence pré-établie (Vref) et au signal de déviation (Voff).

35 2. Circuit selon la revendication 1, caractérisé en ce que le temps de retard provoqué par ledit premier moyen de retard (3, 5) est choisi de manière à valoir sensiblement la moitié de la période du signal de fréquence de référence (Fref).

40 3. Circuit selon la revendication 1, caractérisé en ce que ladite section VCO (2) inclut :

un second moyen de commande de retard (9) pour émettre en sortie un second signal de commande de retard (PV depuis 9) en produisant un niveau de signal correspondant à la tension de commande (Vcont) et au signal de déviation (Voff) ; et

45 un second moyen de retard (10, 11) pour retarder cycliquement la sortie d'oscillation (Fvoc) en fonction du second signal de commande de retard (PV depuis 9) et pour générer la sortie d'oscillation (Fvco).

4. Circuit selon la revendication 1, caractérisé en ce que ledit premier moyen de retard (3, 5) inclut :

50 une pluralité de portes de transmission (21, 23) et une pluralité d'inverseurs (22, 24) connectés en alternance en série à ladite pluralité de portes de transmission (21, 23) ; et

le premier signal de commande de retard (PV depuis 8) est utilisé en tant qu'entrées de portes de ladite pluralité de portes de transmission (21, 23).

5. Circuit selon la revendication 3, caractérisé en ce que ledit second moyen de retard (10, 11) inclut :

55 une pluralité de portes de transmission (21, 23) et une pluralité d'inverseurs (22, 24) connectés en alternance en série à ladite pluralité de portes de transmission (21, 23) ; et

le second signal de commande de retard (PV depuis 9) est utilisé en tant qu'entrées de portes de ladite pluralité de portes de transmission (21, 23).



6. Circuit selon la revendication 1, caractérisé en ce que ledit premier moyen de retard (3, 5) inclut :
 une pluralité de portes de transmission CMOS (25, 26,) et une pluralité d'inverseurs (22, 24) connectés en alternance en série à ladite pluralité de portes de transmission CMOS (25, 26) ; et
 le premier signal de commande de retard (PV depuis 8) est utilisé en tant qu'entrées de portes pour les portes du type à canal d'un certain type (P) de ladite pluralité de portes de transmission CMOS (25, 26) et un signal inversé (NV) du premier signal de commande de retard (PV depuis 8) est utilisé en tant qu'entrées de portes pour les portes du type à canal de l'autre type (N) de ladite pluralité de portes de transmission CMOS (25, 26).
7. Circuit selon la revendication 3, caractérisé en ce que ledit second moyen de retard (10, 11) inclut :
 une pluralité de portes de transmission CMOS (25, 26,) et une pluralité d'inverseurs (22, 24) connectés en alternance en série à ladite pluralité de portes de transmission CMOS (25, 26) ; et
 le second signal de commande de retard (PV depuis 9) est utilisé en tant qu'entrées de portes pour les portes du type à canal d'un premier type (P) de ladite pluralité de portes de transmission CMOS (25, 26) et un signal inversé (NV) du second signal de commande de retard (PV depuis 9) est utilisé en tant qu'entrées de portes pour les portes du type à canal de l'autre type (N) de ladite pluralité de portes de transmission CMOS (25, 26).
8. Circuit selon la revendication 1, caractérisé en ce que ledit moyen de détection de différence de phase (4, 6, 7) inclut :
 une première bascule de type D (31) cadencée par le signal de fréquence de référence (Fref) ;
 une seconde bascule de type D (32) cadencée par le signal de retard (NDO) ;
 un moyen (33) pour remettre à l'état initial lesdites première et seconde bascules de type D (31, 32) en fonction du produit logique des sorties Q desdites première et seconde bascules de type D (31, 32) ;
 un premier transistor (35) d'un premier type de conductivité (P) piloté par un signal inversé (CP) de la sortie Q de ladite première bascule de type D (31) ;
 un second transistor (36) d'un second type de conductivité (N) piloté par le signal de sortie Q (DP) de ladite seconde bascule de type D (32) ; et
 un moyen (7) pour dériver le signal de déviation (Voff) à partir d'un signal (37) qui est obtenu en combinant des sorties desdits premier et second transistors (35, 36).
9. Circuit selon la revendication 8, caractérisé en ce que ledit moyen de dérivation (7) inclut un filtre passe-bas (figure 4) pour filtrer le signal combiné (37) afin d'émettre en sortie le signal de déviation (Voff).
10. Circuit selon la revendication 1, caractérisé en ce que ledit premier moyen de retard (8) inclut :
 un premier transistor MOS (51) d'un premier type de conductivité (P) comportant une grille qui se voit appliquer le signal de déviation (Voff), une source connectée à un premier circuit d'alimentation (Vcc) et un drain pour émettre en sortie le premier signal de commande de retard (PV depuis 8) ;
 un second transistor MOS (52) du premier type de conductivité (P) comportant une source connectée audit premier circuit d'alimentation (Vcc) et un drain ainsi qu'une grille connectés au drain dudit premier transistor MOS (51) ; et
 un troisième transistor MOS (53) d'un second type de conductivité (N) comportant une grille qui se voit appliquer la tension de référence (Vref), une source connectée à un second circuit d'alimentation (Vss) et un drain connecté au drain dudit premier transistor MOS (51).

