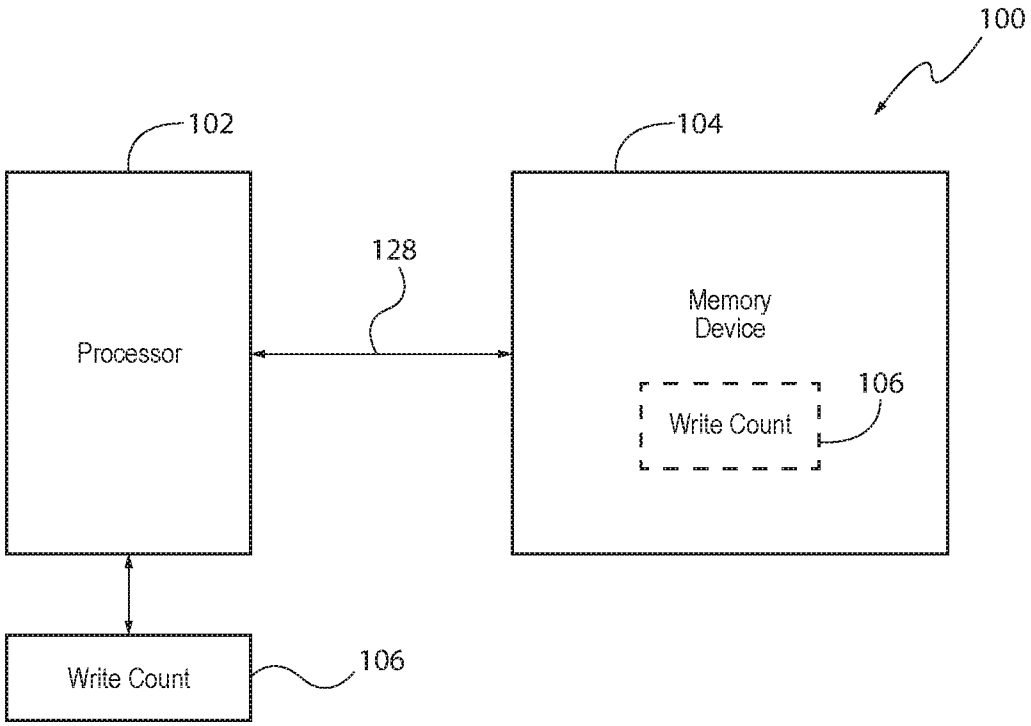
100
102
104
128
Processor
Memory Device
106
Write Count
Write Count
106

FIG. 1A

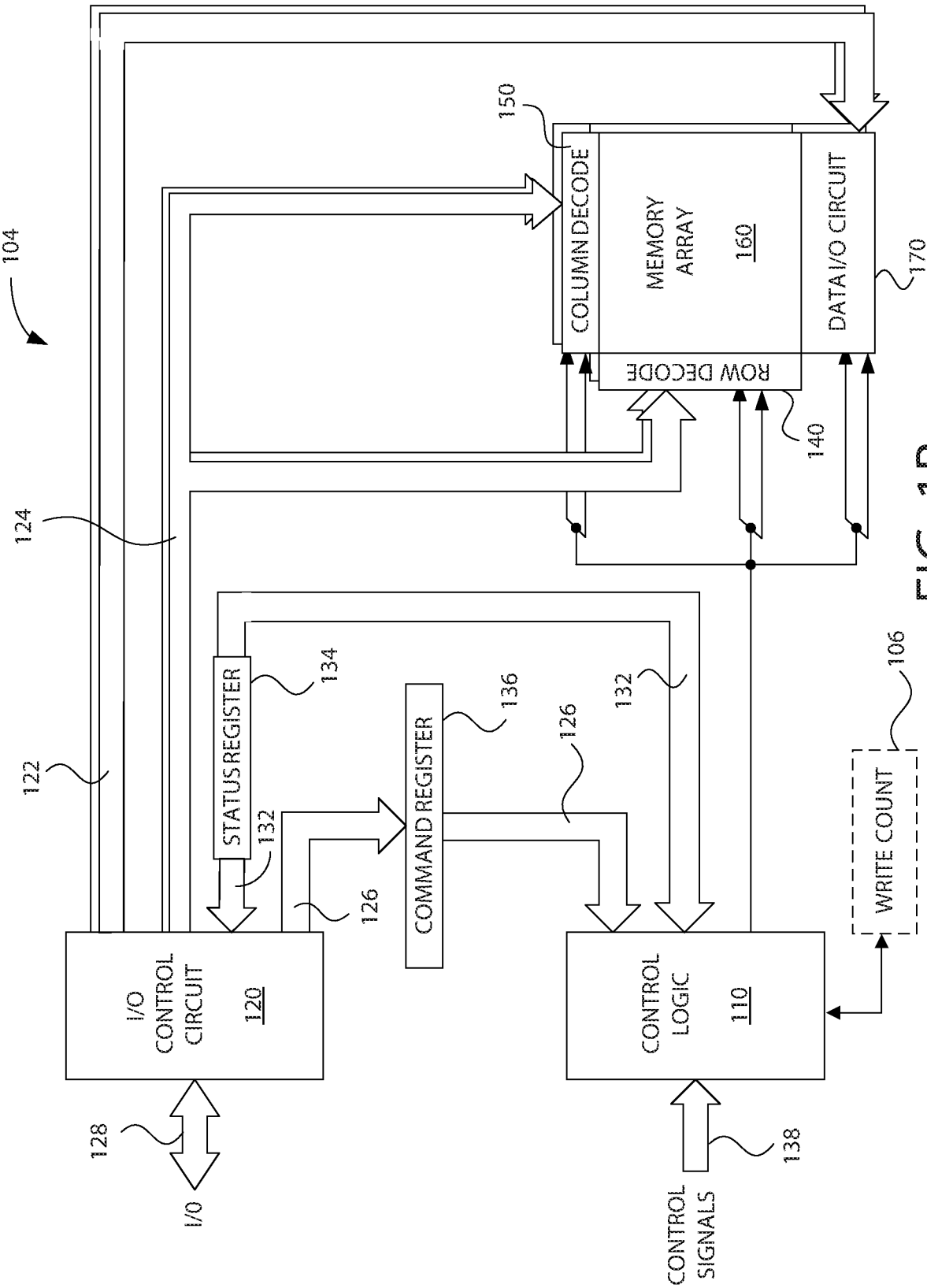
104
150
COLUMN DECODE
MEMORY ARRAY 160
DATA I/O CIRCUIT
170
ROW DECODE
140
124
122
STATUS REGISTER
134
132
COMMAND REGISTER
136
126
132
106
WRITE COUNT
126
I/O CONTROL CIRCUIT 120
CONTROL LOGIC 110
128
I/O
CONTROL SIGNALS
138

FIG. 1B

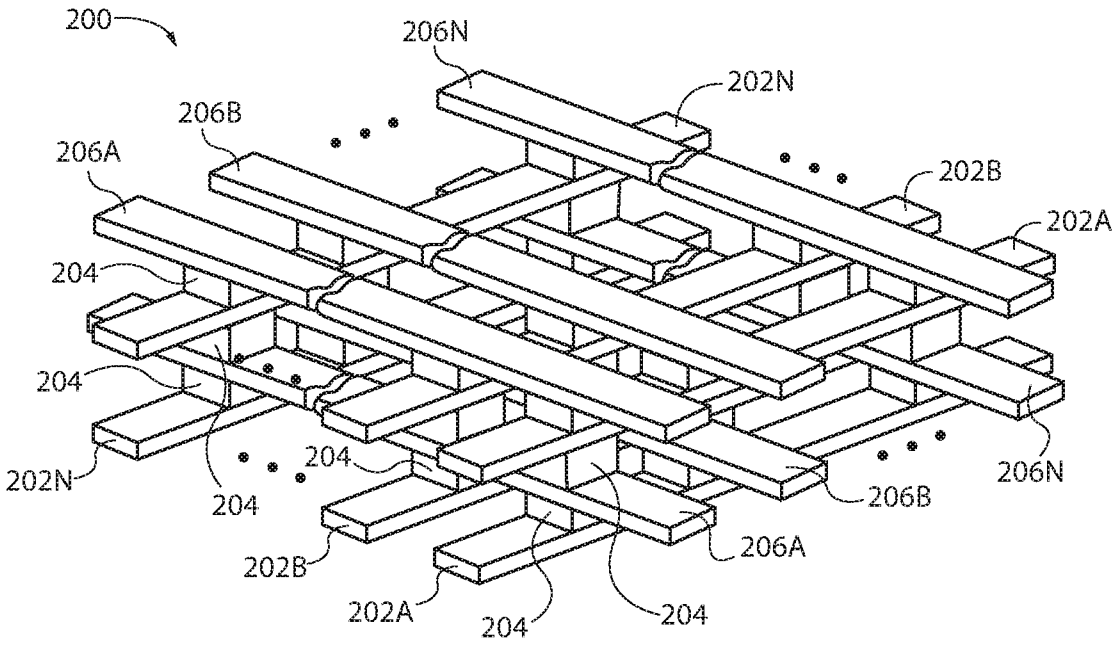
200
206N
202N
206B
206A
202B
202A
204
204
204
202N
204
204
206B
206N
206A
202B
202A
204
204

FIG. 2

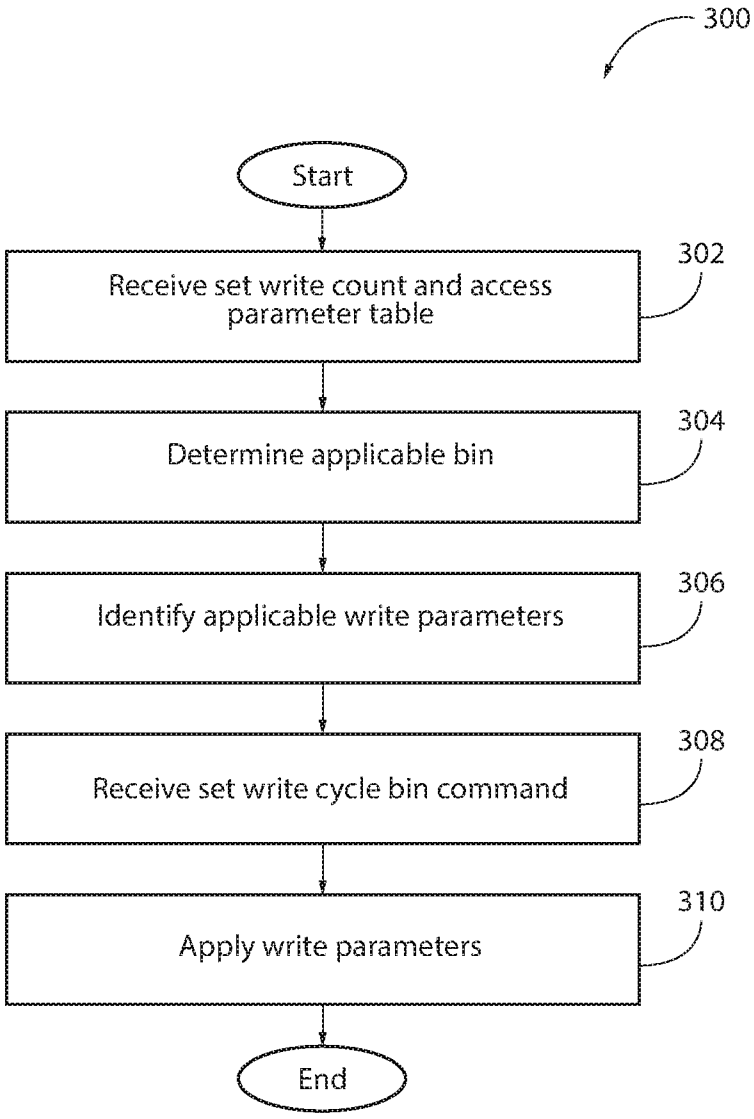
300
Start
Receive set write count and access parameter table
302
Determine applicable bin
304
Identify applicable write parameters
306
Receive set write cycle bin command
308
Apply write parameters
310
End

FIG. 3

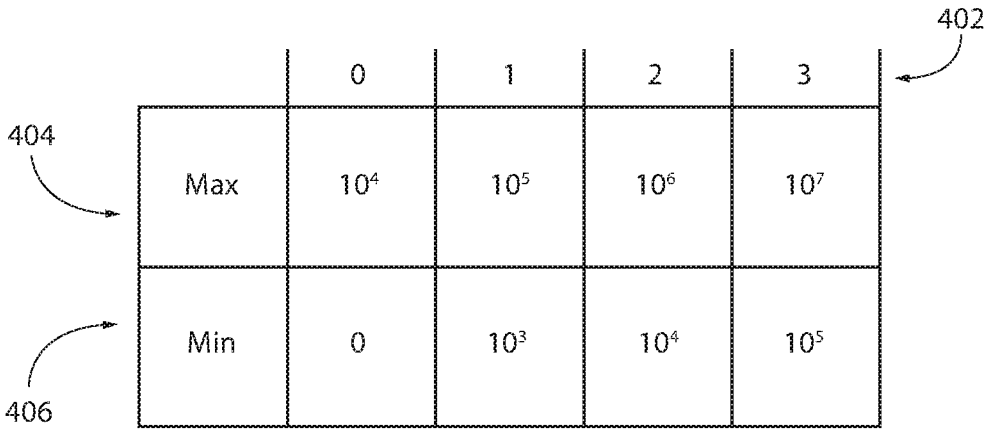

FIG. 4

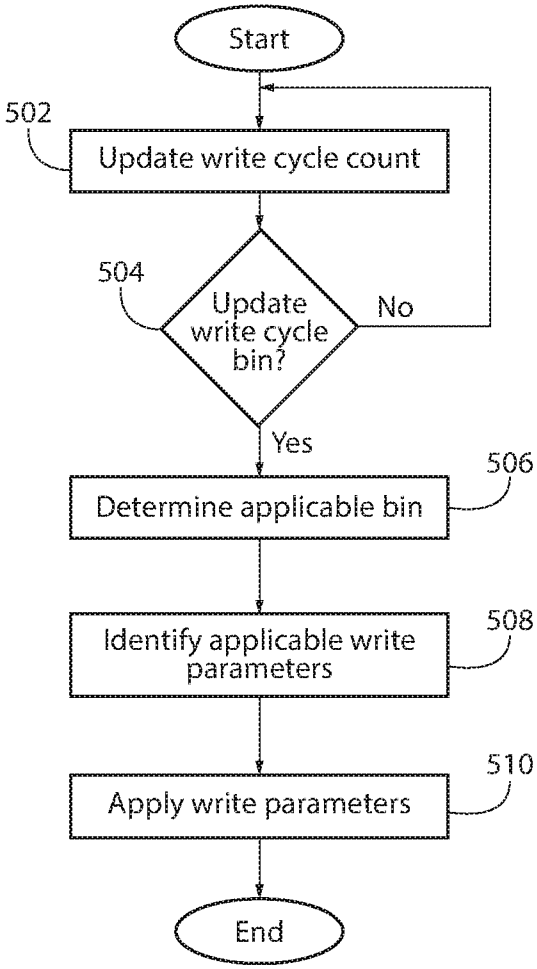
Start
502
Update write cycle count
504
Update write cycle bin?
No
Yes
506
Determine applicable bin
508
Identify applicable write parameters
510
Apply write parameters
End

FIG. 5