CLAIMS:

The invention claimed is:

1. A method to form electronic device fins comprising:

etching away a thickness of a substrate between first top surface areas of a substrate of a first single crystal material to form wide electronic device fins under the first top surface areas and to form trenches between the first top surface areas, the wide electronic device fins having wide single crystal top surfaces and wide sidewalls; then

forming a first thickness of a trench oxide material in the trenches and below the first top surface areas; and then

etching a thickness of the wide single crystal top surfaces and the wide sidewalls of the wide electronic device fins to form narrower electronic device fins from the wide fins, the narrower electronic device fins having narrower single crystal top surfaces and narrower sidewalls with a same single crystal lattice as the wide single crystal top surfaces and the wide sidewalls, wherein etching the thickness of the wide single crystal top surfaces and the wide sidewalls includes removing a thickness of between a 1 nm and 15 nm of the wide single crystal top surfaces and the wide sidewalls.

2. The method of claim 1, further comprising:

after etching the thickness of the wide single crystal top surfaces and the wide sidewalls, without an air break of the treatment chamber, depositing a second single crystal material on the thinned top surfaces and thinned sidewalls to form clad electronic device fins, wherein the second single crystal material has a lattice spacing that is different than a lattice spacing of the first single crystal material.

3. The method of claim 1, further comprising:

prior to etching away the thickness of the substrate, forming hardmask patterns on the first top surface areas of the single crystal substrate where top surfaces of the electronic device fins are desired; then

after etching away the thickness of the substrate, removing the hardmasks; then

depositing a second thickness of a trench oxide material in the trenches formed by etching away the thickness of the substrate between the first top surface areas; then

polishing to remove a third thickness of the trench oxide material above the first top surface areas; and then

prior to etching the thickness of the wide single crystal top surfaces and the wide sidewalls, etching away a fourth thickness of the trench oxide material in the trenches to expose the wide single crystal sidewalls of the wide electronic device fins and to form the first thickness of a trench oxide material.

4. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises maintaining in the narrower single crystal top surfaces and narrower sidewalls, a single crystal lattice structure of the wide top surfaces and the wide sidewalls.

5. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises one of (1) etching using chlorine based chemistry using low ion energy plasma processing, or (2) etching using thermal processing.

6. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises etching using chlorine based chemistry and using less than 5 kW of radio frequency energy for between 10 and 40 seconds.

7. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises etching using chlorine based chemistry and using less than 1 kW of radio frequency energy for between 10 and 40 seconds.

8. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises etching using thermal processing and using less than 900 degrees Celsius heat in an epitaxial deposition chamber for between 30 and 120 seconds in presence of HCl.

9. The method of claim 1, wherein etching the wide top surfaces and the wide sidewalls comprises etching using thermal processing and using less than 700 degrees Celsius heat in an epitaxial deposition chamber for between 30 and 120 seconds in presence of Cl2.

10. The method of claim 1, wherein etching the thickness of the wide single crystal top surfaces and the wide sidewalls includes one of: (1) removing a thickness of between a 8 nm and 10 nm of the wide single crystal top surfaces and the wide sidewalls, or (2) forming the etched fins by trimming a width of the wide fins from greater than 10 nm to 30 nm to a width of the narrower fins of less than 7 nm to 15 nm.

11. The method of claim 1, further comprising:
after etching the thickness of the wide single crystal top surfaces and the wide sidewalls, without an air break of the treatment chamber, depositing a second single crystal material on the thinned top surfaces and thinned sidewalls to form clad electronic device fins, wherein the second single crystal material has a lattice spacing that is different than a lattice spacing of the first single crystal material.

12. The method of claim 11, wherein the first single crystal material is Silicon and the second single crystal material is SiGe, and wherein depositing the second single crystal material comprises depositing a thickness of between a 5 nm and 15 nm of the second single crystal material on the thinned top surface and the thinned sidewalls.

13. The method of claim 11, wherein a width of the clad electronic device fins is equal to or less than 20 nm wide.

14. The method of claim 11, further comprising forming a PMOS device from the clad electronic device fins, wherein forming the PMOS device comprises:
forming a gate on the second single crystal material; and
forming junction regions adjacent to the gate and in the second single crystal material.