Method and Arrangement for Transformation of Signals from a frequency to a time domain

ABSTRACT

An IDCT method decimates a 2-D IDCT into two 1-D IDCT operations and then operates separately on the even and odd pixel input words. In a common processing step, selected input values are passed directly to output adders and subtractors, while others are multiplied by constant, scaled cosine values. In a pre-common processing step, the lowest-order odd input word is pre-multiplied by $\sqrt{2}$, and the odd input words are summed pairwise before processing in a common processing step. In a post-common processing step, intermediate values corresponding to the processed odd input words are multiplied by predetermined coefficients to form odd resultant values. After calculation of the even and odd resultant values, the high-order and low-order outputs are formed by simple subtraction/addition, respectively, of the odd resultant values from/with the even resultant values. The input values are preferably scaled upward by a factor of $\sqrt{2}$. Selected bits of some intermediate resulting data words are optionally adjusted by forcing these bits to either "1" or "0".

The IDCT system includes a pre-common processing circuit (PREC), a common processing circuit (CBLK), and a post-common processing circuit (POSTC), which perform the necessary operations in the respective steps. The system also includes a controller (CNTL) to generate signals to control the loading of system latches and, preferably, to time-multiplex the application of the even and odd input words to latches in the pre-common circuit.

FIGURE 1

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