

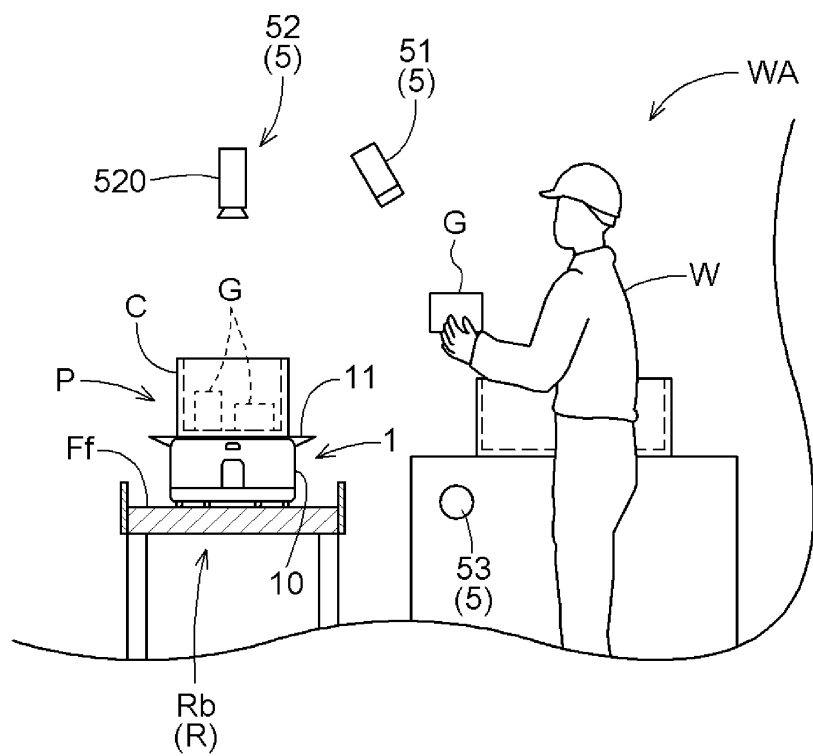
Figure 1 is a plan view of a semiconductor device 100, divided into a first stage (1階) and a second stage (2階). The device is shown with a coordinate system where X is the horizontal axis (X1 to the left, X2 to the right) and Y is the vertical axis. A flow direction U is indicated by arrows.

First Stage (1階): This stage includes a substrate 1 with a grid of elements 30. A central channel 3 is formed. Various components are labeled: SA (source/drain), W (gate), G (gate), C (contact), P (pad), L1 (lead), L2 (lead), WA (wafer), 5 (element), Cp (capacitor), G (gate), 2 (element), and M (metal). The flow direction U is indicated by arrows.

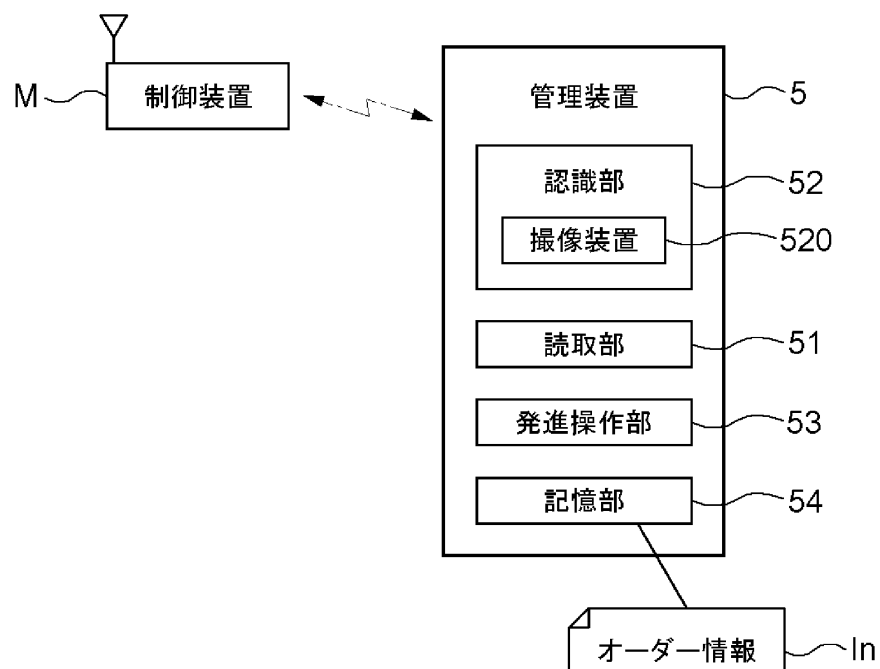
Second Stage (2階): This stage includes a substrate 1 with a grid of elements 30. A central channel 3 is formed. Various components are labeled: SA (source/drain), W (gate), G (gate), C (contact), P (pad), L1 (lead), L2 (lead), WA (wafer), 5 (element), Cp (capacitor), G (gate), 2 (element), and M (metal). The flow direction U is indicated by arrows.

The device 100 is shown with a coordinate system where X is the horizontal axis (X1 to the left, X2 to the right) and Y is the vertical axis. A flow direction U is indicated by arrows.

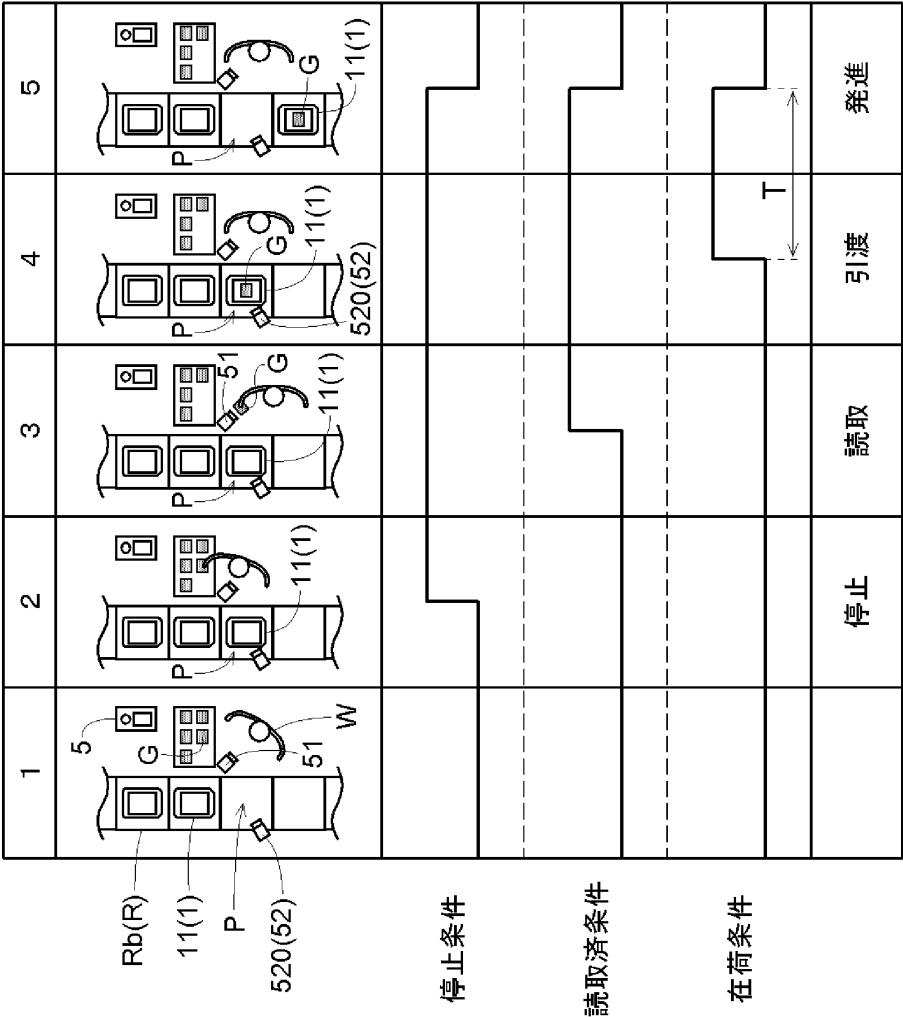
[図2]



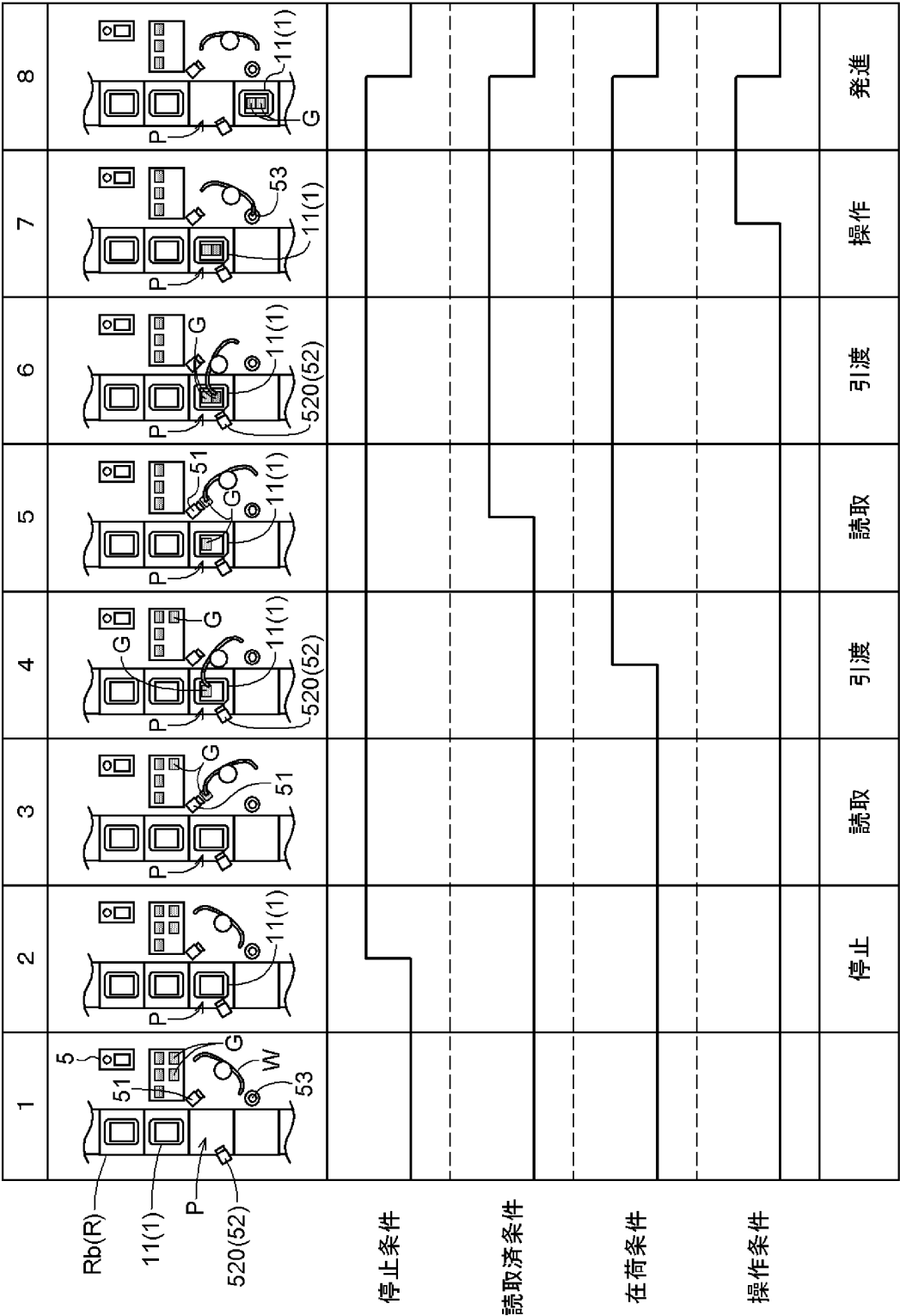
[図3]



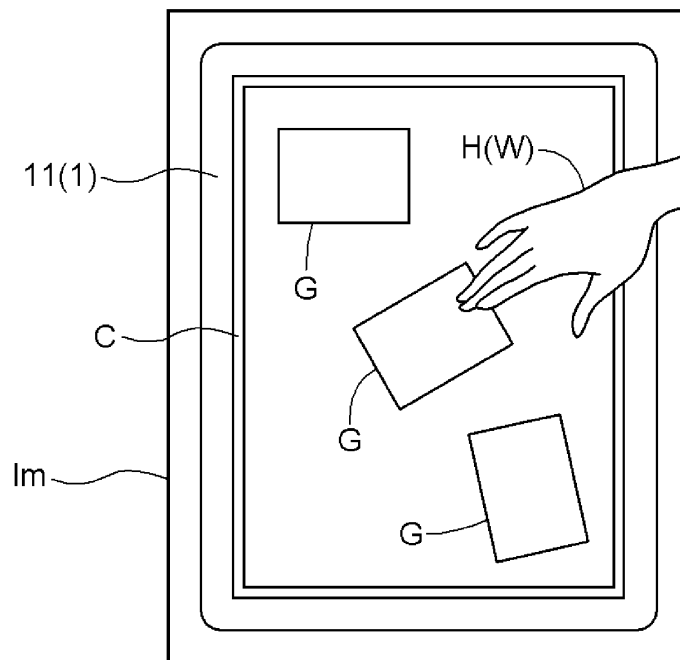
[図4]



[図5]



[図6]



[図7]

