

SEMICONDUCTOR APPARATUS AND METHOD FOR FABRICATING THEREOF

FIELD OF THE INVENTION

5 The disclosures made herein relate generally to a semiconductor apparatus, and more particularly to relates to a method for manufacturing a Surface Engineered Nitride (SEN) template and the use of the SEN template to fabricate a III-nitride semiconductor device stack thereon designated for applications in power and high frequency microelectronic devices.

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BACKGROUND OF THE INVENTION

 In recent years, there has been a growing demand for Gallium nitride (GaN)-based products because of an increasing adoption of a GaN power and radio frequency (RF) devices in a variety of applications, such as military,
15 defence, aerospace and next generation telecommunication, i.e. fifth generation (5G) network. GaN-based materials have a wide bandgap, remarkable breakdown electrical field and high drift velocity which can be utilized for the fabrication of high power and high frequency devices.

 In particular semiconductor devices made thereof are able to operate at
20 environmentally unfriendly conditions which is unattainable by the existing Si- based electronics. In terms of applications, III-nitride materials, i.e. GaN, are generally heteroepitaxially grown on a substrate. Among various substrate materials, the silicon substrate is widely selected for the growth of epitaxial stack comprising III-nitride materials due to the lower substrate cost and flexible

scalability on substrate size. In terms of material property viewpoint, differences such as thermal expansion coefficient and lattice constant between III-nitride materials and silicon substrate can pose technological challenges, i.e. crack, defect, wafer bow, and crystal quality for practical applications.

5 However, despite the great promise displayed by GaN-on-Si RF electronics, there still remains few issues to be resolved. One such issue is the presence of parasitic channel formed at III-nitride/silicon interface. It is generally believed that the parasitic channel is formed by the diffusion of dopants into silicon substrate during the epi growth. Once diffused into the substrate, the
10 dopants produce free carriers to generate a conductive channel, the so-called parasitic channel which is particularly significant giving rise to parasitic loss in layer stack deposited on high-resistivity silicon substrates. The formation of parasitic channel will lead to parasitic loss which will severely degrade the output power, power gain and efficiency of devices especially when they are operating
15 at high frequency. Accordingly, it is of particular importance to inhibit or reduce the formation of parasitic channel in order to realize the high frequency and high power application utilizing GaN-on-Si epi wafers.

SUMMARY OF THE INVENTION

20 The present invention relates to a method for fabricating a semiconductor apparatus. The method includes providing a surface engineered nitride (SEN) template. Further, the method includes forming a III-nitride semiconductor device stack on the SEN template. The III-nitride semiconductor device stack comprises an Aluminum nitride (AlN) layer, a buffer structure and a device structure. The

SEN template is formed by growing a template layer on a substrate within a process temperature range of 700°C to 950°C. The process temperature is cooled down to room temperature after the growth of the template layer on the substrate.

In an embodiment, the template layer comprises an Aluminum (Al) containing nitride formed by a Metal Organic Chemical Vapor Deposition (MOCVD) at the process temperature range of 700°C to 950°C, and wherein the template layer (101) has a thickness ranging from 5 nm to 1 μm.

In an embodiment, the SEN template is stored at a room temperature between 20°C to 25°C under the humidity of 50~60% for more than one day.

10 In an embodiment, the SEN template acts as at least one of a diffusion barrier for p-type dopant and a nucleation layer for an epitaxial growth of III-nitride semiconductor device.

In an embodiment, the AlN layer is formed on the SEN template.

In an embodiment, the buffer structure comprises a strain mitigating layer (SML) and a Gallium nitride (GaN) buffer layer.

15 In an embodiment, the SML includes a first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer directly overlying and in contact with the AlN layer (102), where x is within the range of 0.65 to 0.9, a second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer directly overlying and in contact with the first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, where y is within the range of 0.4 to 0.55; and a third graded $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer directly overlying and in contact with the second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer, where z is within the range of 0.25 to 0.35.

20 In an embodiment, the SML layer is doped by impurities, wherein the impurities comprise carbon, iron, and magnesium, wherein a dopant concentration is in the range of 5×10^{16} to 2×10^{20} ion/cm³.

In an embodiment, the GaN buffer layer is formed on the SML, wherein the GaN buffer layer is doped with impurity to increase the internal electrical resistance with a doping concentration in the range of 5×10^{16} to 2×10^{20} ion/cm³, wherein the impurity comprises a carbon, magnesium and an iron.

- 5 In an embodiment, the device structure comprises a GaN channel layer deposited on the GaN buffer layer, the AlGaIn barrier layer is deposited on the GaN buffer layer, and a GaN cap layer is deposited on the barrier layer.

In an embodiment, a thickness of the buffer structure is more than 1 μm .

In an embodiment, the substrate is made of a silicon.

- 10 In an embodiment, a thickness of the SEN template is less or equal 1 μm .

In an embodiment, the SEN template is provided on another SEN template.

In an embodiment, the buffer structure is epitaxially grown on the AlN layer.

- 15 The present invention relates to a semiconductor apparatus comprises a SEN template, and a III-nitride semiconductor device stack formed on the SEN template. The III-nitride semiconductor device stack comprises an AlN layer, a buffer structure and a device structure. The SEN template is formed by growing a template layer on a substrate within a process temperature range of 700°C to 20 950°C. The process temperature is cooled down to room temperature after the growth of the template layer on the substrate.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

5 **Figure 1** illustrates an example of a semiconductor apparatus in which a SEN template is grown on a silicon substrate, in accordance with one embodiment of the present invention.

Figure 2 shows an Atomic force microscopy (AFM) measurement result showing a surface of a SEN template grown on a silicon surface, according to one
10 embodiment of the present invention.

Figure 3 illustrates a schematic diagram of III-nitride semiconductor device stacks epitaxially grown on an SEN template, in accordance with one embodiment of the present invention.

Figure 4A and **Figure 4B** show a high resolution XRD rocking curve
15 scans for GaN (002) and GaN (102) planes, respectively, in accordance with one embodiment of the present invention.

Figure 5 is an illustration showing an AFM measurement result of a surface of a III-nitride semiconductor device stack epitaxially grown on a SEN template, in accordance with one embodiment of the present invention.

20 **Figure 6** is a carrier concentration profile as a function of depth in a silicon substrate obtained from a spreading resistance profiling (SRP), according to one embodiment of the present invention.

Figure 7 is a flow chart illustrating a method for fabricating a semiconductor apparatus, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Detailed description of preferred embodiments of the present invention is disclosed herein. It should be understood, however, that the embodiments are merely exemplary of the present invention, which may be embodied in various
5 forms. Therefore, the details disclosed herein are not to be interpreted as limiting, but merely as the basis for the claims and for teaching one skilled in the art of the invention. The numerical data or ranges used in the specification are not to be construed as limiting. The following detailed description of the preferred embodiments will now be described in accordance with the attached drawings,
10 either individually or in combination.

Accordingly, the embodiment herein is to provide method for fabricating a semiconductor apparatus. The method includes providing a surface engineered nitride (SEN) template. Further, the method includes forming a III-nitride semiconductor device stack on the SEN template. The III-nitride semiconductor
15 device stack comprises an Aluminum nitride (AlN) layer, a buffer structure and a device structure. The SEN template is formed by growing a template layer on a substrate within a process temperature range of 700°C to 950°C. The process temperature is cooled down to room temperature after the growth of the template layer on the substrate.

20 Unlike conventional methods, the present invention relates to a method of fabricating a semiconductor stack comprising of III-nitride materials epitaxially grown on a silicon substrate for high frequency and high power device applications. The method includes the deposition of a SEN template on a silicon substrate. The SEN template includes an Al-containing nitride layer deposited on

the surface of Si substrate, serving as anatomically smooth nucleation layer and III-nitride material stack is epitaxially grown thereon. More particularly the SEN template is designed to functions as a diffusion barrier of p-type dopants, which have been considered as the main reason resulting in the substrate parasitic loss.

5 Furthermore, the use of SEN template also improves the crystal quality of III- nitride materials since the presence of SEN template layer protects the underlying silicon substrate from attack of NH_3 during epitaxy and provides improvement of parasitic channel.

Referring now to the drawings and more particularly to **Figures 1 through**
10 **7**, where similar reference characters denote corresponding features consistently throughout the figures, there are shown preferred embodiments.

Figure 1 illustrates an example of a semiconductor apparatus (1000) in which a SEN template (200) grown on a silicon substrate (100), in accordance with one embodiment of the present invention. Referring specifically to Figure 1,
15 a schematic diagram of a SEN template (200) of a first embodiment of the present invention is illustrated. The SEN template (200) includes a silicon substrate (100) and a template layer (101). In an embodiment, the template layer (101) comprises an Al-containing nitride formed by a Metal Organic Chemical Vapor Deposition (MOCVD) at a process temperature range of 700~950°C, and the thickness of the
20 template layer (101) is about 10~100 nm. In an embodiment, the template layer (101) has a thickness ranging from 5 nm to 1μm. In an embodiment, the epitaxial process includes a Physical Vapor Deposition (PVD) process, a Molecular-beam epitaxy (MBE) process, an Atomic layer deposition (ALD) process or other applicable epitaxial process. After forming the SEN template (101), the template

substrate (200) is unloaded from the MOCVD reactor and properly stored at ambient temperature about 20~25°C with a controllable humidity of 50~55% for few days, i.e. 1~10 days. The SEN template (101) serves two primary purposes: Firstly, the SEN template (101) functions as a diffusion barrier for p-type dopant, 5 i.e. Aluminum (Al) or gallium (Ga), preventing them from an occurrence of thermal diffusion into the silicon substrate (100) so as to reduce the parasitic loss. Secondly, the SEN template (101) works as a nucleation layer for the following epitaxial growth of III-nitride semiconductor device stack (500). Further, the SEN template (200) presents crack-free and atomically smooth surface with a typical 10 roughness of <1 nm which is viable for fabricating semiconductor device structure thereon.

Figure 2 shows an Atomic force microscopy (AFM) measurement result (2000) showing a surface of the SEN template (200) grown on the silicon surface (100), according to one embodiment of the present invention.

15 **Figure 3** shows a schematic diagram of a III-nitride semiconductor device stack (1000). The III-nitride semiconductor device stack (1000) comprises the SEN template (200), a AlN layer, a buffer structure (300) and a device structure (400). The buffer structure (300) includes a strain mitigating layer (103) (SML) and a GaN buffer layer (104).

20 The SML layer (103) from a bottom to top sequentially comprises a first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer directly overlying and in contact with the AlN layer (102), where x is within the range of 0.65 to 0.9, a second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer directly overlying and in contact with the first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, where y is within the range of 0.4 to 0.55, and a third graded $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer directly

overlying and in contact with the second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer, where z is within the range of 0.25 to 0.35. In an embodiment, the SML layer (103) can be doped by impurities including carbon, iron, and magnesium. In an embodiment, the dopant concentration is in the range of 5×10^{16} to 2×10^{20} ion/cm³.

5 The GaN buffer layer (104) plays a crucial role in determining the electrical resistance of III-nitride semiconductor device stack (500) and has huge impact on breakdown voltage of transistor. In an embodiment, the GaN buffer layer (104) has a thickness ranging from 500 nm to about 6 μm . In an embodiment, the GaN buffer layer (104) can be doped with impurity, i.e. carbon or iron to
10 increase the internal electrical resistance with a doping concentration in the range of 5×10^{16} to 2×10^{20} ion/cm³ so as to resist higher operation voltage. In an embodiment, the GaN buffer layer (104) can be doped with impurity such as magnesium with a doping concentration in the range of 5×10^{16} to 2×10^{20} ion/cm³ so as to resist higher operation voltage.

15 Then a device structure (400) is formed on the buffer structure (300). The device structure (400) from bottom to top sequentially includes a channel layer (105) composed of GaN, a barrier layer (106) composed of $\text{Al}_a\text{Ga}_{1-a}\text{N}$ with $0 < a < 1$ and a cap layer (107) comprising GaN.

Figure 4A and Figure 4B show the FWHM of high resolution XRD
20 rocking curve (4000a and 4000b) for GaN(002) and GaN(102) planes, respectively.

As summarized in table 1, the crystal quality improvement for both GaN (002) and GaN (102) planes can be observed when growing the GaN buffer layer (104) on the SEN template (200) as compared to that grown on normal FZ Si substrate. In particular, significant reduction of FWHM for GaN (102) can be

seen, which suggests that the use of SEN template (200) effectively facilitates the filtration of edge dislocation propagating from the underneath layer stack.

The table1 summarizes the full width at half maximum (FWHM) results for the respective GaN (002) and GaN(102) plane.

5 Table1. FWHM for GaN (002) and GaN(102) planes.

XRD FWHM	SEN Template	FZ Si substrate
GaN(002)_arc sec	714	767
GaN(102)_arc sec	1268	1735

Figure 5A shows the smooth surface morphology (5umx5um) (5000a, 5000b) of III-nitride semiconductor device stack (500) grown on the SEN template (200). A low surface roughness of 0.22 nm with a clear step-flow growth mode is observed in the **Figure 5B**, suggesting high quality of epitaxial growth by the aid of the SEN template (200).

As determined by spreading resistance profiling (SRP), **Figure 6** is a plot (6000) of free carrier concentration as a function of depth in a substrate for III-nitride semiconductor device stacks grown on normal FZ silicon substrate and 15 SEN template, respectively. Qualitatively, when growing III-nitride semiconductor device stacks on the SEN template, much better SRP performance, i.e. lower peak concentration $\sim 2 \times 10^{15} \text{ 1/cm}^3$ and smaller drive-in depth $\sim 0.32 \text{ um}$ was obtained as compared to that when device stack was grown on normal FZ silicon substrate (peak concentration $\sim 2 \times 10^{16} \text{ 1/cm}^3$ and SRP drive-in depth ~ 0.37 20 um). Furthermore, a quantitative comparison can be done by extracting the total integrated p-type area by integrating the carrier concentration profile curve from

the substrate surface to the drive-in depth where the p-type carrier concentration is equal to the substrate background carrier concentration. More specifically, with the use of SEN template as a substrate for III-nitride semiconductor device stacks growth, the total integrated p-type area is 24 times smaller than that when grown
5 with normal FZ silicon substrate. The improved SRP performance indicates that the parasitic channel has been significantly reduced since SEN template is able to function effectively as a diffusion barrier, alleviating the thermal diffusion of p-type impurity during the epitaxial process.

Figure 7 is a flow chart illustrating a method (700) for fabricating a
10 semiconductor apparatus (1000) in accordance with one embodiment of the present invention. The method (700) includes providing a surface engineered nitride (SEN) template (702) and forming a III-nitride semiconductor device stack on the SEN template (704). The III-nitride semiconductor device stack comprises an Aluminum nitride (AlN) layer, a buffer structure and a device structure. The SEN
15 template is formed by growing the template layer on the substrate within a process temperature range of 700°C to 950°C. The process temperature is cooled down to room temperature after the growth of the template layer on the substrate.

Unlike conventional methods, the present invention relates to a method of fabricating a semiconductor stack comprising of III-nitride materials epitaxially
20 grown on a silicon substrate for high frequency and high power device applications. The method includes the deposition of a SEN template on a silicon substrate. The SEN template includes an Al-containing nitride layer deposited on the surface of the Si substrate, serving as an atomically smooth nucleation layer and III-nitride material stack is epitaxially grown thereon. More particularly the

SEN template is designed to functions as a diffusion barrier of p-type dopants, which have been considered as the main reason resulting in the substrate parasitic loss. Furthermore, the use of SEN template also improves the crystal quality of III-nitride materials since the presence of SEN template protects the underlying silicon substrate from attack of NH_3 during epitaxy and provides improvement of parasitic channel.

The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises", "comprising", "including" and "having" are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

15 The method steps, processes and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed. The use of the expression "at least" or "at least one" suggests the use of one or

20 more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

CLAIMS

We claim:

1. A method (700) for fabricating a semiconductor apparatus, the method comprises:
 - 5 i. providing a surface engineered nitride (SEN) template (702); and
 - ii. forming a III-nitride semiconductor device stack on the SEN template (704), wherein the III-nitride semiconductor device stack comprises an Aluminum nitride (AlN) layer, a buffer structure and a device structure, characterized in that the step of providing the SEN template includes:
 - 10 - growing a template layer on a substrate within a process temperature range of 700°C to 950°C, and
 - cooling down the process temperature to room temperature after the growth of the template layer on the substrate.
- 15 2. The method as claimed in claim 1, wherein the template layer comprises an Aluminum (Al) containing nitride formed by a Metal Organic Chemical Vapor Deposition (MOCVD) at the process temperature range of 700°C to 950°C, and wherein the template layer has a thickness ranging from 5 nm to 1µm.
- 20 3. The method as claimed in claim 1, wherein the SEN template is stored at a room temperature between 20°C to 25°C under the humidity of 50~60% for more than 24 hours.

4. The method as claimed in claim 1, wherein the SEN template acts as at least one of a diffusion barrier for p-type dopant and a nucleation layer for an epitaxial growth of III-nitride semiconductor device.
- 5 5. The method as claimed in claim 1, wherein the AlN layer is formed on the SEN template.
6. The method as claimed in claim 1, wherein the buffer structure comprises a strain mitigating layer (SML) and a Gallium nitride (GaN) buffer layer.
- 10 7. The method as claimed in claim 6, wherein the SML comprises:
- a) a first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer directly overlying and in contact with the AlN layer, where x is within the range of 0.65 to 0.9;
- b) a second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer directly overlying and in contact with
- 15 the first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, where y is within the range of 0.4 to 0.55; and
- c) a third graded $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer directly overlying and in contact with the second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer, where z is within the range of 0.25 to 0.35.
- 20 8. The method as claimed in claim 6, wherein the SML is doped by impurities, wherein the impurities comprise at least one of carbon, iron, and magnesium, wherein a dopant concentration is in the range of 5×10^{16} to 2×10^{20} ion/cm³.

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9. The method as claimed in claim 1, wherein the GaN buffer layer is formed on the SML, wherein the GaN buffer layer is doped with impurity to increase the internal electrical resistance with a doping concentration in the range of 5×10^{16} to 2×10^{20} ion/cm³, wherein the impurity comprises a carbon, magnesium and an iron.
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10. The method as claimed in claim 1, wherein the device structure comprises:
- a) a GaN channel layer;
 - b) a AlGaN barrier layer; and
 - 10 c) a GaN cap layer, wherein the GaN channel layer deposited on the GaN buffer layer, the AlGaN barrier layer is deposited on the GaN buffer layer, and the GaN cap layer is deposited on the barrier layer.
11. The method as claimed in claim 1, wherein a thickness of the buffer structure is more than 1 μm .
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12. The method as claimed in claim 1, wherein the substrate is made of silicon.
13. The method as claimed in claim 1, wherein a thickness of the SEN template is less or equal 1 μm .
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14. The method as claimed in claim 1, wherein the SEN template is provided on another SEN template.

15. The method as claimed in claim 1, wherein the buffer structure is epitaxially grown on the AlN layer.
16. A semiconductor apparatus (1000), the semiconductor apparatus (1000) comprises:
- 5 i. a surface engineered nitride (SEN) template (200); and
- ii. an III-nitride semiconductor device stack (500) formed on the SEN template (200), wherein the III-nitride semiconductor device stack (500) comprises an Aluminum nitride (AlN) layer (102), a buffer structure (300) and a device structure (400),
- 10 characterized in that the SEN template (200) is formed by growing a template layer (101) on a substrate (100) within a process temperature range of 700°C to 950°C, wherein the process temperature is cooled down to room temperature after the growth of the template layer (101)
- 15 on the substrate (100).
17. The semiconductor apparatus (1000) as claimed in claim 16, wherein the template layer (101) comprises an Aluminum (Al) containing nitride formed by a Metal Organic Chemical Vapor Deposition (MOCVD) at the process
- 20 temperature range of 700°C to 950°C, and wherein the template layer (101) has a thickness ranging from 5 nm to 1μm.
18. The semiconductor apparatus (1000) as claimed in claim 16, wherein the SEN template (200) is stored at a room temperature between 20°C to 25°C
- 25 under the humidity of 50~60% for more than 24 hours.

19. The semiconductor apparatus (1000) as claimed in claim 16, wherein the SEN template (101) acts as at least one of a diffusion barrier for p-type dopant and a nucleation layer for an epitaxial growth of III-nitride semiconductor device (500).
20. The semiconductor apparatus (1000) as claimed in claim 16, wherein the AlN layer (102) is formed on the SEN template (200).
21. The semiconductor apparatus (1000) as claimed in claim 16, wherein the buffer structure (300) comprises a strain mitigating layer (SML) (103) and a Gallium nitride (GaN) buffer layer (104).
22. The semiconductor apparatus (1000) as claimed in claim 21, wherein the SML comprises:
- a) a first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer directly overlying and in contact with the AlN layer (102), where x is within the range of 0.65 to 0.9;
 - b) a second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer directly overlying and in contact with the first graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, where y is within the range of 0.4 to 0.55; and
 - c) a third graded $\text{Al}_z\text{Ga}_{1-z}\text{N}$ layer directly overlying and in contact with the second graded $\text{Al}_y\text{Ga}_{1-y}\text{N}$ layer, where z is within the range of 0.25 to 0.35.
23. The semiconductor apparatus (1000) as claimed in claim 21, wherein the SML layer is doped by impurities, wherein the impurities comprise at least

one of a carbon, iron, and magnesium, wherein a dopant concentration is in the range of 5×10^{16} to 2×10^{20} ion/cm³.

24. The semiconductor apparatus (1000) as claimed in claim 16, wherein the
5 GaN buffer layer (104) is formed on the SML (103), wherein the GaN buffer layer (104) is doped with impurity to increase the internal electrical resistance with a doping concentration in the range of 5×10^{16} to 2×10^{20} ion/cm³, wherein the impurity comprises a carbon, magnesium and an iron.
- 10 25. The semiconductor apparatus (1000) as claimed in claim 16, wherein the device structure (400) comprises:
- a) a GaN channel layer (105);
 - b) a AlGaN barrier layer (106); and
 - c) a GaN cap layer (107), wherein the GaN channel layer (105) deposited
15 on the GaN buffer layer (104), the AlGaN barrier layer (106) is deposited on the GaN buffer layer (104), and the GaN cap layer (107) is deposited on the barrier layer (106).
26. The semiconductor apparatus (1000) as claimed in claim 16, wherein a
20 thickness of the buffer structure (300) is more than 1 μm .
27. The semiconductor apparatus (1000) as claimed in claim 16, wherein the substrate is made of silicon.

28. The semiconductor apparatus (1000) as claimed in claim 16, wherein a thickness of the SEN template (200) is less or equal 1 μm .
29. The semiconductor apparatus (1000) as claimed in claim 16, wherein the
5 SEN template (200) is provided on another SEN template.
30. The semiconductor apparatus (1000) as claimed in claim 16, wherein the buffer structure (300) is epitaxially grown on the AlN layer (102).