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SYSTEM AND METHOD OF IMPLEMENTING A WIRELESS
COMMUNICATION SYSTEM USING A RECONFIGURABLE
CHIP WITH A RECONFIGURABLE FABRIC

BACKGROUND OF THE INVENTION

5 The present invention relates to communication systems, more particularly to wireless communication systems.

Wireless communication systems are typically implemented using integrated circuits. For many situations, application-specific integrated chips (ASICs) are used to implement the communication system. This is especially done for wireless communication base stations, which can be used to service a large number of users. The desire for flexibility in the communication systems have led to the use of field programmable gate arrays (FPGAs) to implement a portion of the communication system. The FPGAs, however, have a considerable down side. The size and resulting cost of the FPGAs used to implement the complex algorithms used in wireless communication systems, especially base stations, can be significant. For this reason, it is desired to have a flexible yet inexpensive solution to the implementation of a computer communication system.

SUMMARY OF THE PRESENT INVENTION

20 The present invention comprises using a reconfigurable chip with a background and foreground configuration plane to implement a communication system. The wireless communication system can be a wireless communication system, for example, a wireless communication base station. The reconfigurable chip allows a portion of the communication system algorithm to be loaded into the background configuration plane while another portion of the communication system algorithm operates as configured by the foreground configuration plane.

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The configuration in the background plane can be quickly switched into the foreground plane. This is not possible with FPGAs. FPGAs require a significant amount of time (in the range of one second) for the configuration loading. While this is acceptable in many situations, for communication algorithms, such as the multiple-step frame processing used in a wireless communication base station, the configuration needs to be switched much quicker.

Another embodiment of the present invention comprises a method of implementing a communication system comprising the step of loading a first portion of the communication design in the reconfigurable chip; running the first portion of the reconfigurable chip, and at least during part of the running step; loading a second portion of the configuration system design in the reconfigurable chip, and running the second portion of the communication design on the reconfigurable chip.

Simultaneous loading of the background plane configuration and the operating of the foreground plane configuration allows for the communication algorithm to be implemented quickly and efficiently. Portions of the communication system design are switched in as needed without delays.

The use of the reconfigurable chip allows for the communication system design to be broken down into smaller configurations. This allows, for example, a smaller reconfigurable chip having foreground and background planes to be used in a situation where a larger FPGA would otherwise be needed. This can significantly reduce the cost of the communication system unit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates an example of a reconfigurable chip with foreground and background configuration planes which can be used with the system of the present invention.

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Fig. 2A illustrates a preferable implementation of the switching between the foreground and background planes.

Fig. 2B shows a less preferred implementation of the switching between the foreground and background planes.

5 Figs. 3A and 3B illustrate a single reconfigurable chip implemented such that it switches between three configuration functions.

Figs. 4A and 4B illustrate two reconfigurable chips, one of which is implemented to switch between two communication system configurations.

10 Figs. 5A and 5B illustrate the switching of a reconfigurable fabric between a path search configuration and a rake receiver configuration.

Fig. 6 is a flow chart illustrating the switching between a path searcher, rake receiver, and Viterbi configurations for a reconfigurable chip such as the system shown in Figs. 3A and 3B.

15 Fig. 7 is a diagram illustrating the switching of the communication system configurations for a reconfigurable chip as well as the central processing unit processing during the different configurations for one embodiment of the system of the present invention.

20 Figs. 8A and 8B illustrate a system using multiple reconfigurable chips, one of the reconfigurable chips switching between a Viterbi and Turbo configuration.

Fig. 9 illustrates a two-reconfigurable chip implementation of a CDMA communication system.

Fig. 10 illustrates the operation of the first reconfigurable chip in the system of Fig. 9.

25 Fig. 11 is a flow chart that illustrates the operation of the system shown in Fig. 10.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is an illustration of a reconfigurable chip 20 which can be used in one embodiment of the present invention. The reconfigurable chip includes a foreground configuration plane 22 and a background configuration plane 24. The foreground configuration plane 22 configures the elements of the reconfigurable fabric 26, such that a portion of the communication system design can be implemented. In a preferred embodiment, the reconfigurable chip 20 also includes a processor 28 such as a reduced instruction set computing (RISC) central processing unit (CPU). In one embodiment, the CPU 28 runs portions of a communication system algorithm which are difficult to implement in the reconfigurable fabric. The reconfigurable fabric 26, in a preferred embodiment, includes a number of configurable data path units, memory units, and interconnect elements. In one embodiment, the data path units include comparators, an arithmetic logic unit (ALU), and registers which are configurable to implement operations of the algorithm. In one embodiment, the reconfigurable fabric 26 also includes dedicated elements such as multipliers and memory elements. The memory elements can be used for storing data of the algorithm.

In a preferred embodiment, the configuration bits for the different configurations of the communication system are implemented by compiling the algorithm with a software compiler which allocates the reconfigurable elements in the reconfigurable fabric to portions of the algorithm. The external memory 30 can be used to store the different configurations for the communication system algorithm. These configurations can be loaded using the memory access unit 32 and bus 34 into the background plane. In a preferred embodiment, the background and foreground planes are interleaved with the reconfigurable elements in the fabric. The loading of the background plane is preferably done with a separate bus system from the data-connect lines used in the reconfigurable fabric 26.

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Additional details of the reconfigurable chip can be found from the disclosure of U.S. Patent No. 5,970,254, "An Integrated Processor And Programmable Data Path Chip for Reconfigurable Computer," issued to Laurence H. Cooke, et al., incorporated herein by reference.

5 Fig. 2A illustrates the preferred configuration of the switching between the foreground and background planes. The background configuration memory element 40 is loadable from the external memory, while the foreground configuration memory element 42 configures the configurable unit 44 within the reconfigurable fabric. When the background plane is activated, the data in the
10 background plane writes over the data in the foreground plane. If the old configuration needs to be run again, it is reloaded into the background plane.

 Fig. 2B shows an alternate and less preferred embodiment in which the background configuration element 40' and foreground configuration element 42' are connected to the configurable unit 44' using a multiplexer 46. Due to the
15 additional overhead of this embodiment, it has been found to be less preferable than the example of Fig. 2A.

 Figs. 3A and 3B illustrate a reconfigurable chip 50 which implements three portions of a wireless communication system. In this example, the reconfigurable chip 50 is part of a base station unit which implements, within a frame 52
20 operation time, three different configurations: a path search configuration 52a, a rake receiver configuration 52b, and a Viterbi configuration 52c. Note that in a conventional FPGA implementation, each of the configurations needs to be loaded in an FPGA chip at the same time. This requires the FPGA to be significantly greater than the size of a reconfigurable chip used with the present invention.
25 Note that during the operation of each of the configurations, another configuration is loaded into the background plane. Thus, when the operation of one of the portions of the communication system is finished, the reconfigurable chip can quickly switch to another configuration.

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Fig. 4A illustrates an alternate system in which two reconfigurable chips, reconfigurable chip 54 and reconfigurable chip 56, are used. As shown in Fig. 4B, in this embodiment within the frame operation time 58, a path search configuration 58a and rake receiver configuration 58b operate. The reconfigurable chip 56 is implemented with a Viterbi configuration.

Figs. 5A and 5B illustrate the switching between a path searcher configuration and a rake receiver configuration. An example of this switching is done at the transition between configurations 52a and 52b of Fig. 3B, and 58a and 58b of Fig. 4B.

In Fig. 5A, the foreground configuration memory 60 contains the path searcher configuration. This configures the reconfigurable fabric 62 into the path search configuration, and the reconfigurable fabric implements the path searching portion of the computer system. The rake receiver configuration is loaded into the background plane 64.

Note that the reconfigurable fabric includes a memory unit which can allow data from one configuration to be accessed by a second configuration without requiring data transfer.

Looking at Fig. 5B, when the path search configuration has finished operating, the rake receiver configuration from the background plane 64' can be loaded into the foreground plane 60'. This then almost instantaneously configures the reconfigurable fabric 62' in the rake receiver configuration, which can be completely different from the path search configuration. The switching, as shown in Figs. 5A and 5B, can be done within a single clock cycle, as long as there is sufficient time during the processing of the prior configuration to load the next configuration into the background plane.

Fig. 6 is a flow chart of the system of Figs. 3A and 3B. Note while one of the configurations is being loaded, the other configuration can be run concurrently.

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Fig. 7 illustrates the use of a reconfigurable chip in multiple configurations. This shows the reconfigurable fabric processing as well as the CPU processing. The CPU allows the calculation of portions of the communication algorithm difficult to implement on the reconfigurable fabric. It also provides a resource for
5 calculation which is separate from the reconfigurable fabric. The use of the CPU on a reconfigurable chip having a reconfigurable fabric thus provides advantages to implementing the communication system algorithm.

Fig. 8A illustrates an embodiment with multiple reconfigurable chips, some of the reconfigurable chips implementing a fixed configuration. The symbol rate
10 processor 70 switches between a Viterbi configuration 72a and a Turbo configuration 72b.

Figs. 9-11 illustrate an implementation of a wireless communication system following a U.S. standard for wireless Code Division Multiple Access (CDMA).

Fig. 9 illustrates an embodiment in which a reconfigurable chip 80
15 implements pseudo-random-number generation, demodulation, figure search and access search, while reconfigurable chip 82 implements the Viterbi and other processing.

Fig. 10 illustrates the switching between the different configurations in the reconfigurable chip 80 of Fig. 9.

20 Fig. 11 is a flow chart illustrating the operation of the reconfigurable chip 80 of Fig. 9.

Note that reconfigurable chips used in the present invention are especially useful in the base station operation of a wireless communication system. In the base station operation, multiple communication connections are operated
25 processed. The assignment of the number configurations to the different reconfigurable chips is partially determined by the number of users serviced by the base station and the resulting processing burden in each configuration. Large base stations may have many users and use more reconfigurable chips, some of which

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are dedicated to a single configuration. A base station working with fewer users may have more of the communication system configurations implemented on a single reconfigurable chip. The required processing speeds also affect this implementation arrangement.

5 Note that in the systems of Figs. 3-8, a pseudo-random-number generator is not shown. In one embodiment, the pseudo-random-number generator is implemented as a portion of the path searcher or rake receiver implementation, which may require additional configuration switching. Alternately, the pseudo-random-number generator can be implemented in a spare time slot. In one
10 embodiment, the pseudo-random-number generator is a gold-code generator.

 Additional details of one embodiment of an implementation of a communication system (a wireless base station) on a reconfigurable chip is given in the following appendices. Appendix 1 describes an overview of the path searching and rake receiver. Appendix 2 gives details of the rake receiver
15 embodiment including details of a gold-code generator. Appendix 3 gives details of the implementation of a Viterbi algorithm on a reconfigurable chip.

 It will be appreciated by those of ordinary skill in the art that the invention can be implemented in other specific forms without departing from the spirit or character thereof. The presently disclosed embodiments are therefore considered
20 in all respects to be illustrative and not restrictive. The scope of the invention is illustrated by the appended claims rather than the foregoing description, and all changes that come within the meaning and range of equivalents thereof are intended to be embraced herein.

What is claimed is:

1. A communication reconfigurable chip comprising:
a configurable memory to store first and second configurations; and
a reconfigurable logic unit responsive to the first and second configurations to implement an algorithm within a communication frame, wherein the first and second configurations program different operations within the reconfigurable chip based on the algorithm.
2. The communication reconfigurable chip of claim 1 wherein the first communication configuration implements a path search operation by the reconfigurable logic unit.
3. The communication reconfigurable chip of claim 1 wherein the second communication configuration implements a rake receiver operation by the reconfigurable logic unit.
4. The communication reconfigurable chip of claim 1 further including a third communication configuration to implement a Viterbi operation by the reconfigurable logic unit.
5. A method of implementing a communication system comprising:
loading a first configuration to configure a reconfigurable portion of an integrated circuit;
operating the reconfigurable portion of the integrated circuit with the first configuration;
loading a second configuration to configure the reconfigurable portion of the integrated circuit; and

operating the reconfigurable portion of the integrated circuit with the second configuration, wherein an algorithm is implemented by configuring the reconfigurable chip with the first and second configurations within one communication frame.

6. The method of claim 5 further comprising storing the first configuration in a first memory and the second configuration in a second memory.

7. The method of claim 5 further comprising storing the first configuration in a first block of a memory and the second configuration in a second block of the memory.

8. The method of claim 5 wherein operating the reconfigurable portion of the integrated circuit with the first configuration comprises a path searcher configuration.

9. The method of claim 5 wherein operating the reconfigurable portion of the integrated circuit with the second configuration comprises a rake receiver configuration.

10. A system comprising:

one or more bidirectional antenna(e) and;

a device coupled to the one or more bidirectional antenna(e), wherein the device includes,

a memory to store first and second configurations; and

a reconfigurable portion of the device responsive to the first and second configurations to implement within a communication frame an algorithm that uses the first and second configurations to provide different operations within the device.

11. A storage medium comprising content, which, when executed by a machine, causes the machine to:

load a first portion of the communication system design in a reconfigurable chip;

run the first portion of the communication system design on the reconfigurable chip in a foreground plane;

load a second portion of the communication system design in the reconfigurable chip in a background plane, at least during part of the running of the first portion; and

run the second portion of the communication system design on the reconfigurable chip by switching the background plane to the foreground plane, wherein the switching occurs within a communication frame and an algorithm implements different operations in the foreground plane and the background plane.

12. The storage medium of claim 11 wherein the communication system comprises a wireless communication system

13. The storage medium of claim 11 wherein the communication system is a part of a base station.