

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a lower semiconductor chip comprising a first semiconductor substrate, which comprises a first semiconductor device on an active surface thereof and a protrusion defined by a recess region on an inactive surface thereof opposite to the active surface, a plurality of external connecting pads on a bottom surface of the first semiconductor substrate, and a plurality of through-electrodes electrically connected to the plurality of external connecting pads; and

at least one upper semiconductor chip stacked on the protrusion of the lower semiconductor chip and electrically connected to the plurality of through-electrodes, the at least one upper semiconductor chip comprising a second semiconductor substrate which comprises a second semiconductor device on an active surface thereof,

wherein the at least one upper semiconductor chip has a horizontal area less than a horizontal area of the lower semiconductor chip to be superimposed on at least a portion of the protrusion in a vertical direction,

wherein the lower semiconductor chip further comprises a first cover insulating layer covering a top surface of the protrusion and not covering a side surface of the protrusion and a lower surface of the recess region, and the at least one upper semiconductor chip further comprises a second cover insulating layer covering the active surface of the second semiconductor substrate, and

wherein the first cover insulating layer and the second cover insulating layer are bonded together with a covalent bond.

2. The semiconductor package of claim 1, wherein the semiconductor package further comprises a plurality of bonded pads electrically connecting a space between the upper semiconductor chip and the plurality of through-electrodes penetrating the first cover insulating layer and the second cover insulating layer.

3. The semiconductor package of claim 2, wherein a bottom surface of the plurality of bonded pads and the lower surface of the recess region are at the same level.

4. The semiconductor package of claim 2, wherein the lower surface of the recess region is at a level lower than a bottom surface of the plurality of bonded pads.

5. The semiconductor package of any one of claims 1 to 4, wherein a side surface of the at least one upper semiconductor chip is aligned with the side surface of the protrusion in a vertical direction.

6. The semiconductor package of any one of claims 1 to 4, wherein the at least one upper semiconductor chip and the protrusion overlap each other in a vertical direction.

7. The semiconductor package of claim 1, further comprising: a plurality of chip connecting terminals electrically connecting the plurality of through-electrodes to the at least one upper semiconductor chip; and an underfill material layer configured to fill a space between a top surface of the protrusion and the at least one upper semiconductor chip to surround the plurality of chip connecting terminals, the underfill material layer extending outwardly therefrom.

8. The semiconductor package of claim 7, wherein the underfill material layer covers at least a portion of the side surface of the protrusion.

9. The semiconductor package of claim 7, wherein the underfill material layer covers the side surface of the protrusion and a portion of the lower surface of the recess region adjacent to the protrusion.

10. The semiconductor package of any one of claims 7 to 9, further comprising a molding member configured to cover a top surface of the lower semiconductor chip, a side surface of the at least one upper semiconductor chip, and the side surface of the protrusion, the molding member being configured to fill the recess region.

11. A semiconductor package comprising:
a lower semiconductor chip comprising a first semiconductor substrate, which comprises a first semiconductor device on an active surface thereof and a protrusion defined by a first recess region on an inactive surface thereof opposite to the active surface, a first cover insulating layer configured to cover a top surface of the protrusion and configured not to cover a side surface of the protrusion and a lower surface of the first recess region, a plurality of external connecting pads on a bottom surface of the first semiconductor substrate, and a plurality of first through-electrodes electrically connected to the plurality of external connecting pads;

at least one upper semiconductor chip comprising a second semiconductor substrate, stacked on the protrusion of the lower semiconductor chip and comprising a second semiconductor device on an active surface thereof, and a second cover insulating layer configured to cover the active surface of the second semiconductor substrate; and

a plurality of bonded pads across the first cover insulating layer and the second cover insulating layer, the plurality of bonded pads electrically connecting the at least one upper semiconductor chip to the plurality of first through-electrodes,

wherein the first cover insulating layer and the second cover insulating layer are bonded together with a covalent bond.

12. The semiconductor package of claim 11, wherein all of the at least one upper semiconductor chips are configured to overlap the protrusion in a vertical direction.

13. The semiconductor package of claim 11 or claim 12, wherein a horizontal area of the at least one upper semiconductor chip is identical to a horizontal area of a top surface of the protrusion.

14. The semiconductor package of any one of claims 11 to 13, wherein the plurality of bonded pads are diffusion-bonded to each other to form an integral body.

15. The semiconductor package of claim 11, wherein the at least one upper semiconductor chip comprises a first upper semiconductor chip and a second upper semiconductor chip stacked on the first upper semiconductor chip, in which respective side surfaces thereof are aligned with each other in a vertical direction.

16. The semiconductor package of claim 15, wherein the first upper semiconductor chip comprises a plurality of second through-electrodes electrically connected to the second upper semiconductor chip.

17. The semiconductor package of any one of claims 11 to 16, wherein the first semiconductor substrate comprises a plurality of second recess regions filled by the plurality of bonded pads, and the lower surface of the first recess region and a lower surface of the plurality of second recess regions are at an identical level.

18. A semiconductor package comprising:

a lower semiconductor chip comprising a first semiconductor substrate which comprises a first semiconductor device on an active surface thereof and a plurality of first through-electrodes configured to penetrate the first semiconductor substrate, the lower semiconductor chip comprising protrusions defined by recess regions on an inactive surface opposite to the active surface of the first semiconductor substrate;

a first upper semiconductor chip comprising a second semiconductor substrate which comprises a second semiconductor device thereon and a plurality of second through-electrodes configured to penetrate the second semiconductor substrate; and

a second upper semiconductor chip stacked on the first upper semiconductor chip and electrically connected to the plurality of second through-electrodes, the second upper semiconductor chip comprising a third semiconductor substrate which comprises a third semiconductor device thereon,

wherein each of side surfaces of the first upper semiconductor chip and each side surfaces of the second upper semiconductor chip are aligned with each of side surfaces of the protrusions of the lower semiconductor chip in a vertical direction,

wherein the second semiconductor device and the third semiconductor device are of an identical type and are different from the first semiconductor device,

wherein the lower semiconductor chip further comprises a first cover insulating layer configured to cover a top surface of the protrusions and configured not to cover the side

surfaces of the protrusions and lower surfaces of the recess regions, and the first upper semiconductor chip further comprises a second cover insulating layer configured to cover an active surface of the second semiconductor substrate, and

wherein the first cover insulating layer and the second cover insulating layer are bonded together with a covalent bond.

19. The semiconductor package of claim 18, wherein a plurality of bonded pads are across the first cover insulating layer and the second cover insulating layer, and electrically connect a space between the first upper semiconductor chip and the plurality of first through-electrodes.

20. The semiconductor package of claim 19, further comprising a molding member configured to cover an upper surface of the lower semiconductor chip, each of the side surfaces of the first upper semiconductor chip, each of the side surfaces of the second upper semiconductor chip, and each of the side surfaces of the protrusions, wherein a bottom surface of the molding member and bottom surfaces of the plurality of bonded pads are at an identical level.