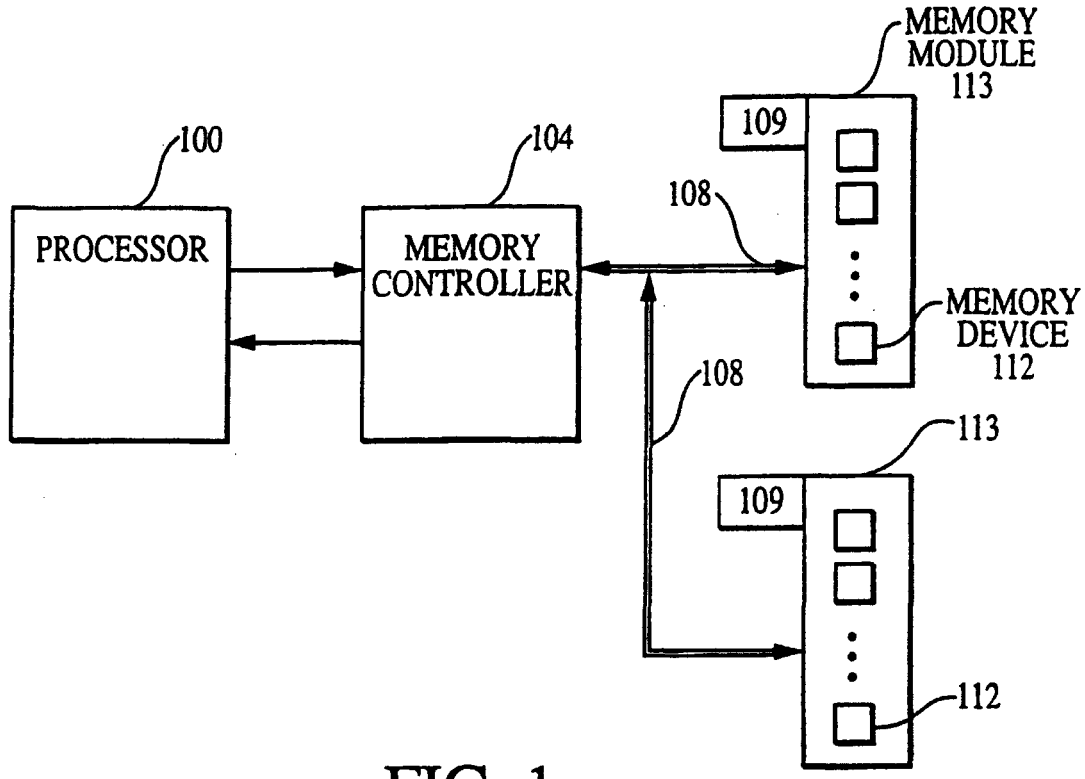

MEMORY
MODULE
113
109
100
104
108
PROCESSOR
MEMORY
CONTROLLER
MEMORY
DEVICE
112
108
113
109
112

FIG. 1

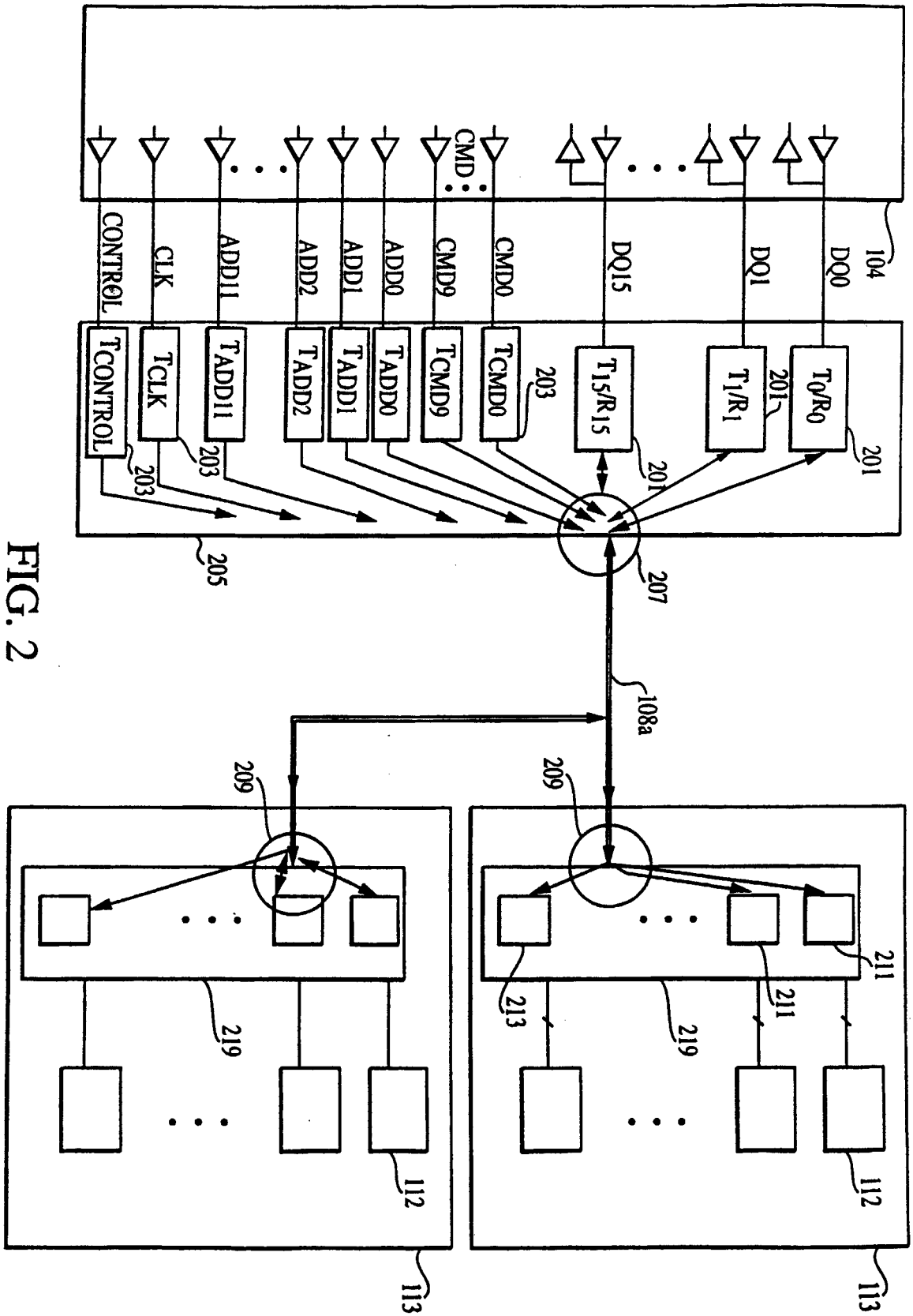

CONTROL
CLK
ADD11
ADD2
ADD1
ADD0
CMD9
CMD0
DQ15
DQ1
DQ0
104
TCONTROL
TCLK
TADD11
TADD2
TADD1
TADD0
TCMD9
TCMD0
T15/R15
T1/R1
T0/R0
203
201
205
207
108a
209
211
213
219
112
113

FIG. 2

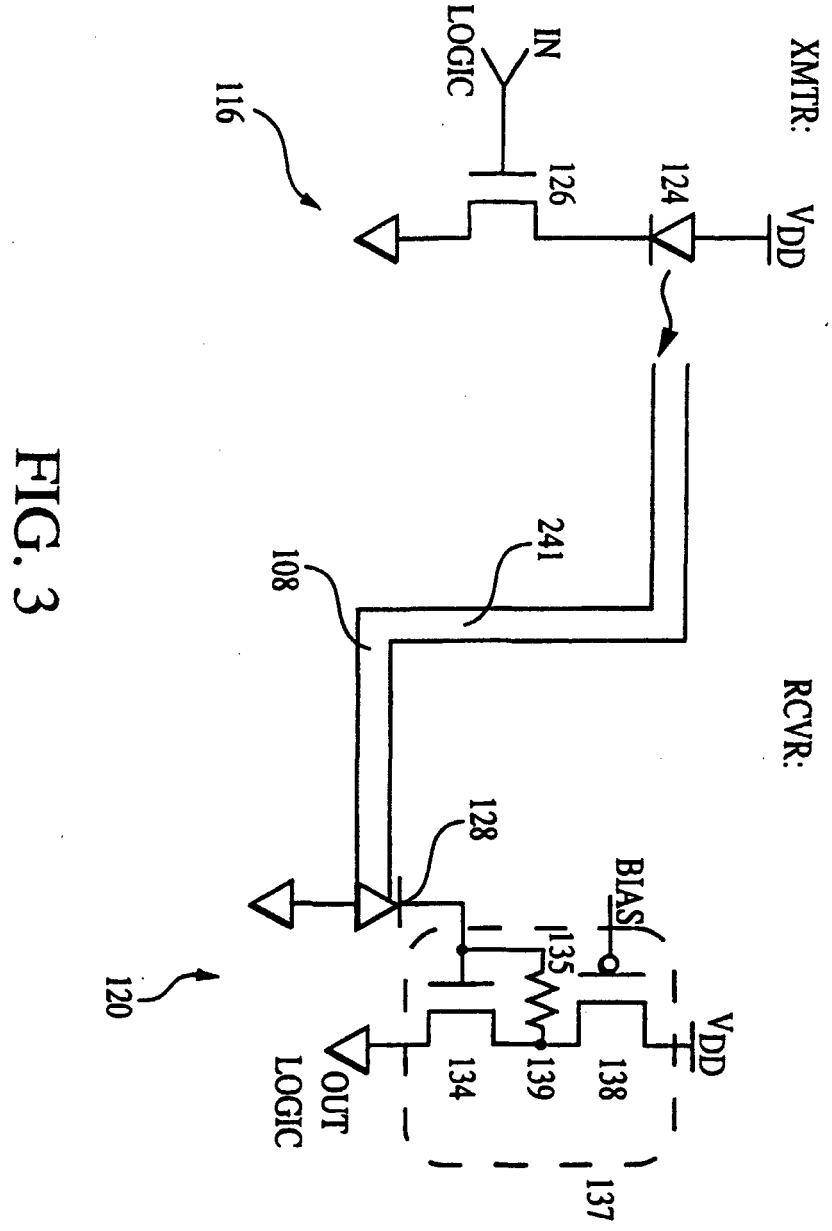

XMTR:
RCVR:
LOGIC
IN
116
126
124
V_{DD}
241
108
128
BIAS
135
120
V_{DD}
V_{OUT}
LOGIC
134
139
138
137

FIG. 3

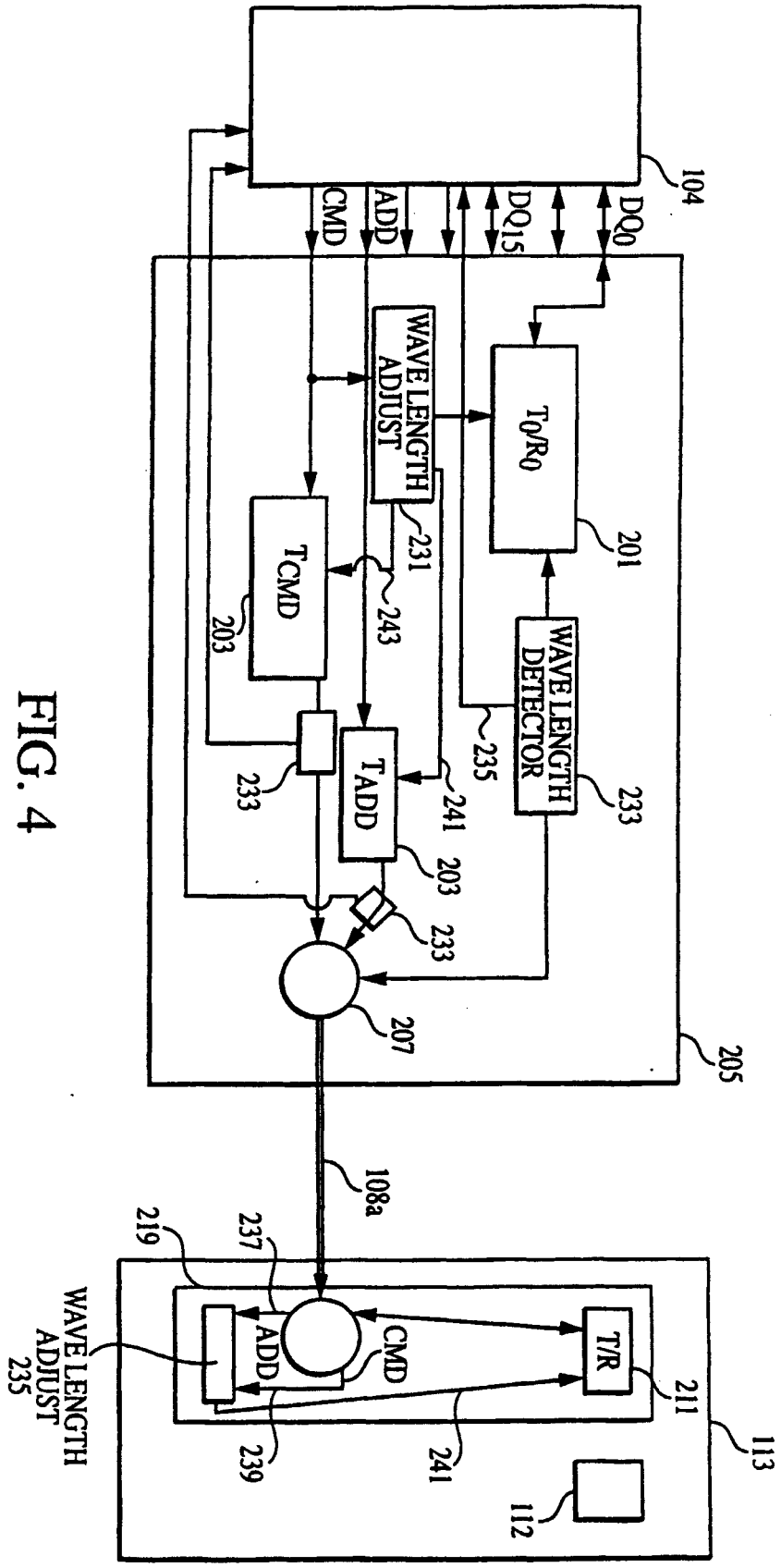

104
CMD
ADD
DQ15
DQ0
WAVE LENGTH ADJUST
T0/R0
201
231
TCMD
203
243
WAVE LENGTH DETECTOR
233
235
233
TADD
241
203
233
207
205
108a
219
237
WAVE LENGTH ADJUST 235
ADD
CMD
T/R
211
113
239
241
112

FIG. 4

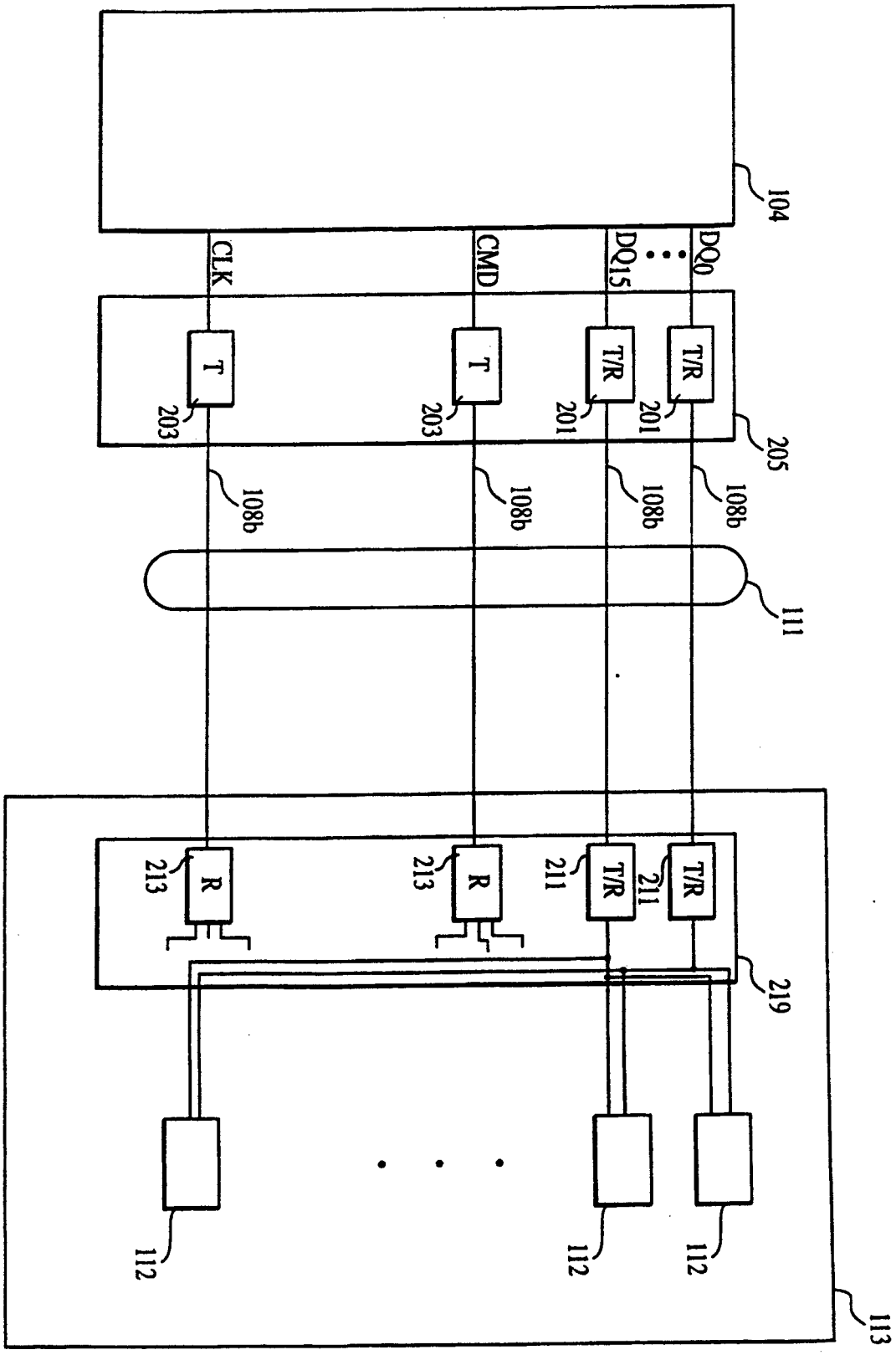

104
CLK
CMD
DQ15
DQ0
T
T
T/R
T/R
203
203
201
201
205
108b
108b
108b
108b
111
213
213
211
211
R
R
T/R
T/R
219
112
112
112
113

FIG. 5

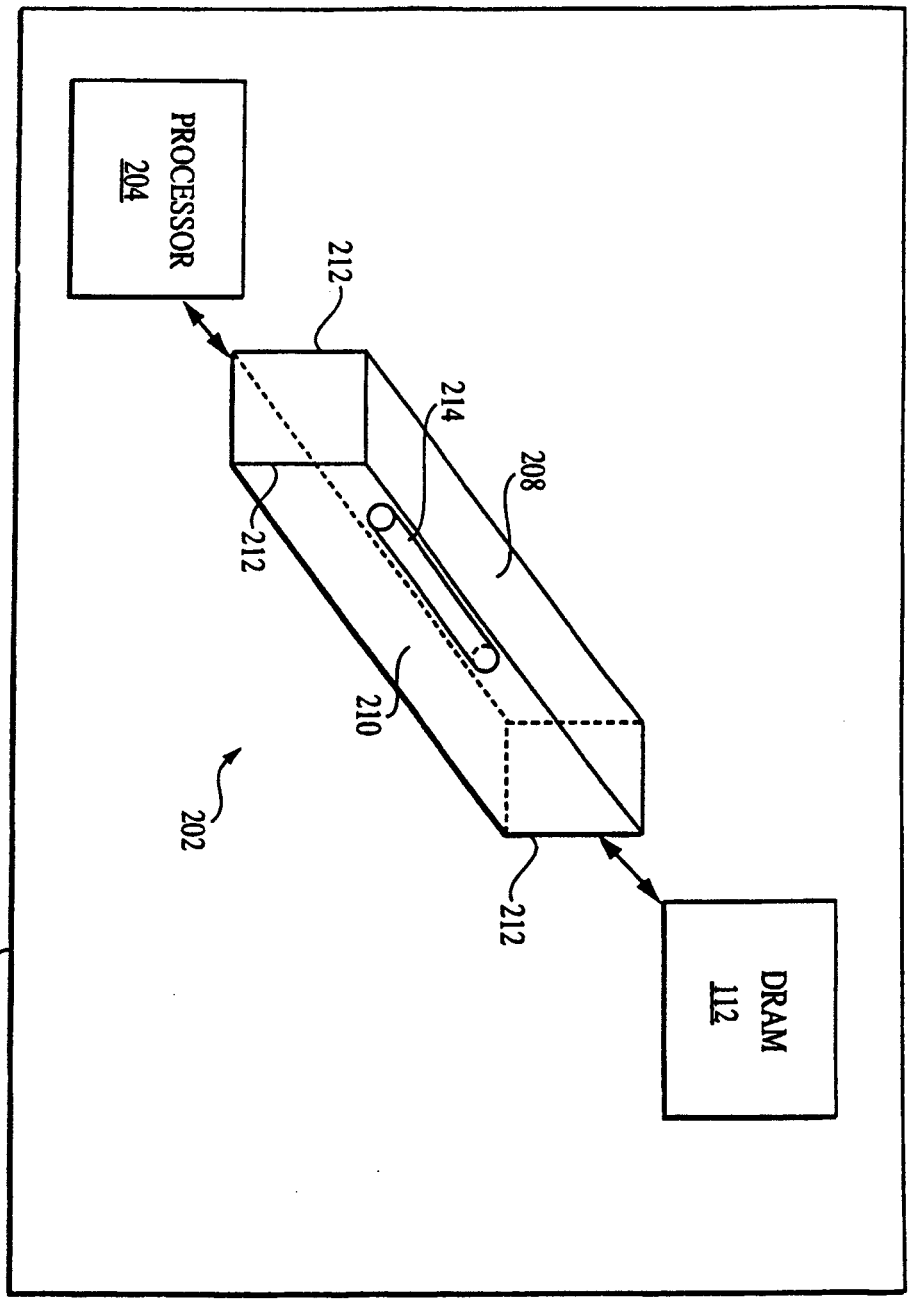


FIG. 6

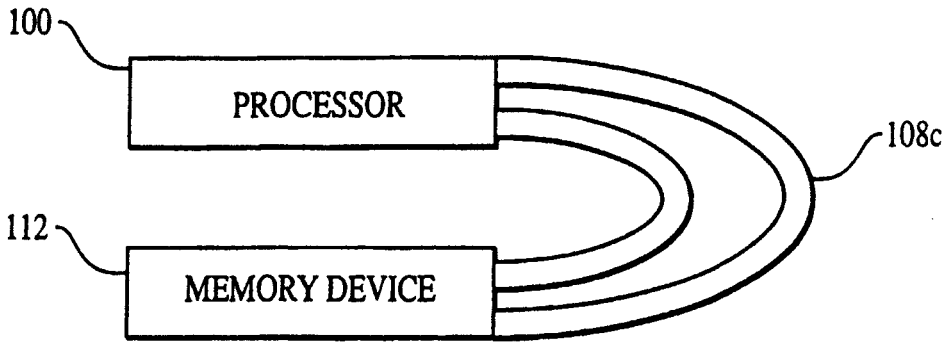


FIG. 7