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(54) Title: MECHANISM THAT PERFORMS INTERRUPT DESTINATION REDIRECTION

(57) Abstract

One embodiment of the invention includes an apparatus (10), such as a bridge, for use in connection with computer system. The apparatus includes remote priority capture logic (32) to hold task priority data indicative of a task priority of each processor P0 in the computer system that is available for lowest priority interrupt destination arbitration (LPIDA). The apparatus also includes lowest priority logic (42) to perform the LPIDA to select processor in the computer system is to receive an interrupt message based on contents of the remote priority capture logic (32). Another embodiment of the invention includes a multi-processor system having processors and a processor bus (18) coupled to the processors (P0, P1, P2, P3). The system includes remote priority capture logic (32) to hold task priority data indicative of a task priority of the processors while they are available for lowest priority interrupt destination arbitration (LPIDA). The system also includes lowest priority logic (42) to perform the LPIDA to select processors (P0, P1, P2, P3) is to receive an interrupt message based on contents of the remote priority capture logic (32), the interrupt message being provided to the processor through the processor bus (18).

