

ABSTRACT

A storage device includes nonvolatile memory chips including a first nonvolatile memory chip and a second nonvolatile memory chip and a storage controller. The first nonvolatile memory chip includes a first chip enable interface circuit and a first chip interface pin connected to the first chip enable interface circuit performs a first DMA operation, internally generates a self termination signal indicating that the first DMA operation is completed and transfers the self termination signal to the second nonvolatile memory chip through the first chip interface pin. The second nonvolatile memory chip includes a second chip interface pin and a second chip enable interface circuit connected to the second chip interface pin, is self-enabled based on the self termination signal and performs a second DMA operation without a selection chip enable command from the storage controller.

FIG. 4