

A Pulse Width Modulation Power Converter

This invention concerns electrical power conversion using pulse width modulation (PWM).

5

Switch mode power converters are frequently implemented by means of a normal H-bridge. This can either be controlled by a class AD or class BD modulator, e.g. as described in Journal of the Audio Engineering Society, 10 Jul/Aug. 1997, pp. 554-570. Class AD is characterised by simple implementation and as an advantage it has a common mode free output. But on the other hand it has some disadvantages:

- 15 • 1st harmonic of the carrier and intermodulation components are present.
- At higher powers the current in the single switching device become too high and the H-bridge implementation is no longer attractive.

20 Class BD solves the problem with the 1st harmonic of the carrier and the intermodulation products since the high frequency components are only present above the 2nd harmonic. On the other hand a common mode signal is now present at the output. The power handling capabilities 25 for class BD has the same limitations as class AD since this also uses an H-bridge.

It is also known to convert power by means of PWM, and improvements known as multi-level PWM are known in the 30 literature, such as G. Carrara, S. Gardella, M. Marchesoni, R. Salutari & G. Sciutto, 'A New Multilevel PWM Method - a Theoretical Analysis', IEEE Transactions of Power Electronics, Vol 7, No. 3 (July 1992). The basis is generally a switching power stage with multiple power 35 supply voltage levels and frequently complex control circuitry. However, each switch still has to be able to handle the full load current, and furthermore the general drawback of such methods is the severe distortion

CONFIRMATION COPY

introduced by diodes in the signal path. This is detrimental for e.g. electric motor drives because the distortion causes audible magnetostriction noise and a residual DC component may provoke saturation. In audio
5 amplifiers distortion is obviously not tolerated. There is hence a need for a different approach, which avoids the above disadvantages. More particularly, it is the purpose of the present invention to:

- Reduce the high frequency content for the differential
10 output,
- Obtain a common mode free output,
- Reduce the current in the single switching device.

This is obtained in the method according to the invention
15 which is particular in that $N/2$ PWM generators are connected in parallel at each side of a load, using a total of N PWM generators. The modulation of each PWM generator is obtained by $N/2$ phase-shifted versions of the carrier. The $N/2$ carriers are equally distributed
20 over 180° or 360° .

The conversion is performed in a scalable structure of two or more half bridges each controlled by individually generated PWM signals. The PWM signals are generated from
25 a comparison between a reference signal, which might either be analog or digital and the inverted reference signal with several phase-shifted versions of a carrier. The generated signals corresponding to the reference signal are used at one side of the load and the PWM
30 signals corresponding to the inverted reference signal are used on the other side of load. The outputs from the half bridges are summed together for each side of the load.

35 Several advantages can be obtained by intelligently controlling the phase shift between the carriers. The invention can be used in many applications, such as audio amplifiers, motor control, DC-DC converters, etc.

The invention will be designated Balanced Phase Shifted Carriers Pulse Width Modulation (BPSCPWM).

5 The mathematical expressions for the phase shift between the carriers are given by:

1) $\theta_p = \frac{2\pi}{N}$, According to claim 2.

2) $\theta_p = \frac{4\pi}{N}$, According to claim 3.

10 The $N/2$ PWM signals are created by a comparison between the carriers and the reference signal. These are summed together on one side of the load. On the other side of the load the carriers are compared with the inverted reference signal and summed together.

15 The advantage of using $N/2$ carriers and N half bridges are:

- The current in the load is evenly divided between the half bridges of one side of the load. This will lead to a reduced stress of the single switching device.
- The high frequency content will be reduced for both
20 choices of the phase shift, θ_p .
- For $\theta_p = \frac{2\pi}{N}$ the high frequency content for differential mode will start around $N \cdot f_s$, with corresponding intermodulation products. f_s is the carrier frequency. The common mode high frequency content will start
25 around the 1st harmonic of the carrier frequency.
- For $\theta_p = \frac{4\pi}{N}$ the high frequency content for differential mode will start around $N \cdot f_s$ for $N/2$ odd, and around

$$\frac{N \cdot f_s}{2}$$
for $N/2$ even. For $N/2$ odd the common mode
spectrum will start around $\frac{N \cdot f_s}{2}$, and for $N/2$ even
30 there will be no common mode in the output.

A possible implementation of the invention is explained in the following. N PWM signals are created as described above. Comparators carry out the comparison between the carriers and the reference signal. Simple half bridges
5 make the amplification of the PWM signals from the comparators. The summing of the amplified versions of the PWM signals are carried out by means of inductors, such that each PWM generator is connected to the output via an inductor. The inductors do offer a filtering but further
10 filtering is possible and advisable.

In the case where N equals 4 and $\theta_p = \pi$ an especially easily implemented version is obtained by using comparators with inverted and non-inverted outputs. It is
15 in this case possible to use only one carrier and two comparators. The outputs from the comparators should in this case not be connected as explained in the general description, but rather an inverted and non-inverted output is used on both sides of the load, and the two
20 outputs should be taken from each comparator.

For the case where N/2 is an even number and $\theta_p = \frac{4\pi}{N}$ an especially simplified implementation for the summing inductors exists. Two inductors coming from each side of
25 the load share one inductor core. The PWM signal from one side shares the inductor core with the inverted version of the PWM signal from the other side of the load.

In an implementation of a BPSCPWM system the decision of
30 how many half bridges to use and the decision of which θ_p to use, depends on the actual requirements. Several factors might affect the decision:

- The desired high frequency content in the common mode
35 spectrum. The high frequency content will be reduced with increasing N,

- The high frequency content in the differential mode spectrum. The high frequency content will be reduced with increasing N,
- The current in the switching devices. The current in the single switching device will be reduced with increasing N,
- The complexity of the modulator increases with N.

As the carrier both single-sided and double-sided signals are possible or a combination of the two kinds. The invention requires that the carriers are DC free for optimum performance, and therefore it is advisable to make high pass filtering of the carriers before the comparators.

The PWM signals can be generated digitally in e.g. a DSP.

A control system can be implemented to improve system linearity. Using global feedback could do it. Also local feedback can be implemented around each half bridge. The two proposed control systems can be combined. The local feedback topology is an obvious possibility for a system utilising digital input, since normal global feedback requires an A/D converter in the feedback path.

The principle of the invention is independent of the utilisation of the PWM signal and is independent of the construction of the power amplifier stage or stages.

30 Brief description of the figures

The invention will be described in the following with reference to the figures:

- Fig. 1 shows the general modulator structure for the invention.
- Fig. 2 shows the general modulator structure together with a possible realisation of the power stage.

- Fig. 3 shows a particular embodiment of the modulator in the case where $N/2$ is even and $\theta_p = \frac{4\pi}{N}$ with a simplified power stage.
- Fig. 4 shows a particular embodiment of the modulator in the case where $N=4$ and $\theta_p = \pi$ with a simplified power stage.
- Fig. 5 shows possible carrier signals that are useful in the invention.
- Fig. 6 shows an example of a control system with both global feedback and feedback before the filtering, applied to a system with analog input.
- Fig. 7 shows a system with local feedback for each half bridge.
- Figs. 8 - 11 show the time domain characteristics for the invention in the case of $N=4$.

Detailed description of the figures

Fig. 1 shows the general modulator structure for a balanced embodiment of the invention. Input $V_r(t)$ to the system (11) is either analog or digital. An inversion of the reference signal is performed (12). The carrier $V_{c,1}(t)$ (13) is the base for generating the other phase shifted versions of the carrier, in that these are phase shifted by the angle θ_p (14) between one carrier and the next.

The reference signal is compared (15) with the generated carriers, and $N/2$ PWM signals are generated, which are summed (16) together. The inverted version of the reference signal is also compared with carriers and the generated $N/2$ PWM signals are also summed together. The load (17) is placed between the two sums of PWM signals.

Fig. 2 shows a possible general realisation of the balanced solution. The reference signal (21) and the carriers (22) are compared (23) producing PWM signals as described above. The generated PWM signals control half

bridges (24), which cause an amplification of the PWM signals, because the high state voltage of the PWM signal now equals the supply voltage V_{cc} . The summing of the PWM signals are performed by means of inductors (25). The inductors also filter the resulting summed PWM signal, but further filtering might be necessary. Adding a capacitor (26) in parallel with the load (27) easily does this. This implements an effective 2nd order filtering of the output signal. In case that more filtering is needed an additional differential- or common mode filter could be applied.

Fig. 3 shows an alternative method for $N/2$ even and

$\theta_p = \frac{4\pi}{N}$. As shown only $N/4$ carrier are required in this

case. The method requires $N/2$ comparators with two outputs, non-inverted and inverted. The non-inverted PWM signals generated from the reference signal (31) together with the inverted PWM signals generated from the inverted reference signal (32) are used on the one side of the load, while the remaining are used on the other side of the load. The summing inductors corresponding to the amplified PWM signals coming from the same comparator shares the same inductor core (33), since the PWM signals are inverted versions.

Fig. 4 shows an embodiment of the system described above. For this case $N=4$ and $\theta_p = \pi$. As shown only two comparators and one carrier are needed. Furthermore only two inductor cores for the four inductors L are used.

Fig. 5 shows examples of three different kinds of carrier signals that might be used in the invention. The two first kinds are sawtooth while the bottom one is a triangular wave. Generally any periodical signal is suitable for the carrier. But it should be emphasised that pleasant high frequency characteristics for the

differential mode and common-mode only are obtained for the double-sided carrier.

Fig. 6 shows a general control for the system. The figure
5 shows the possibility for feedback from the output (61) and feedback before the output (62), which will be a feedback of the PWM signals.

Fig. 7 shows a local control system for the individual
10 half bridge. This can be combined with the control system from Fig. 6. The non-amplified PWM signal (71) is used as a reference for a comparison with the feedback from the amplified version of the PWM signal (72). This will produce an error signal (73), which is used for the
15 correction.

Figs. 8 - 11 show the resulting time domain characteristics for the invention for the case for $N=4$. In all four Figs. The top graph shows the modulating
20 signal and the interleaved carriers, the centre graph shows the resulting differential output signal, and the bottom graph shows the resulting common-mode output. Fig. 8 and Fig. 10 show single-side modulated waveforms, and Fig. 9 and Fig. 11 show double-side modulated waveforms.
25 The latter also shows that where the two carriers are distributed equally over 360° and the carriers are double-sided, there is no common-mode signal in the output.

**PATENT CLAIMS**

1. A method for electrical power conversion using pulse width modulation (PWM) characterized in that N/2 paralleled PWM generators on each side of a load
5 in which the modulation of the N/2 PWM signals is produced by N/2 phase-shifted versions of the carrier (12) compared with the reference signal (11) on one side of the load and the inverted reference signal on the opposite side of the load.

10

2. A system according to claim 1 characterized in that the phase shifts (θ_p) between the carriers are distributed uniformly over 180°,

$$\theta_p = \frac{2\pi}{N}.$$

15

3. A system according to claim 1 characterized in that the phase shifts (θ_p) between the carriers are distributed uniformly over 360°,

$$\theta_p = \frac{4\pi}{N}.$$

20

4. A system according to claim 1-3 characterized in that it comprises:

- An input terminal (21) for either analog or digital input,
- 25 - N modulators (23) controlled by N/2 phase shifted carriers and the reference signal and its inverted version for generation of N pulse width modulated signals,
- N half bridges each driven by a pulse width modulated
30 signal (24),
- N inductors with equal inductance for summing and demodulation (25),
- Filtering before the output (26) with capacitors in differential (26) or common mode configuration.

35

This Sheet Has Been Replaced



5. A system according to claim 1-5 where $\theta_p = \frac{4\pi}{N}$ characterised in that inductors from each side of the load share the same inductor core (33), such that the PWM signals that share the core are inverted versions.
6. A system according to claim 5 for $N=4$ and $\theta_p = \pi$ characterised in that only one carrier (41) is used and that modulation is effected by two comparators (42) with non-inverting (43) and inverting outputs (44) such that each of said outputs are used on each side of the load and in that a non-inverted output and inverted output is used for either side of the load.
7. A method according to claim 1-5 characterised in that each carrier is a sawtooth, a triangular wave or a combination of a sawtooth and a triangular wave.
8. A system according to claim 1-5 with a digital reference signal characterised in that each carrier is digitally generated and the modulation is performed by digital comparators.
9. A system according to claim 4 and 5 with an analog reference signal characterised in that a feedback control system is applied.
10. A system according to claim 4 and 5 characterised in that a control system is applied to each half bridge.

This Sheet Has Been Replaced

