Claims

What is claimed:

1. A semiconductor device, comprising:

a wafer level substrate including a semiconductor material; a plurality of first conductive vias formed through the wafer level substrate;

a first semiconductor die ~~mounted to~~ disposed over the wafer level substrate, the first semiconductor die including ~~a first surface with~~ contact pads ~~oriented toward~~ disposed over a first surface of the wafer level substrate;

a first encapsulant deposited over the first semiconductor die and wafer level substrate;

a second semiconductor die ~~mounted to~~ disposed over the wafer level substrate, the second semiconductor die including ~~a first surface with~~ contact pads ~~oriented toward~~ disposed over a second surface of the wafer level substrate opposite the first surface; ~~of the wafer level substrate;~~

~~a second encapsulant deposited over the second semiconductor die; and~~

a plurality of first bumps formed over the ~~plurality of first conductive vias,~~ wafer level substrate outside a footprint of the second semiconductor die; and

a second encapsulant deposited over the second semiconductor die and over the plurality of first bumps while the plurality of first bumps remains partially exposed from the second encapsulant.

2. The semiconductor device of claim 1, further including:

a first insulating layer formed with openings over the first surface of the wafer level substrate;

a first conductive layer formed in the openings in the first insulating layer and over the first surface of the wafer level substrate;

a second insulating layer formed with openings over the second surface of the wafer level substrate; and

a second conductive layer formed in the openings in the second insulating layer and over the second surface of the wafer level substrate.

3. The semiconductor device of claim 1, further including a plurality of second conductive vias formed through the first encapsulant and electrically connected to the plurality of first conductive vias.

4. The semiconductor device of claim 1, wherein the plurality of first bumps is formed over the second surface of the wafer level substrate.

5. The semiconductor device of claim 1, ~~wherein the first encapsulant is deposited around the plurality of bumps~~ further including a plurality of second bumps formed over the first surface of the wafer level substrate.

6. The semiconductor device of claim 1, wherein a plurality of semiconductor devices is stacked and each contains the first and second semiconductor die ~~mounted to~~ disposed over the first and second surfaces of the wafer level substrate.

7. The semiconductor device of claim 1, wherein the wafer level substrate ~~has~~includes a coefficient of thermal expansion (CTE) that matches a CTE of a base material of the first and second semiconductor die.

8. A semiconductor device, comprising:

a ~~wafer level~~ semiconductor substrate including a first conductive via formed through the ~~wafer level~~ semiconductor substrate;

a first semiconductor die ~~mounted to the wafer level substrate, the first semiconductor die~~ including ~~a first surface~~

~~with~~ contact pads ~~oriented toward~~ disposed over a first surface of the ~~wafer level~~ semiconductor substrate;

a first encapsulant deposited over the first semiconductor die and ~~wafer level~~ side surfaces of the semiconductor substrate;

a second semiconductor die ~~mounted to the wafer level substrate, the second semiconductor die~~ including ~~a first surface with~~ contact pads ~~oriented toward~~disposed over a second surface of the ~~wafer level~~ semiconductor substrate opposite the first surface ~~of the wafer level substrate~~; ~~and~~

a second encapsulant deposited over the second semiconductor die; and

a second conductive via formed through the first encapsulant and electrically connected to the first conductive via.

9. The semiconductor device of claim 8, further including a bump formed ~~over the first conductive via and~~ over ~~the second surface of~~ the ~~wafer level~~ semiconductor substrate.

~~10. The semiconductor device of claim 8, further including a second conductive via formed through the first encapsulant and electrically connected to the first conductive via.~~

1~~1~~0. The semiconductor device of claim 8, wherein a plurality of semiconductor devices is stacked and each contains the first and second semiconductor die ~~mounted to~~ disposed over the first and second surfaces of the ~~wafer level~~ semiconductor substrate.

1~~2~~1. The semiconductor device of claim 8, wherein the ~~wafer level~~ semiconductor substrate ~~has~~ includes a coefficient of

thermal expansion (CTE) that matches a CTE of a base material of the first and second semiconductor die.

132. A semiconductor device, comprising:

a substrate including a first conductive via formed through the substrate;

a first semiconductor die ~~mounted~~disposed over a first surface of the substrate;

a first encapsulant deposited over the first semiconductor die and substrate;

a second semiconductor die ~~mounted~~disposed over a second surface of the substrate opposite the first surface of the substrate, wherein the substrate includes a coefficient of thermal expansion (CTE) that matches a CTE of a base material of the first and second semiconductor die;

~~a second encapsulant deposited over the second semiconductor die; and~~

a first bump formed over the first surface of the ~~first conductive via~~substrate outside a footprint of the first semiconductor die; and

a second bump formed over the second surface of the substrate outside a footprint of the second semiconductor die.

143. The semiconductor device of claim 132, wherein:

the first semiconductor die is ~~mounted to~~ disposed over the substrate, the first semiconductor die including ~~a first surface with~~ contact pads oriented toward the first surface of the substrate; and

the second semiconductor die is ~~mounted to~~disposed over the substrate, the second semiconductor die including ~~a first surface with~~ contact pads oriented toward the second surface of the substrate opposite the first surface ~~of the substrate~~.

15~~3~~4. ~~The semiconductor device of claim 13~~ A semiconductor device, comprising:

a substrate including a first conductive via formed through the substrate;

a first semiconductor die mounted over a first surface of the substrate;

a first encapsulant deposited over the first semiconductor die and substrate;

~~, further including~~ a second conductive via formed through the first encapsulant and electrically connected to the first conductive via;

a second semiconductor die mounted over a second surface of the substrate opposite the first surface of the substrate;

a second encapsulant deposited over the second semiconductor die; and

a bump formed over the first conductive via.

~~16. The semiconductor device of claim 13, wherein the bump is formed over the second surface of the substrate.~~

175. ~~The semiconductor device of claim 13,~~ A semiconductor device, comprising:

a substrate including a first conductive via formed through the substrate;

a first semiconductor die mounted over a first surface of the substrate;

a first encapsulant deposited over the first semiconductor die and substrate;

a second semiconductor die mounted over a second surface of the substrate opposite the first surface of the substrate;

a second encapsulant deposited over the second semiconductor die; and

a bump formed over the first conductive via, wherein a plurality of semiconductor devices is stacked and each contains the first and second semiconductor die mounted to the first and second surfaces of the substrate.

~~18. The semiconductor device of claim 13, wherein the substrate has a coefficient of thermal expansion (CTE) that matches a CTE of the first and second semiconductor die.~~

196. A semiconductor package, comprising:

a substrate ~~having~~ including a first conductive via extending through the substrate;

a first semiconductor die ~~mounted to~~ disposed over a first surface of the substrate;

a first encapsulant deposited over the first semiconductor die and side surfaces of the substrate;

a second semiconductor die ~~mounted to~~disposed over a second surface of the substrate opposite the first surface ~~of the substrate~~, wherein the substrate includes a coefficient of

thermal expansion (CTE) that matches a CTE of a base material of the first and second semiconductor die; ~~and~~

a second encapsulant deposited over the second semiconductor die; and

a second conductive via formed through the first encapsulant and electrically connected to the first conductive via.

~~20~~17. The semiconductor ~~device~~ package of claim ~~19~~16, wherein:

the first semiconductor die is ~~mounted to~~ disposed over the substrate, the first semiconductor die including ~~a first surface with~~ contact pads oriented toward the first surface of the substrate; and

the second semiconductor die is ~~mounted to~~ disposed over the substrate, the second semiconductor die including ~~a first surface with~~ contact pads oriented toward the second surface of the substrate opposite the first surface ~~of the substrate~~.

~~21~~18. The semiconductor ~~device~~ package of claim ~~19~~16, further including a bump formed over ~~the conductive via and over the second surface of~~ the substrate.

~~22~~19. The semiconductor ~~device~~ package of claim ~~21~~18, wherein the first encapsulant is deposited around the bump.

2~~3~~0. The semiconductor ~~device~~package of claim ~~21~~18, wherein a plurality of semiconductor devices is stacked and each contains the first and second semiconductor die ~~mounted to~~disposed over the first and second surfaces of the substrate.

~~24. The semiconductor device of claim 21, wherein the substrate has a coefficient of thermal expansion (CTE) that matches a CTE of the first and second semiconductor die.~~

2~~5~~1. The semiconductor ~~device~~package of claim 1~~9~~6, further including:

a first insulating layer formed with openings over the first surface of the substrate;

a first conductive layer formed in the openings in the first insulating layer and over the first surface of the substrate;

a second insulating layer formed with openings over the second surface of the substrate; and

a second conductive layer formed in the openings in the second insulating layer and over the second surface of the substrate.

22. A semiconductor device, comprising:

a substrate including a first conductive via formed through the substrate;

a first semiconductor die disposed over a first surface of the substrate;

a first encapsulant deposited over the first semiconductor die and side surfaces of the substrate;

a second semiconductor die disposed over a second surface of the substrate opposite the first surface; and

a second conductive via formed through the first encapsulant and electrically connected to the first conductive via.

23. The semiconductor device of claim 22, further including a second encapsulant deposited over the second semiconductor die.

24. The semiconductor device of claim 22, further including a bump formed over the first conductive via outside a footprint of the second semiconductor die.

25. The semiconductor device of claim 22, wherein an active surface of the first semiconductor die is oriented toward the substrate.

26. The semiconductor device of claim 22, wherein an active surface of the second semiconductor die is oriented toward the substrate.