(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 July 2008 (03.07.2008)

PCT

(10) International Publication Number
WO 2008/078132 A1

(51) International Patent Classification:
H01L 21/322 (2006.01) *H01L 21/762* (2006.01)

(21) International Application Number:
PCT/IB2006/003957

(22) International Filing Date:
26 December 2006 (26.12.2006)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **KONONCHUK, Oleg** [US/FR]; 4 Place Bir Hakeim, F-38000 Grenoble (FR).

(74) Agents: **SCHRIMPF, Robert** et al.; Cabinet Regimbeau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

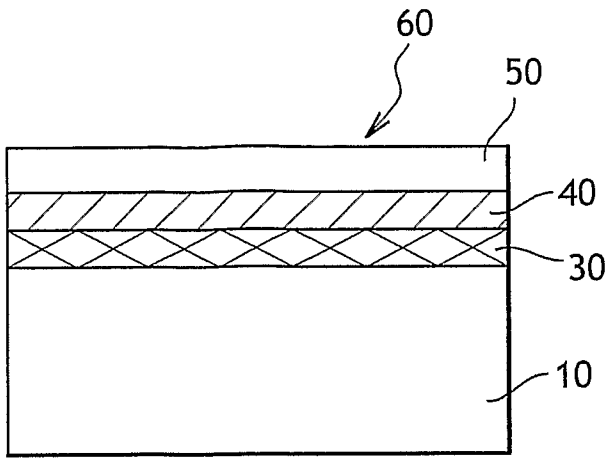
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

WO 2008/078132 A1

(54) Title: METHOD FOR PRODUCING A SEMICONDUCTOR-ON-INSULATOR STRUCTURE



(57) Abstract: The invention relates to a process of treating a structure for electronics or optoelectronics, the structure comprising successively: - a substrate, - a dielectric layer having a thermal conductivity substantially higher than the thermal conductivity of an oxide layer made of an oxide of a semiconductor material, - an oxide layer made of an oxide of the said semiconductor material, - a thin semiconductor layer made of said semiconductor material, characterized in that it comprises a heat treatment of the structure in an inert or reducing atmosphere with a temperature value and a duration chosen for inciting an amount of oxygen of the oxide layer to diffuse through the semiconductor layer so that the thickness of the oxide layer decreases by a determined value. The invention also relates to a process of manufacturing a structure for electronics or optoelectronics comprising the said heat treatment.