CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a composite structure comprising a first semiconductor crystalline material interspersed with a high aspect ratio to a second material, the composite structure to have a planar surface; and

a strained second semiconductor crystalline material over the first semiconductor crystalline material at the planar surface, wherein the surface of the first semiconductor crystalline material has a surface roughness RMS of 5nm or less, and wherein the planar surface is treated by a pre-bake process using gases consisting of hydrogen or combinations of hydrogen and inert gas to reduce impurity concentrations at an interface between the first and second semiconductor crystalline materials ~~has reduced impurity concentrations~~.

2. The device of claim 1, wherein the surface of the second semiconductor crystalline material has a surface roughness RMS of about 4nm or less, about 3nm or less, about 1nm or less, about 0.5nm or less, or no greater than 0.3nm.

3. The device of claim 1, wherein ~~the interface has reduced~~ the pre-bake process using gases consisting of hydrogen or combinations of hydrogen and inert gas reduces oxygen impurity concentrations at the interface between the first and second semiconductor crystalline materials.

4. The device of claim 1, wherein the strain is along a longitudinal direction of the opening, perpendicular to the longitudinal direction or both along and perpendicular to the longitudinal.

5. The device of claim 1, wherein the composite structure comprises:

a semiconductor crystalline substrate;

an insulator having an opening to the substrate;

the first semiconductor crystalline material within the opening in the insulator, the first semiconductor crystalline material being lattice-mismatched with the substrate.

6. The device of claim 5, wherein the substrate is configured with depressions in the substrate, and wherein the insulator overlies sides of the depression to form said opening.

7. The device of claim 1 further comprising a CMOS device integrated with the substrate.

8. The device of claim 1, wherein the crystalline material is a group III-V compound.

9. The device of claim 1, wherein the interface between the first and second semiconductor crystalline materials is heat treated by the pre-bake process using gases consisting of hydrogen ~~for a selected period of time~~ at temperatures between 760 ^{o}C to 860 ^{o}C ~~in H_2 gas~~.

10. The device of claim 1, wherein the growing the second semiconductor crystalline material is strained Ge and the first semiconductor crystalline material a SiGe alloy.

11. A method of manufacturing a semiconductor structure, comprising:

providing a semiconductor crystalline substrate;

forming an insulator defining openings to a surface of the substrate; and

growing a first semiconductor crystalline material lattice-mismatched with the substrate within the openings of the insulator;

polishing a top surface of the first semiconductor crystalline material and the insulator;

growing a second semiconductor crystalline material over the polished first semiconductor crystalline material; and

heating the polished top surface ~~at a selected temperature range~~ by a pre-bake process using gases consisting of hydrogen or combinations of hydrogen and inert gas to reduce impurities at the interface of the first and second semiconductor crystalline material.

12. The method of claim 11, wherein the heating comprises heating at temperatures between 760 ^{o}C to 860 ^{o}C.

13. The method of claim 11, wherein the surface of the second semiconductor crystalline material has a surface roughness RMS of about 5nm or less, about 3nm or less, about 1nm or less, about 0.5nm or less, or no greater than 0.3nm.

14. The method of claim 11, wherein ~~the interface has reduced~~ the pre-bake process using gases consisting of hydrogen or combinations of hydrogen and inert gas oxygen impurity concentrations at the interface between the first and second semiconductor crystalline materials.

15. The method of claim 11, wherein the second semiconductor crystalline material is elastically strained at least along a first direction relative to the opening, along a second direction perpendicular to the first direction or along both the first and second directions.

16. The method of claim 11, wherein the openings have an aspect ratio sufficient to trap defects in the crystalline material, and further comprising forming a semiconductor device at least in part in an opening.

17. The method of claim 11, wherein the heating comprises heating at a temperature ~~range~~ independent of a temperature used in the growing a second semiconductor crystalline material.

18. A method of manufacturing a semiconductor structure comprising:

epitaxially growing by CVD a first semiconductor crystalline material on a polished surface of a lattice-mismatched semiconductor crystalline material exposed within an opening of an insulator; and

cleaning the polished surface by heating the polished surface of the lattice-mismatched semiconductor crystalline material exposed within an opening of an insulator by a pre-bake process using gases consisting of hydrogen or combinations of hydrogen and inert gas to reduce an oxygen impurity concentration below a prescribed level.

19. The method of claim 18, wherein the first crystalline material is a group IV element or compound including at least one group IV element.

20. The method of one of claims 18, wherein the growing step includes growing strained Ge on a SiGe alloy.