

MEMORY DEVICE HAVING SHIELDED ACCESS LINES

ABSTRACT

An apparatus including, in one embodiment, a plurality of transistors each formed by: (1) at least a portion of one of a plurality of doped regions formed in a substrate; and (2) at least a portion of one of a plurality of first conductors each extending over one of the plurality of doped regions, the plurality of first conductors included in a first metal layer. A second metal layer includes a plurality of second conductors each interconnecting ones of the plurality of transistors. A third metal layer includes a plurality of bit lines each interconnecting ones of the plurality of transistors. A fourth metal layer includes a plurality of word lines each interconnecting ones of the plurality of transistors.

(FIG. 1)