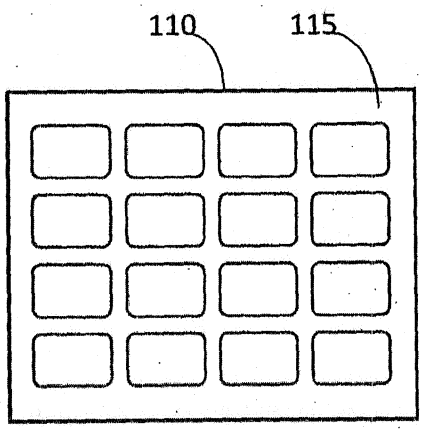

FIG. 1A
PRIOR ART

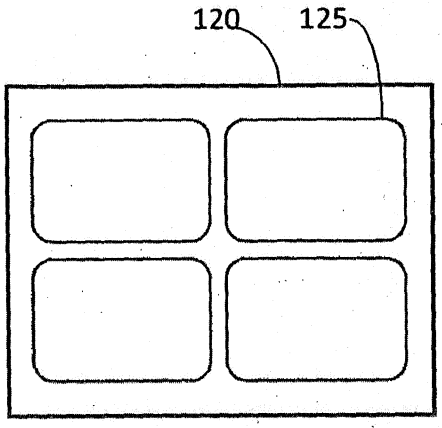

FIG. 1B
PRIOR ART

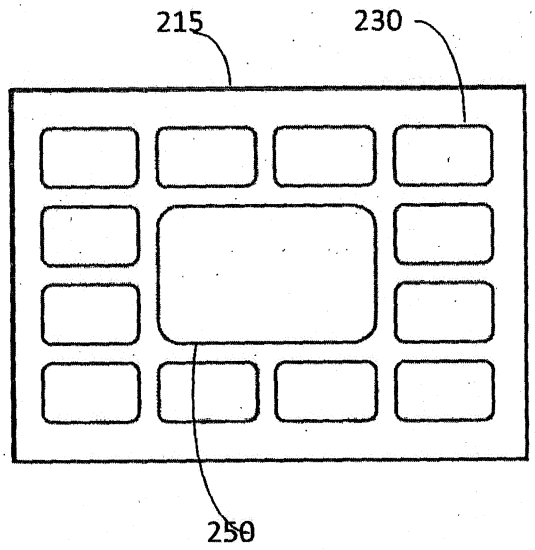

FIG. 2
PRIOR ART

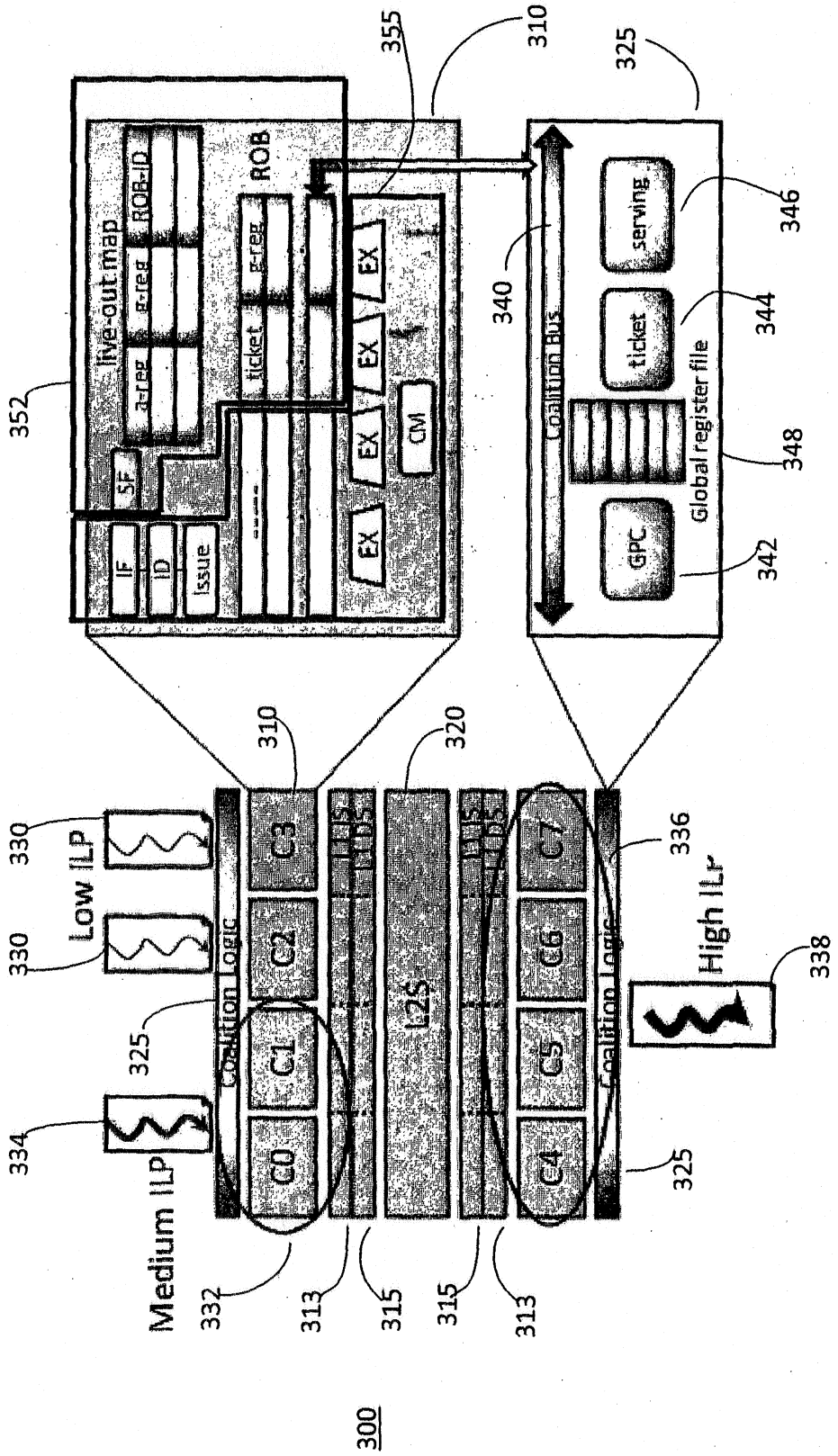
300
Medium ILP
Low ILP
High ILP
Coalition Logic
C0
C1
C2
C3
C4
C5
C6
C7
L2S
live-out map
ROB-ID
g-reg
a-reg
ROB
ticket
IF
ID
Issue
SF
EX
CM
Coalition Bus
serving
ticket
GPC
Global register file
310
320
325
330
332
334
336
338
340
342
344
346
348
352
355
313
315

FIG. 3

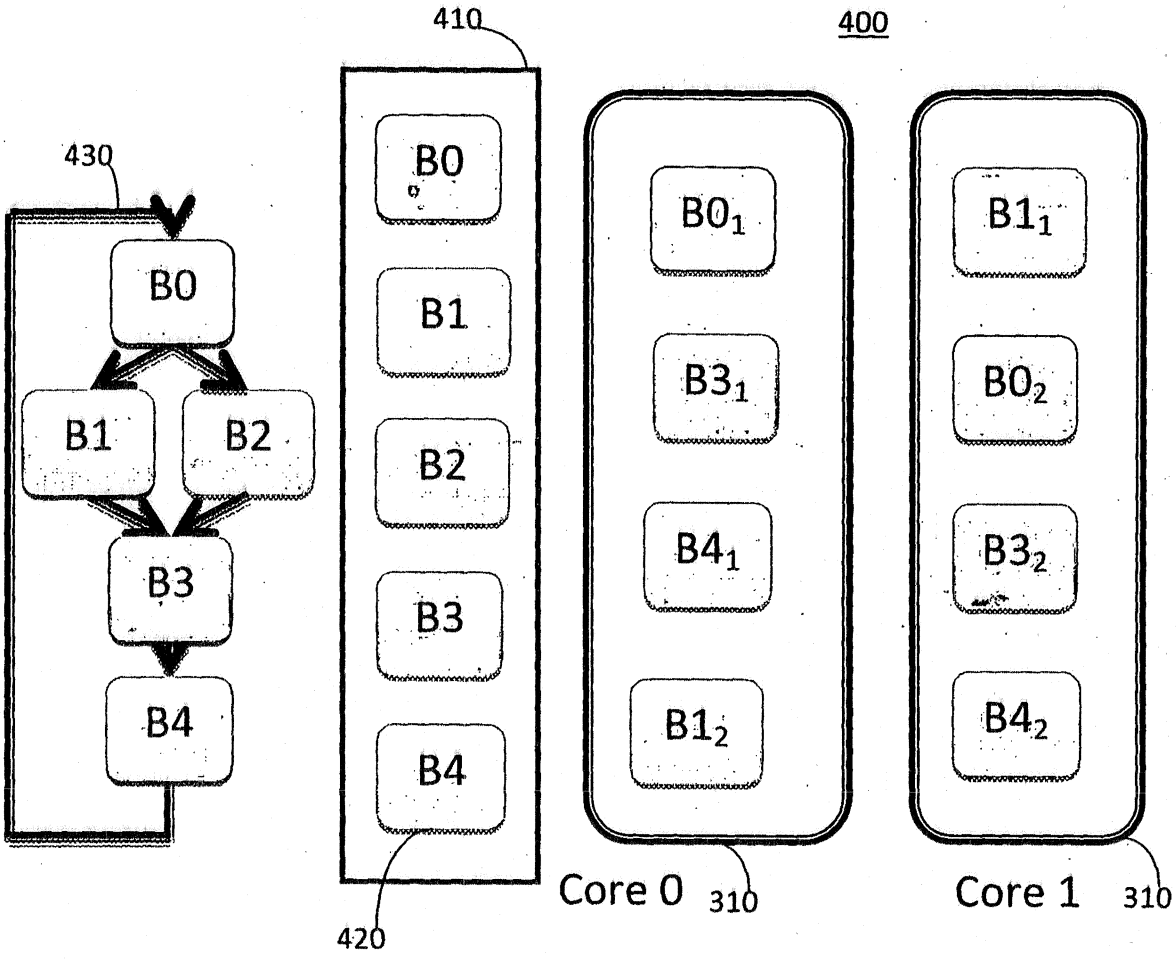

FIG. 4

500

OPCODE	BB_SIZE	BB_TYPE	LI_0	LI_1	LI_2	LO_0	LO_1	LO_2

510 520 530 540 550

FIG. 5

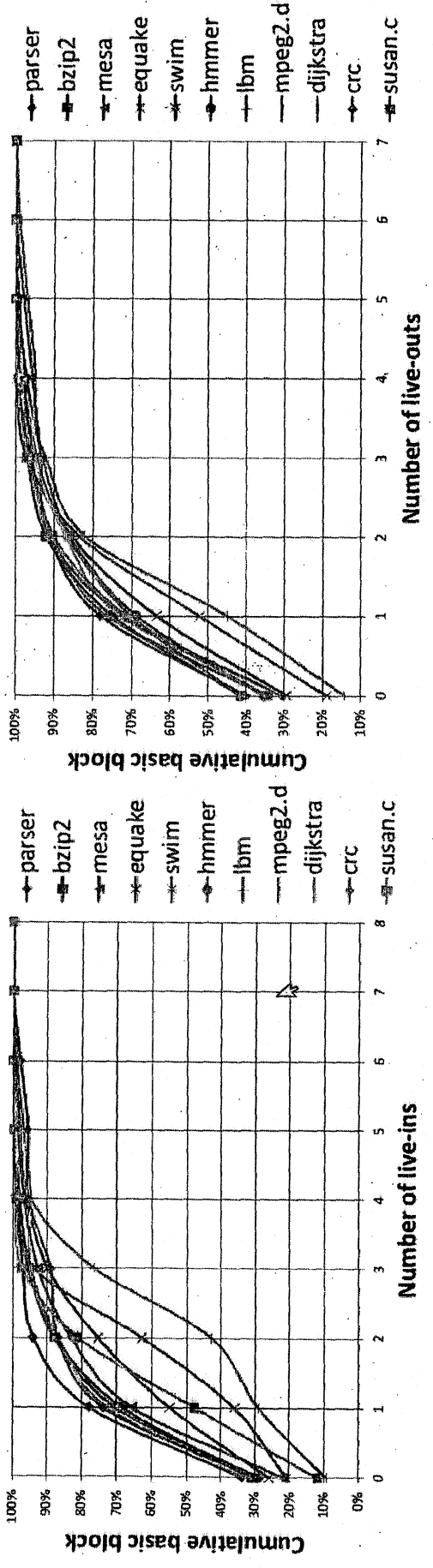
Cumulative basic block
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
0
1
2
3
4
5
6
7
8
Number of live-ins
parser
bzip2
mesa
equake
swim
hmmer
lbm
mpeg2.d
dijkstra
crc
susan.c
Cumulative basic block
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0
1
2
3
4
5
6
7
Number of live-outs
parser
bzip2
mesa
equake
swim
hmmer
lbm
mpeg2.d
dijkstra
crc.
susan.c

FIG. 6

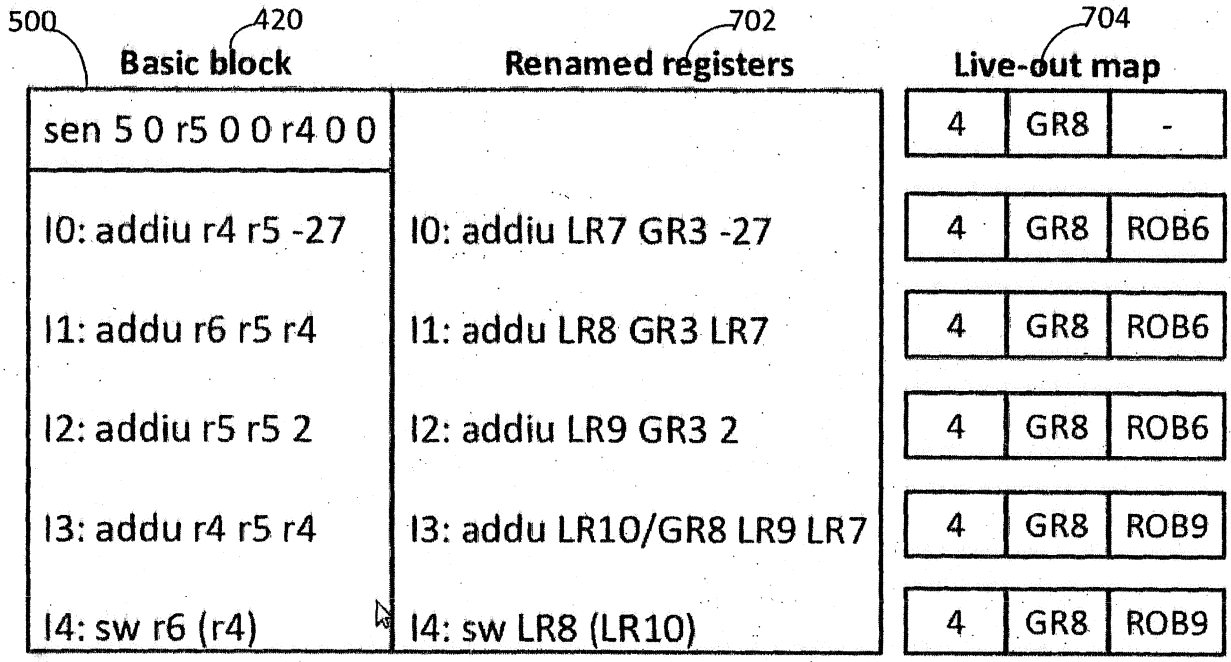
500
420
Basic block
702
Renamed registers
704
Live-out map
sen 5 0 r5 0 0 r4 0 0
4 GR8 -
I0: addiu r4 r5 -27
I0: addiu LR7 GR3 -27
4 GR8 ROB6
I1: addu r6 r5 r4
I1: addu LR8 GR3 LR7
4 GR8 ROB6
I2: addiu r5 r5 2
I2: addiu LR9 GR3 2
4 GR8 ROB6
I3: addu r4 r5 r4
I3: addu LR10/GR8 LR9 LR7
4 GR8 ROB9
I4: sw r6 (r4)
I4: sw LR8 (LR10)
4 GR8 ROB9
700

FIG. 7

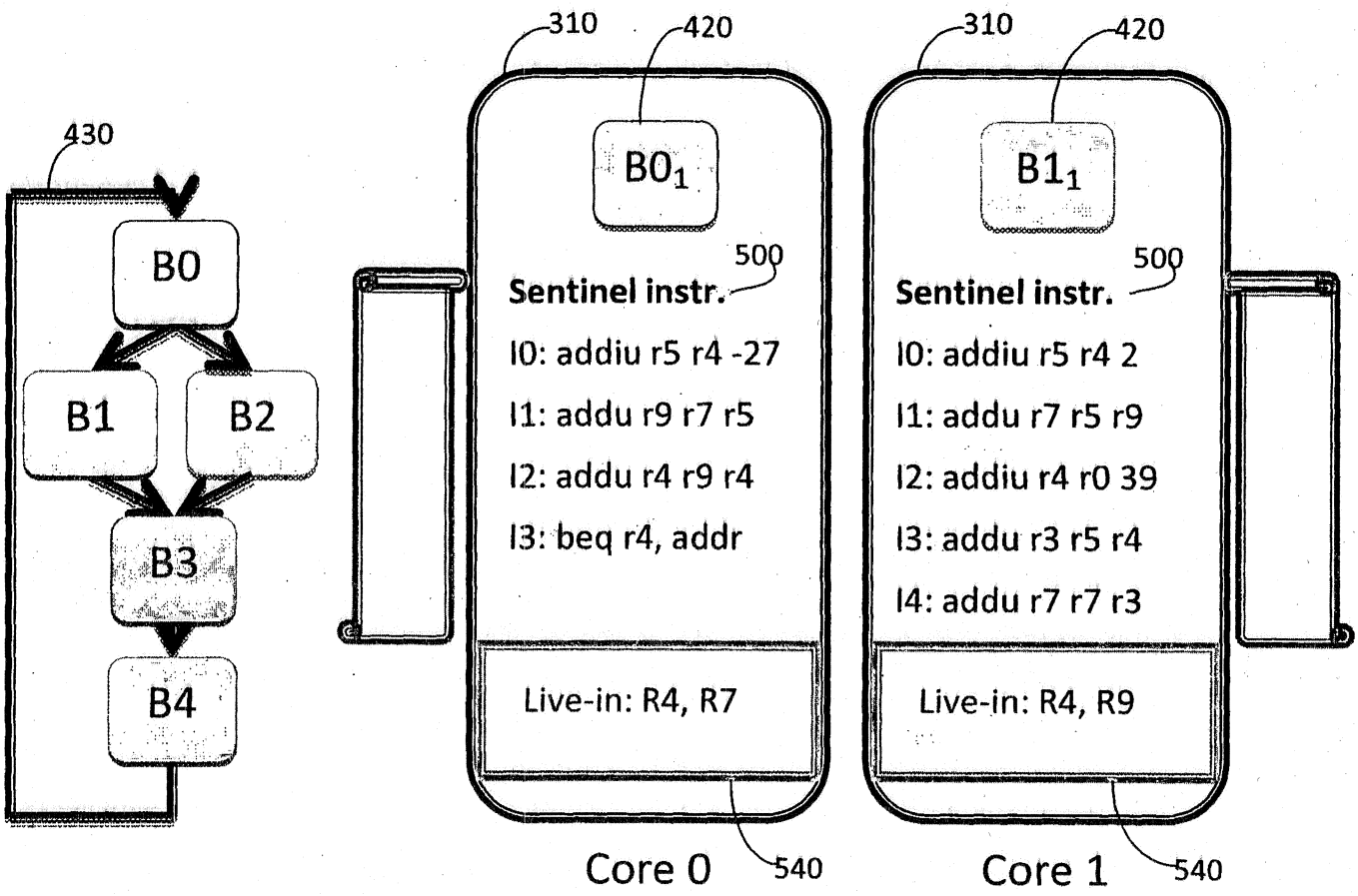
430
B0
B1
B2
B3
B4
310
420
$B0_1$
500
Sentinel instr.
I0: addiu r5 r4 -27
I1: addu r9 r7 r5
I2: addu r4 r9 r4
I3: beq r4, addr
Live-in: R4, R7
Core 0
540
310
420
$B1_1$
500
Sentinel instr.
I0: addiu r5 r4 2
I1: addu r7 r5 r9
I2: addiu r4 r0 39
I3: addu r3 r5 r4
I4: addu r7 r7 r3
Live-in: R4, R9
Core 1
540

FIG. 8

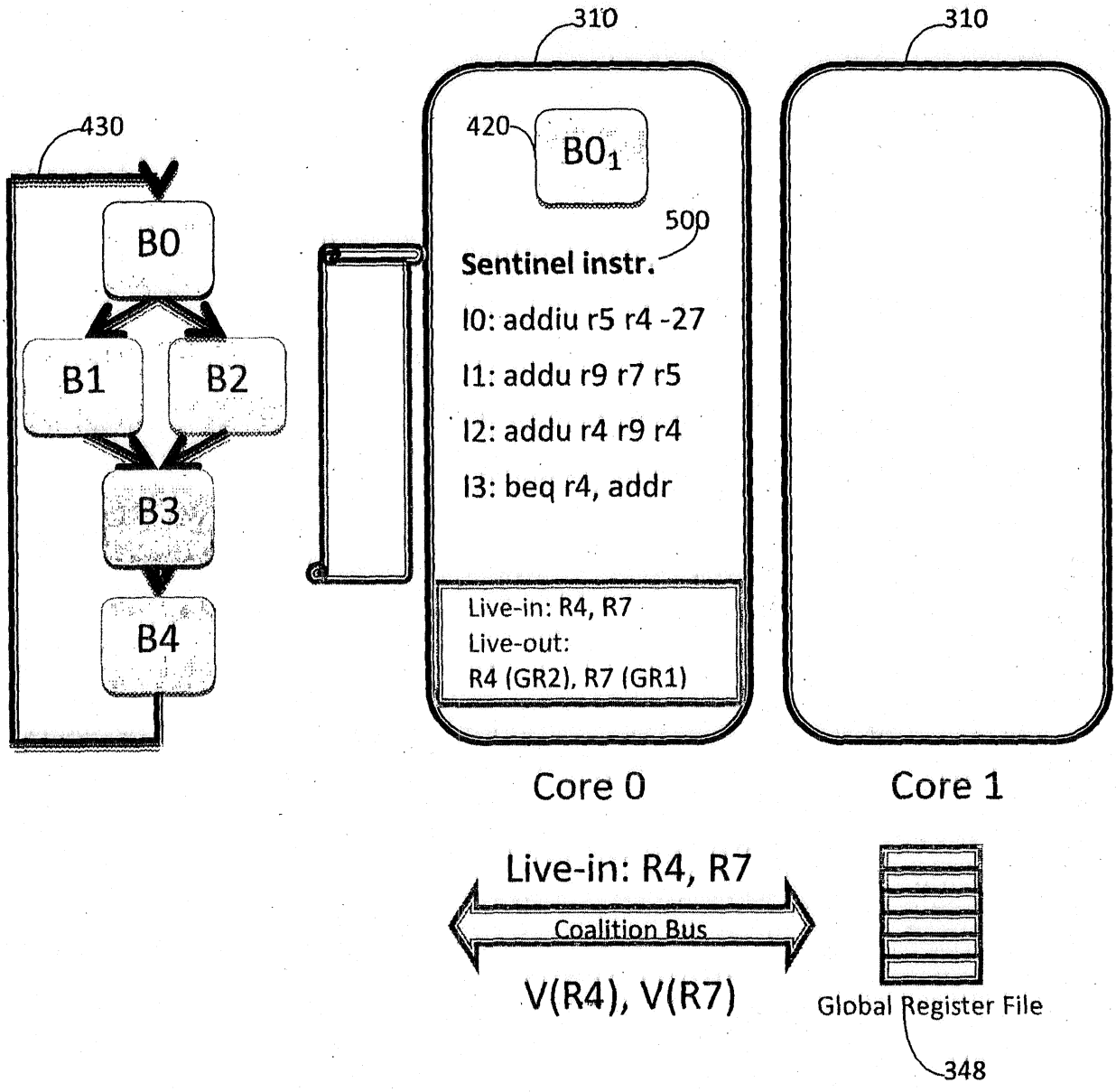
310
310
430
420
BO_1
500
Sentinel instr.
I0: addiu r5 r4 -27
I1: addu r9 r7 r5
I2: addu r4 r9 r4
I3: beq r4, addr
B0
B1
B2
B3
B4
Live-in: R4, R7
Live-out:
R4 (GR2), R7 (GR1)
Core 0
Core 1
Live-in: R4, R7
Coalition Bus
V(R4), V(R7)
Global Register File
348

FIG. 9A

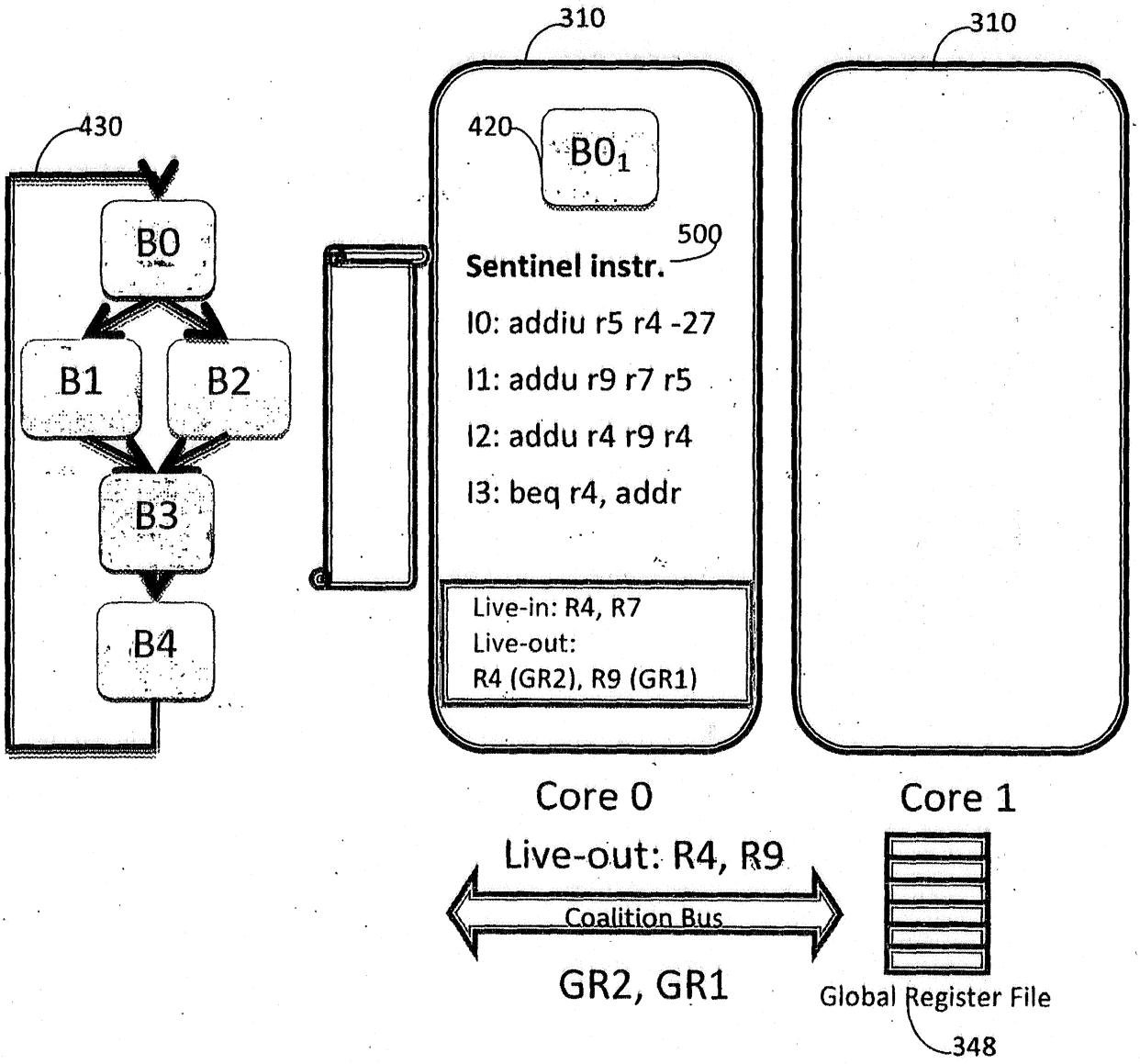
310
310
430
420
$B0_1$
B0
B1
B2
B3
B4
500
Sentinel instr.
I0: addiu r5 r4 -27
I1: addu r9 r7 r5
I2: addu r4 r9 r4
I3: beq r4, addr
Live-in: R4, R7
Live-out:
R4 (GR2), R9 (GR1)
Core 0
Core 1
Live-out: R4, R9
Coalition Bus
GR2, GR1
Global Register File
348

FIG. 9B

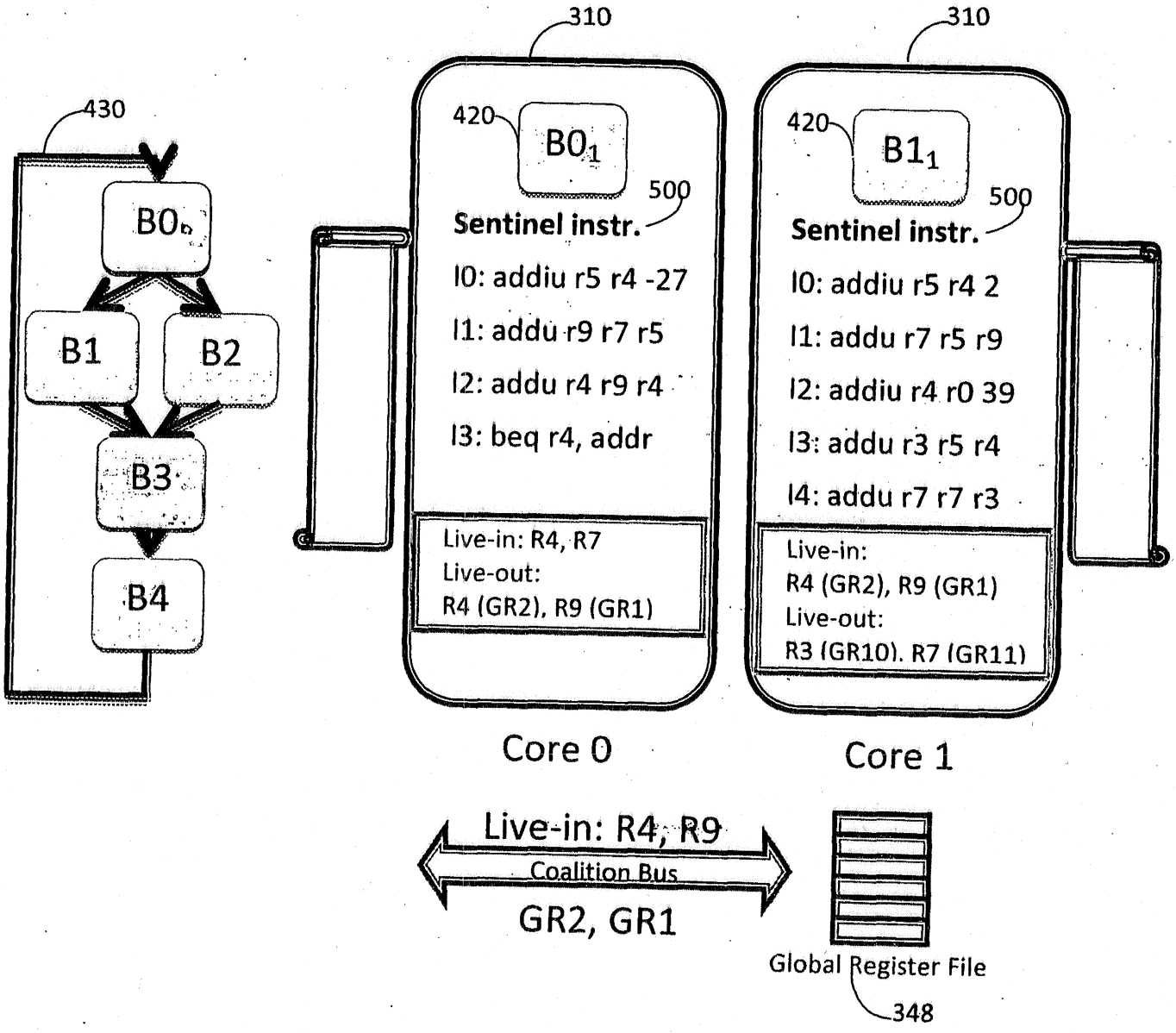
430
B0
B1
B2
B3
B4
310
420
B0 1
500
Sentinel instr.
I0: addiu r5 r4 -27
I1: addu r9 r7 r5
I2: addu r4 r9 r4
I3: beq r4, addr
Live-in: R4, R7
Live-out:
R4 (GR2), R9 (GR1)
310
420
B1 1
500
Sentinel instr.
I0: addiu r5 r4 2
I1: addu r7 r5 r9
I2: addiu r4 r0 39
I3: addu r3 r5 r4
I4: addu r7 r7 r3
Live-in:
R4 (GR2), R9 (GR1)
Live-out:
R3 (GR10), R7 (GR11)
Core 0
Core 1
Live-in: R4, R9
Coalition Bus
GR2, GR1
Global Register File
348

FIG. 9C

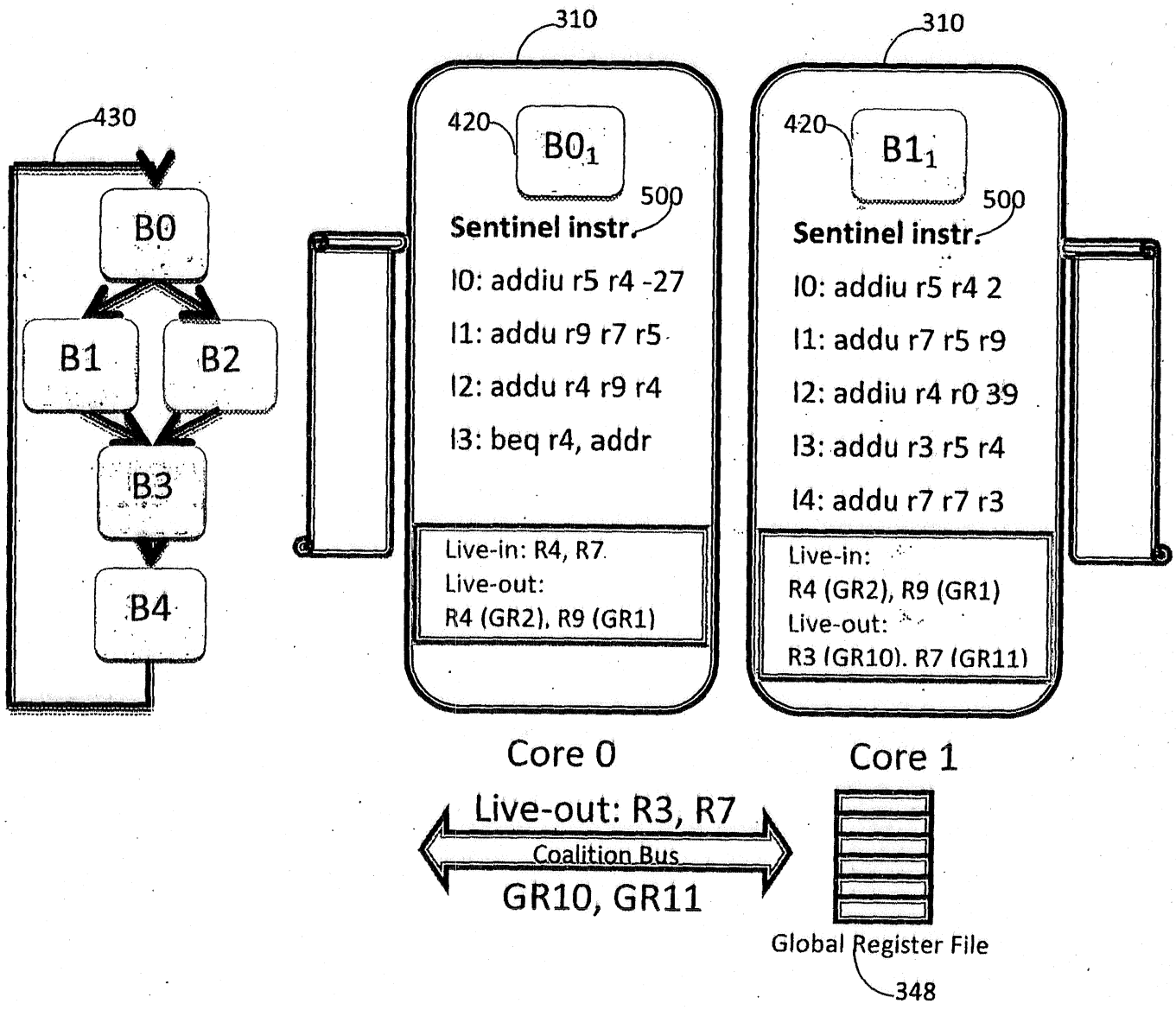
430
B0
B1
B2
B3
B4
310
420
B0$_1$
500
Sentinel instr.
I0: addiu r5 r4 -27
I1: addu r9 r7 r5
I2: addu r4 r9 r4
I3: beq r4, addr
Live-in: R4, R7
Live-out:
R4 (GR2), R9 (GR1)
310
420
B1$_1$
500
Sentinel instr.
I0: addiu r5 r4 2
I1: addu r7 r5 r9
I2: addiu r4 r0 39
I3: addu r3 r5 r4
I4: addu r7 r7 r3
Live-in:
R4 (GR2), R9 (GR1)
Live-out:
R3 (GR10), R7 (GR11)
Core 0
Core 1
Live-out: R3, R7
Coalition Bus
GR10, GR11
Global Register File
348

FIG. 9D

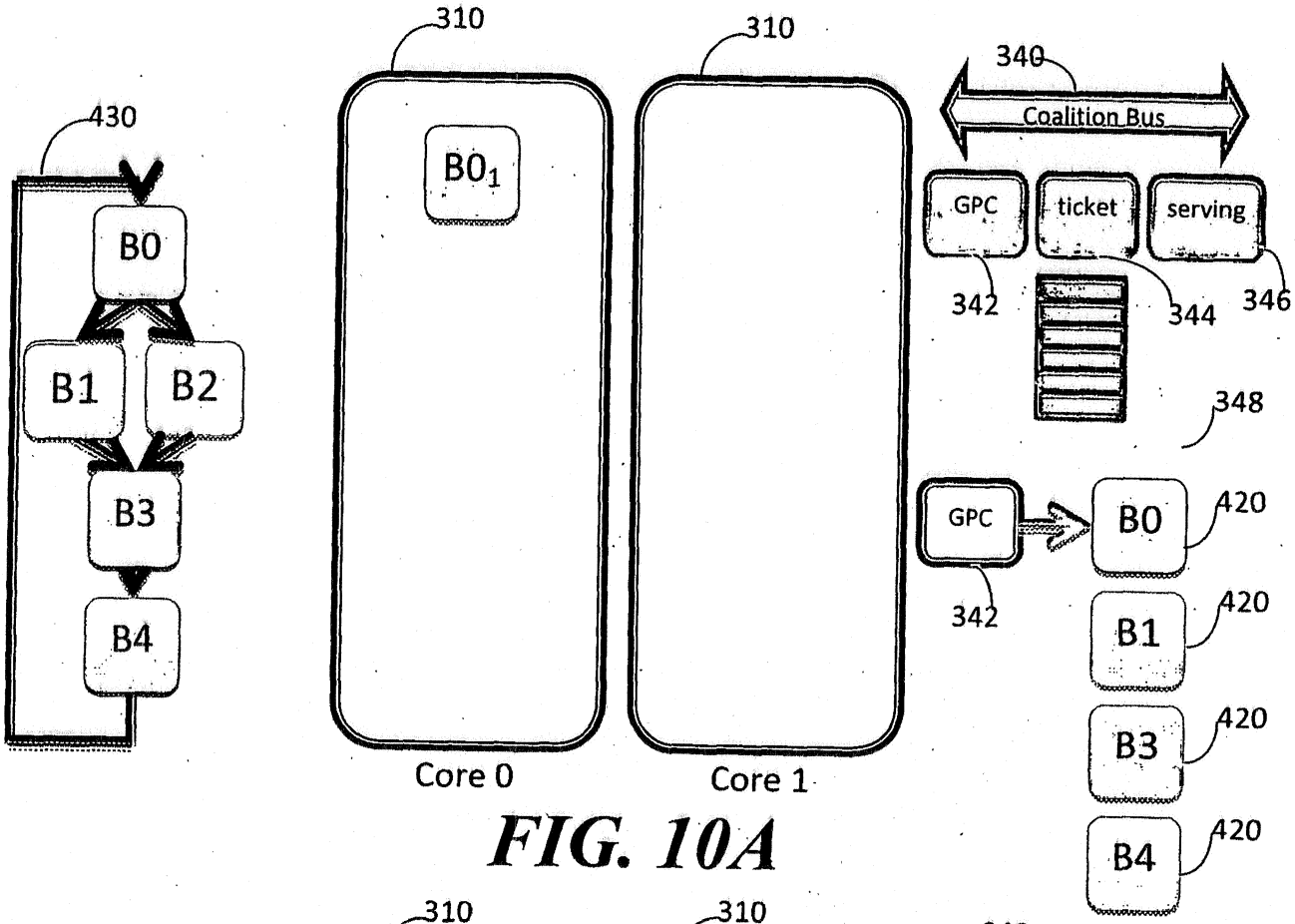

FIG. 10A

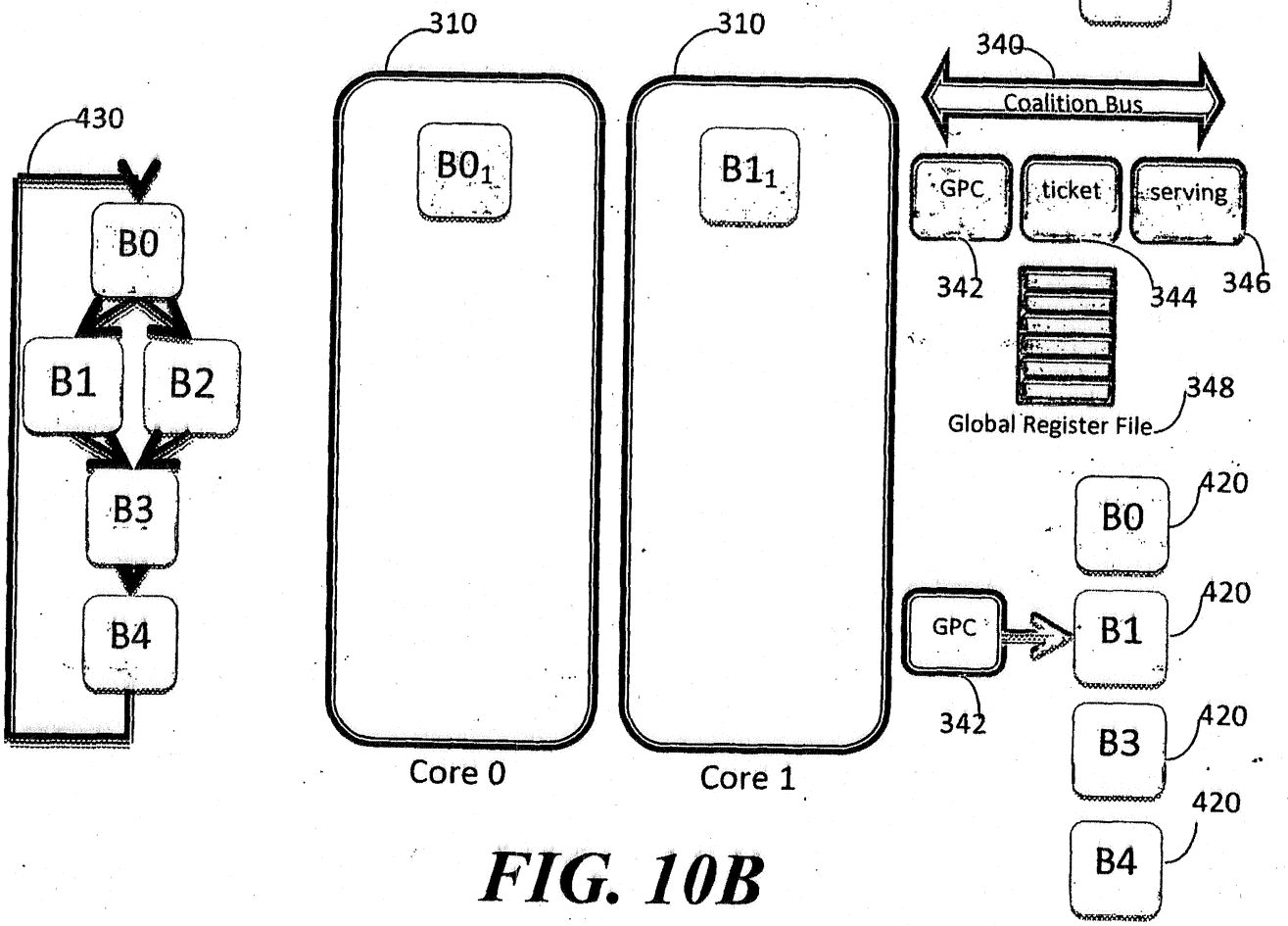

FIG. 10B

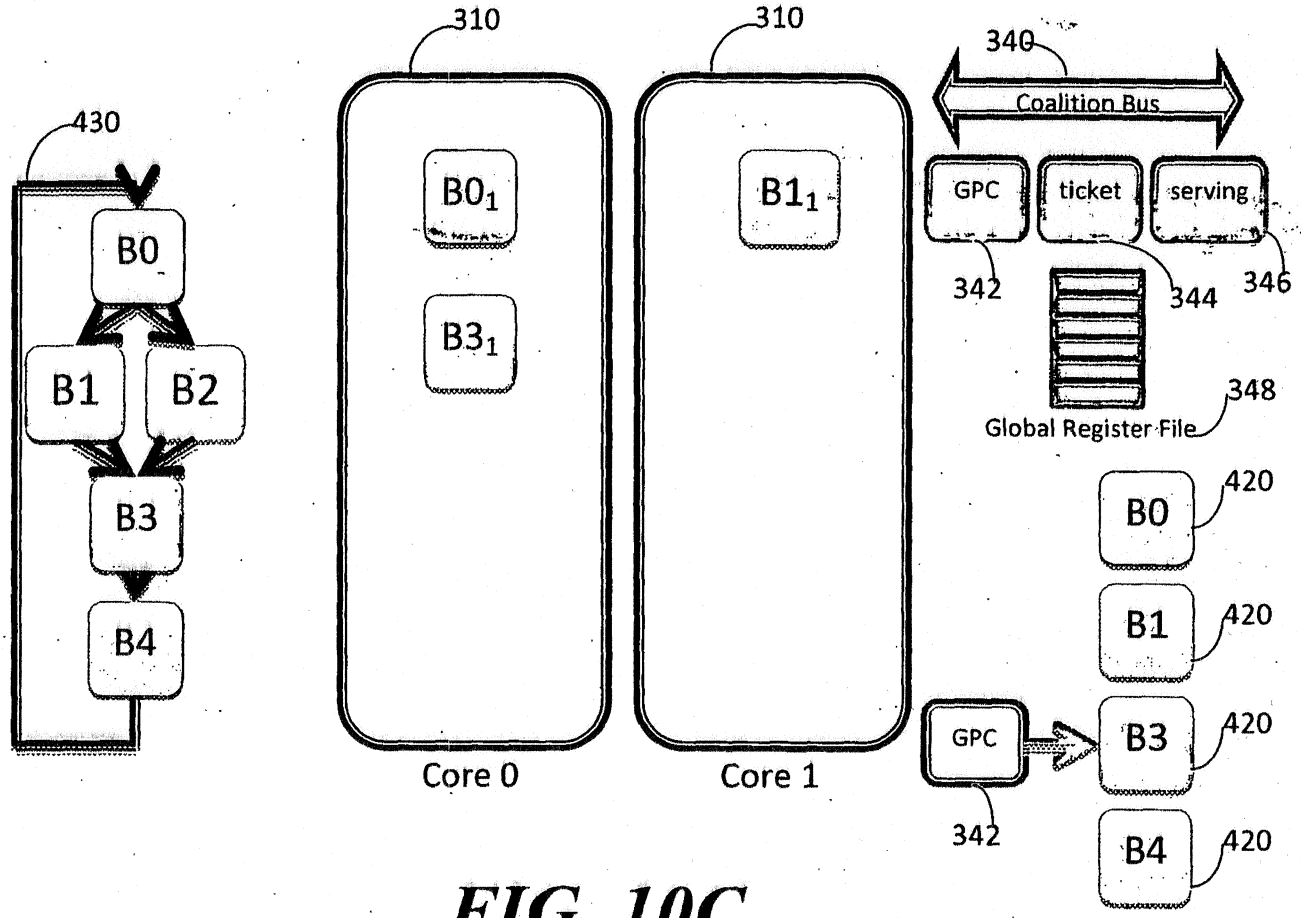

FIG. 10C

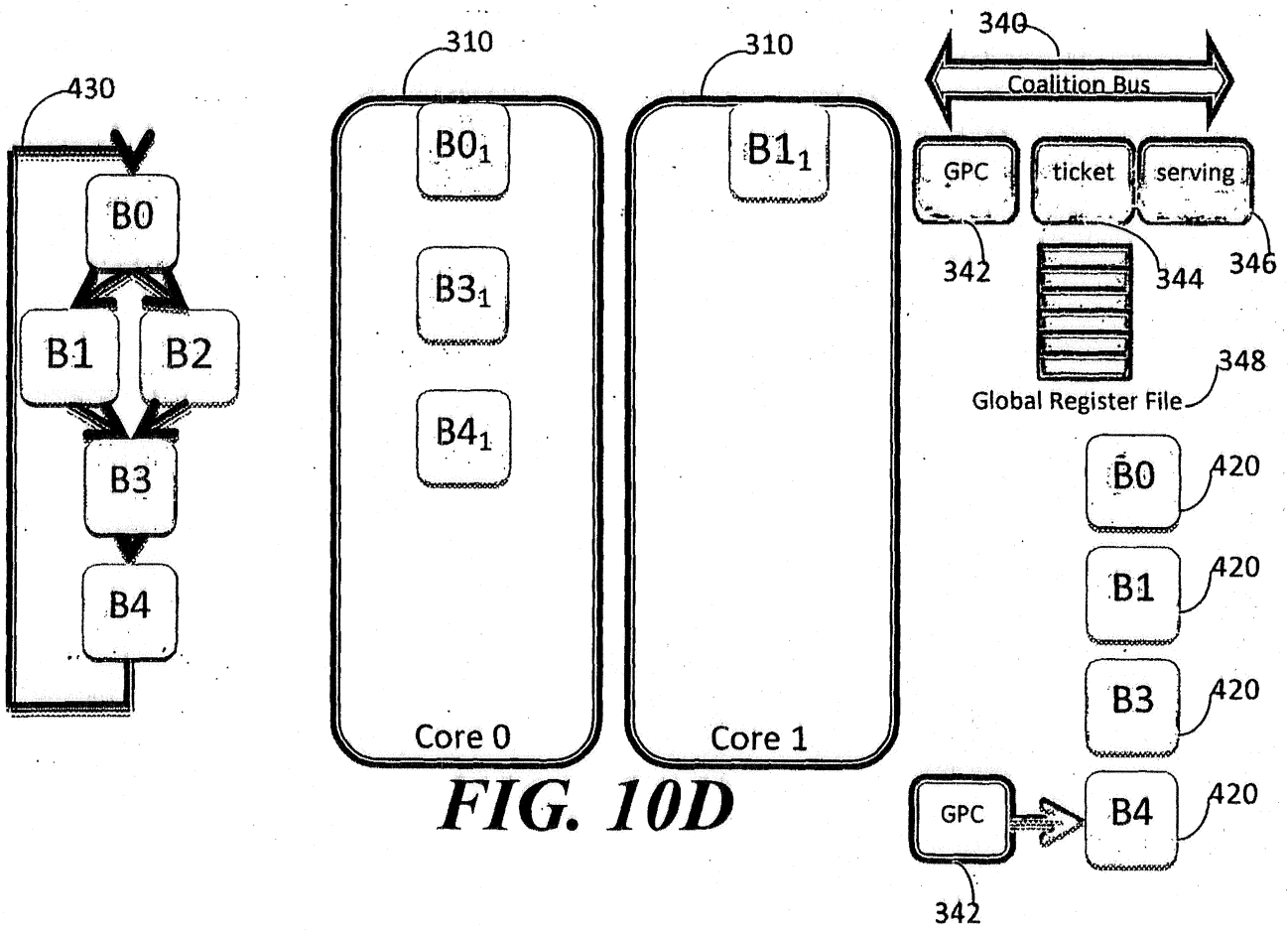

FIG. 10D

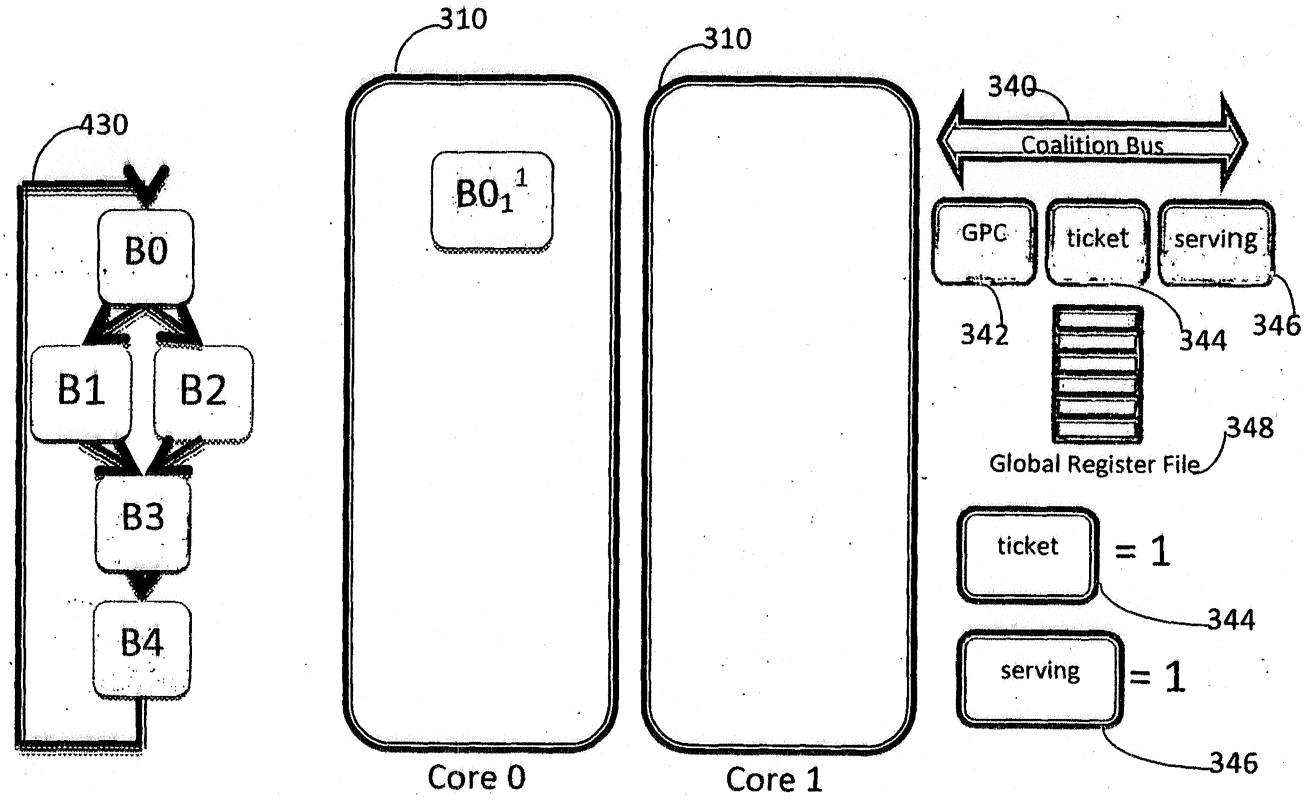

FIG. 11A

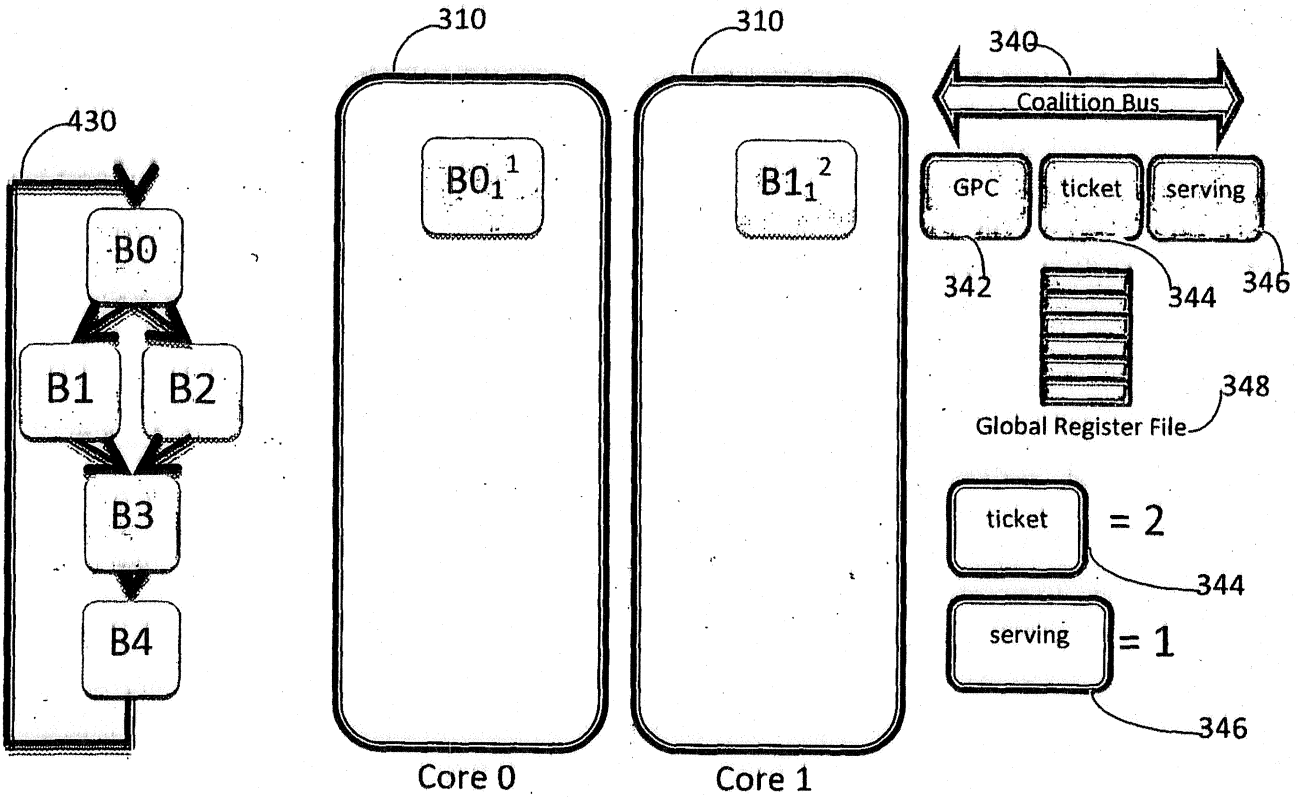

FIG. 11B

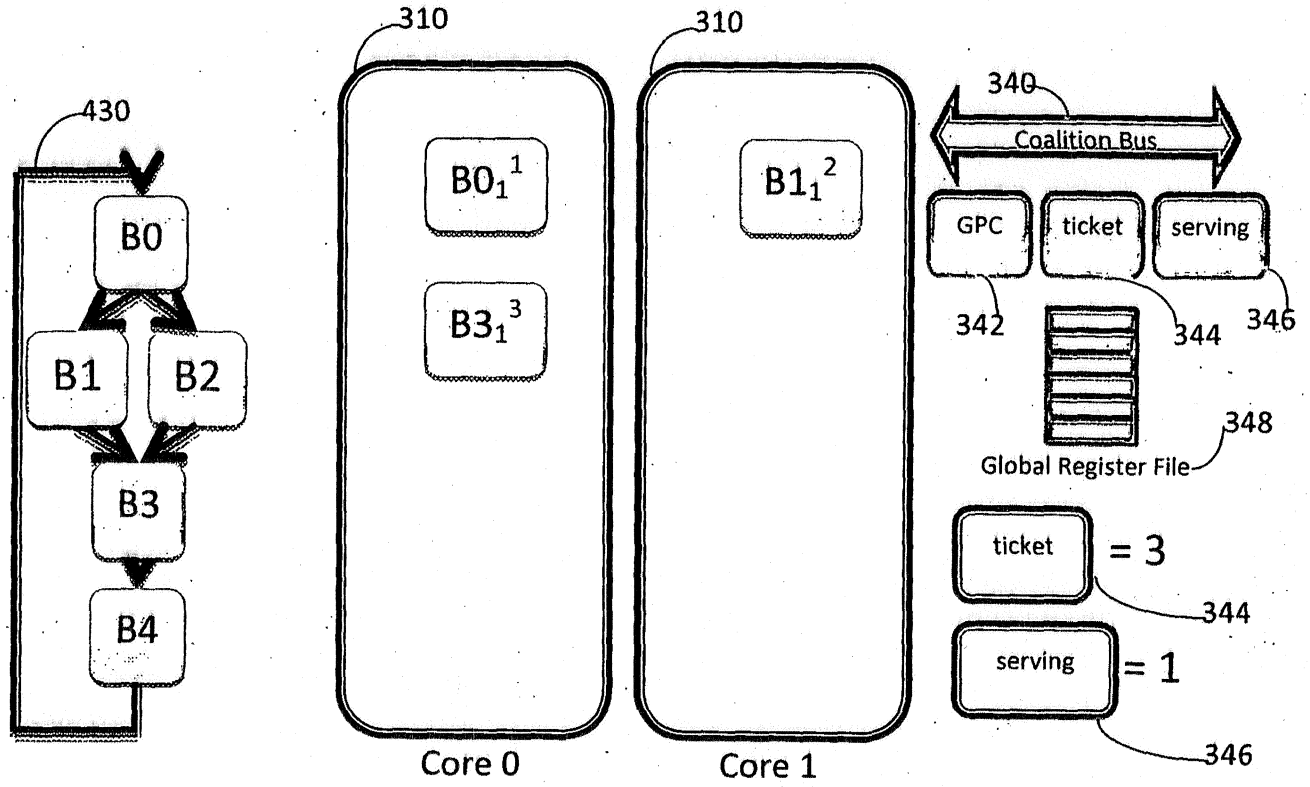

FIG. 11C

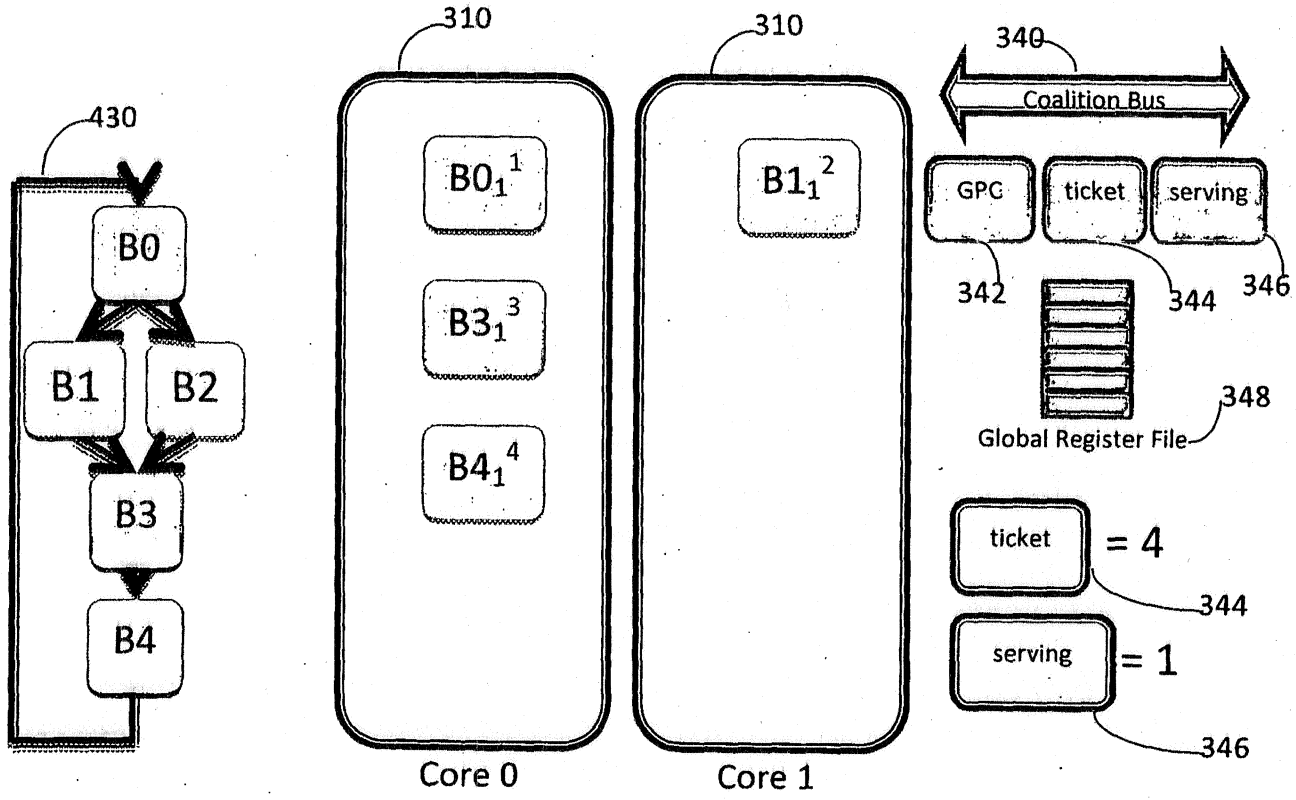

FIG. 11D

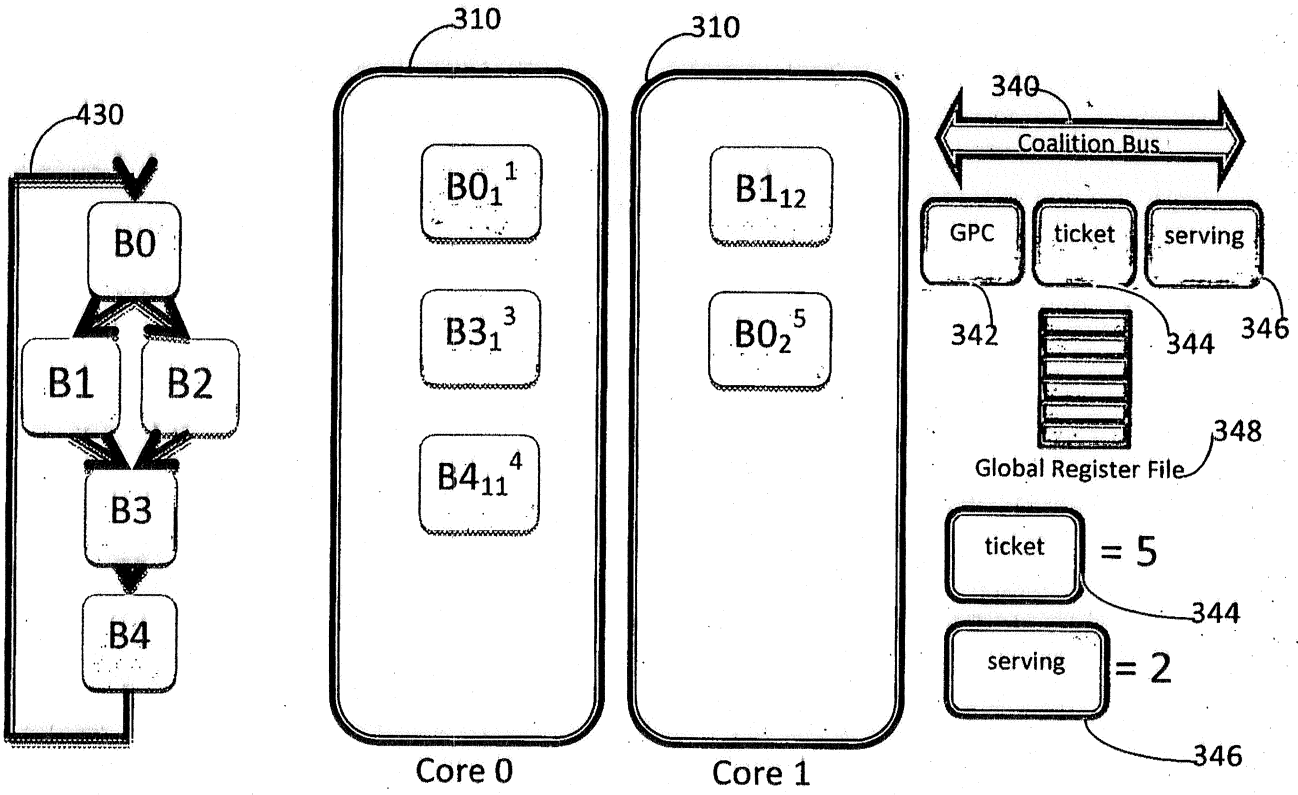

FIG. 11E

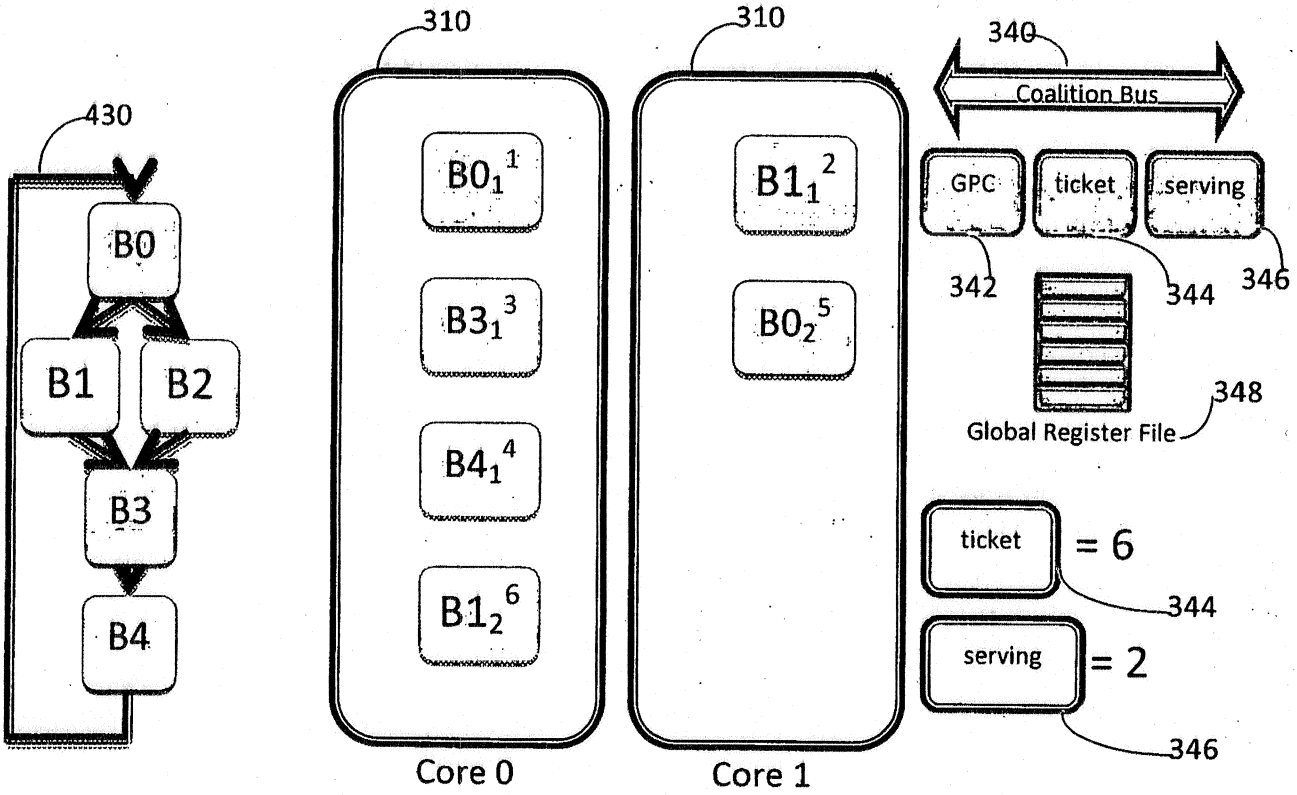

FIG. 11F

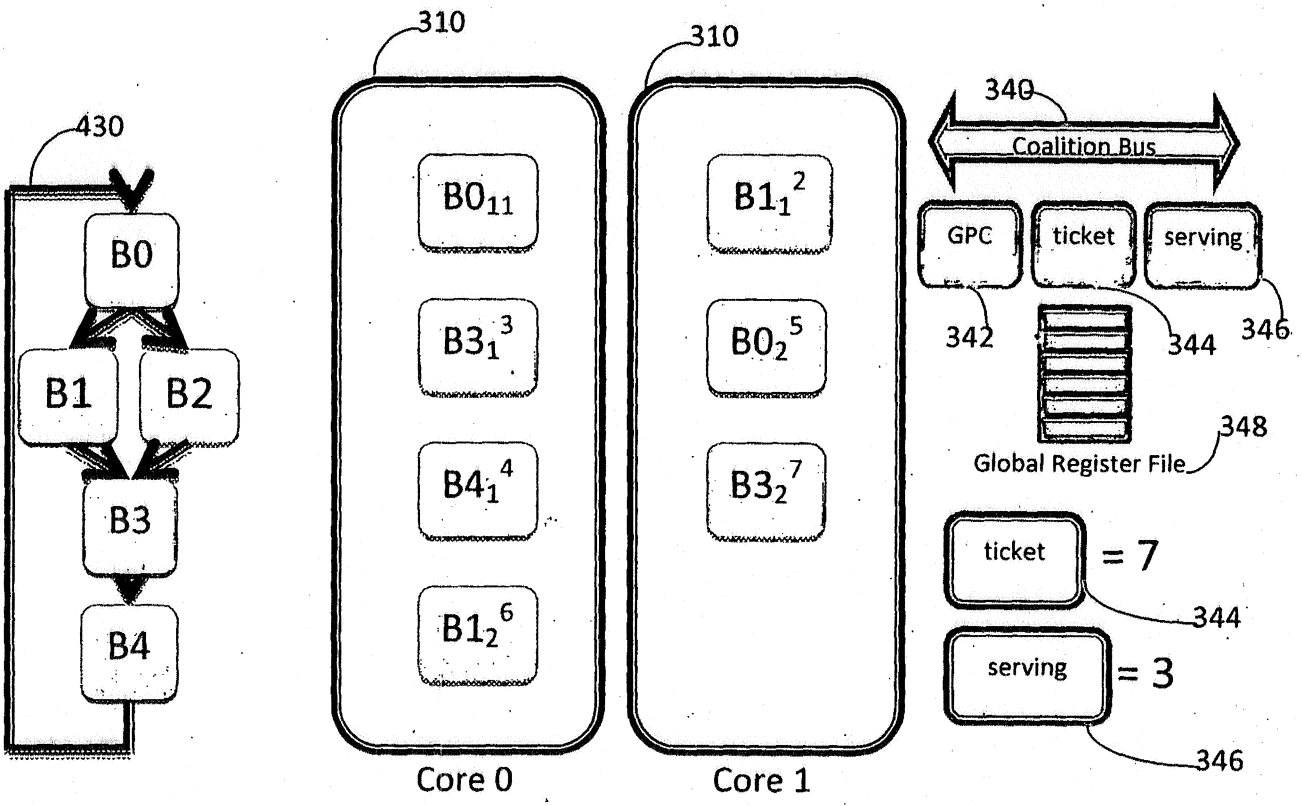

FIG. 11G

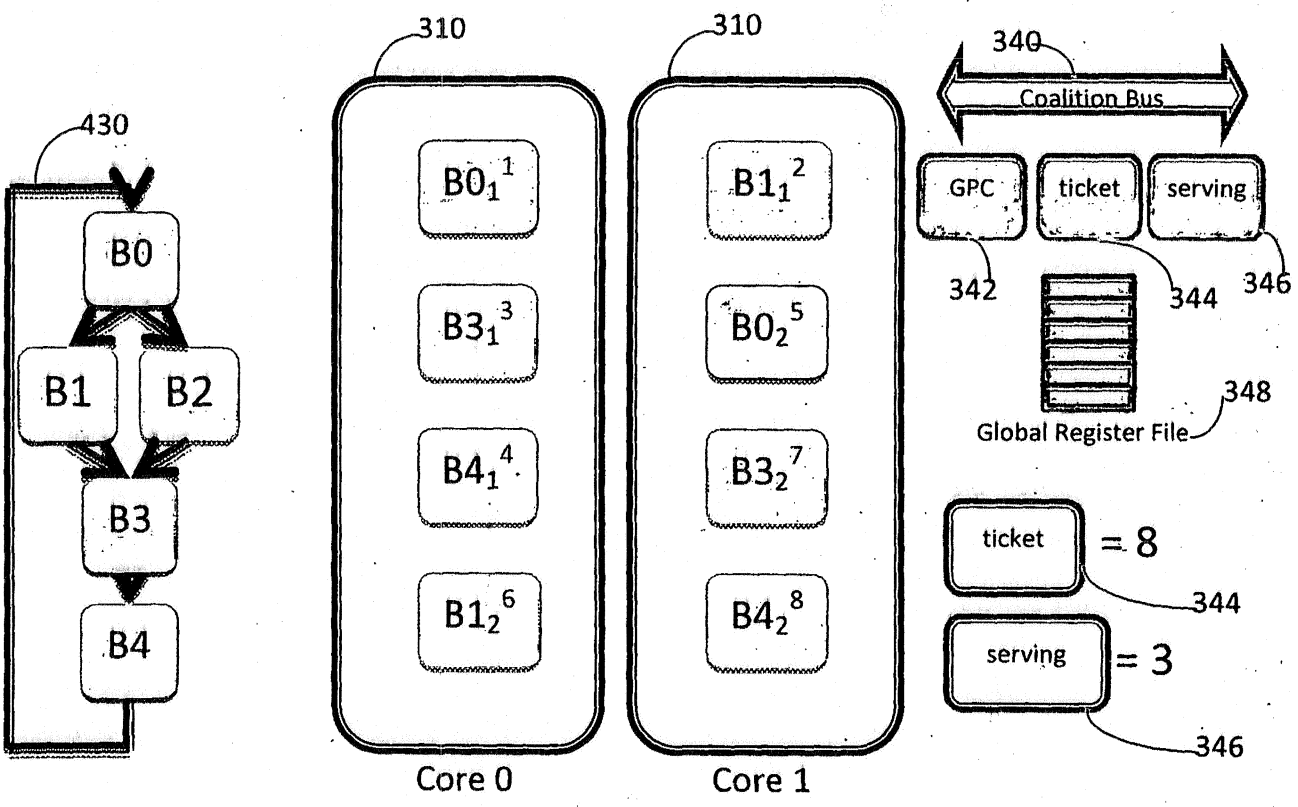

FIG. 11H

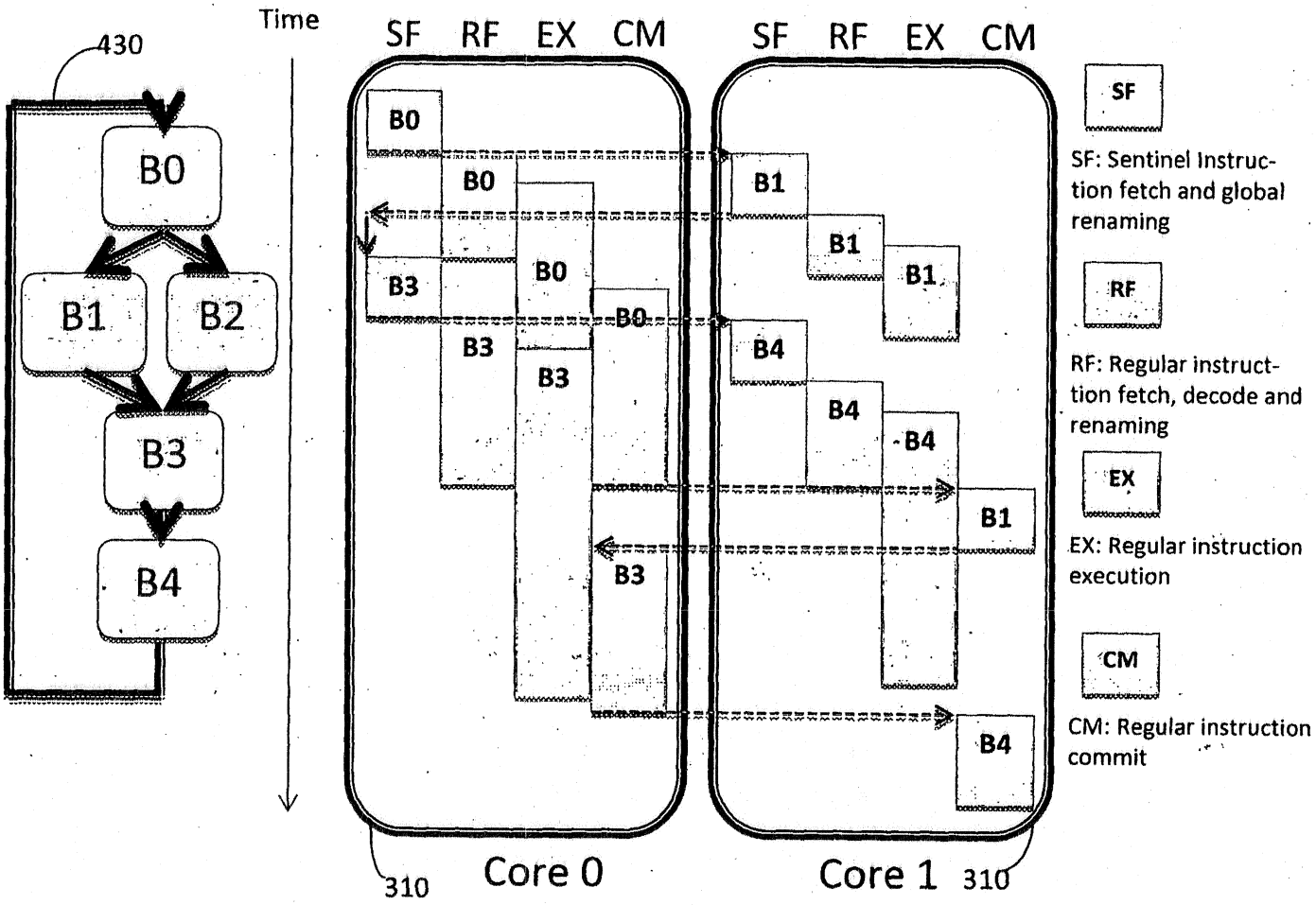
430
B0
B1
B2
B3
B4
Time
SF RF EX CM
SF RF EX CM
B0
B0
B3
B0
B0
B3
B3
B3
B1
B1
B1
B4
B4
B4
B1
B3
B4
310
Core 0
Core 1
310
SF
SF: Sentinel Instruction fetch and global renaming
RF
RF: Regular instruction fetch, decode and renaming
EX
EX: Regular instruction execution
CM
CM: Regular instruction commit

FIG. 12

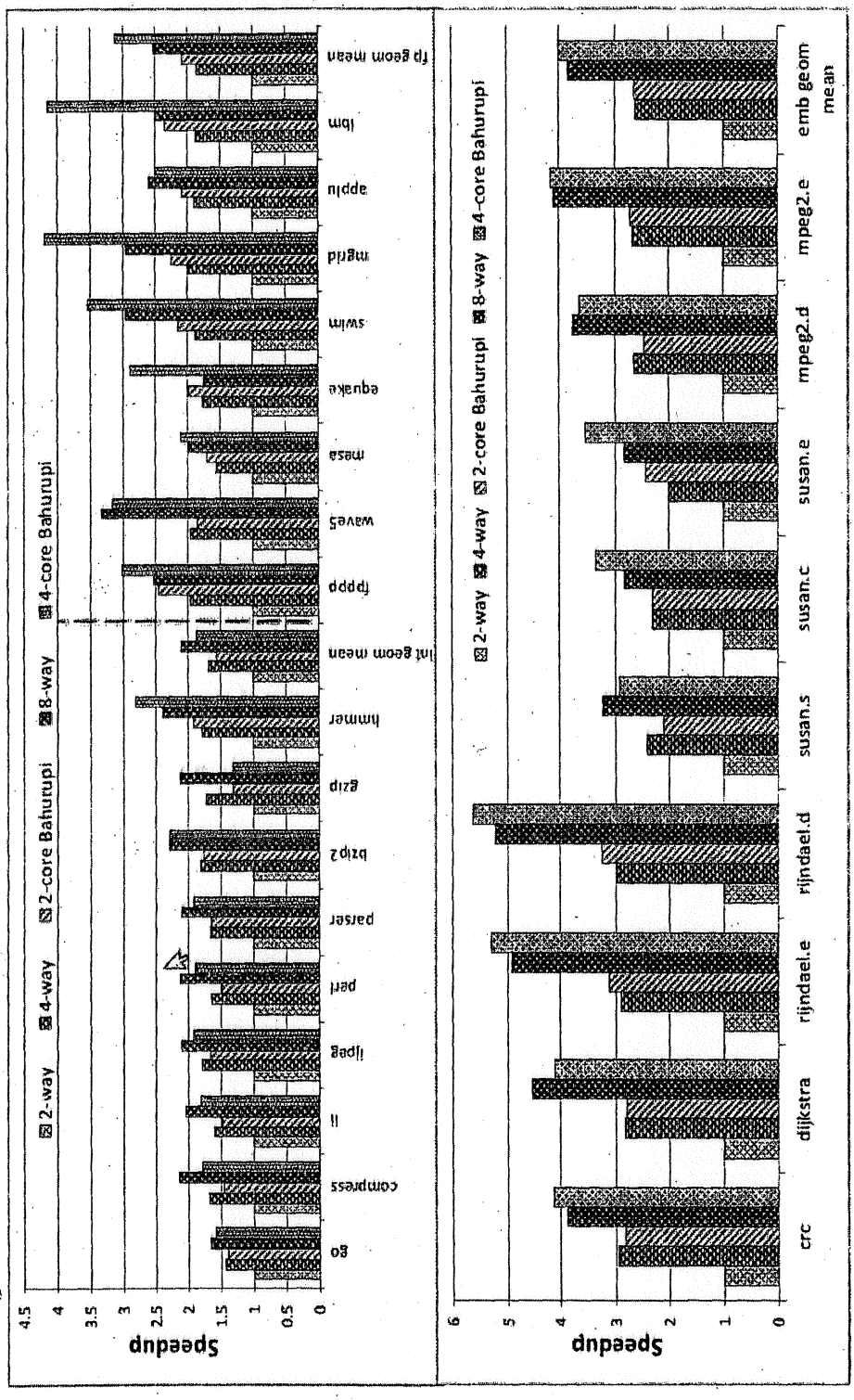
2-way
4-way
2-core Bahurupi
8-way
4-core Bahurupi
Speedup
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
go
compress
li
ijpeg
perl
parser
bzip2
gzip
hmmer
int geom mean
fpppp
wave5
mesa
equake
swim
mgrid
applu
lbm
fp geom mean
6
5
4
3
2
1
0
crc
dijkstra
rijndael.e
rijndael.d
susan.s
susan.c
susan.e
mpeg2.d
mpeg2.e
emb geom mean

FIG. 13A

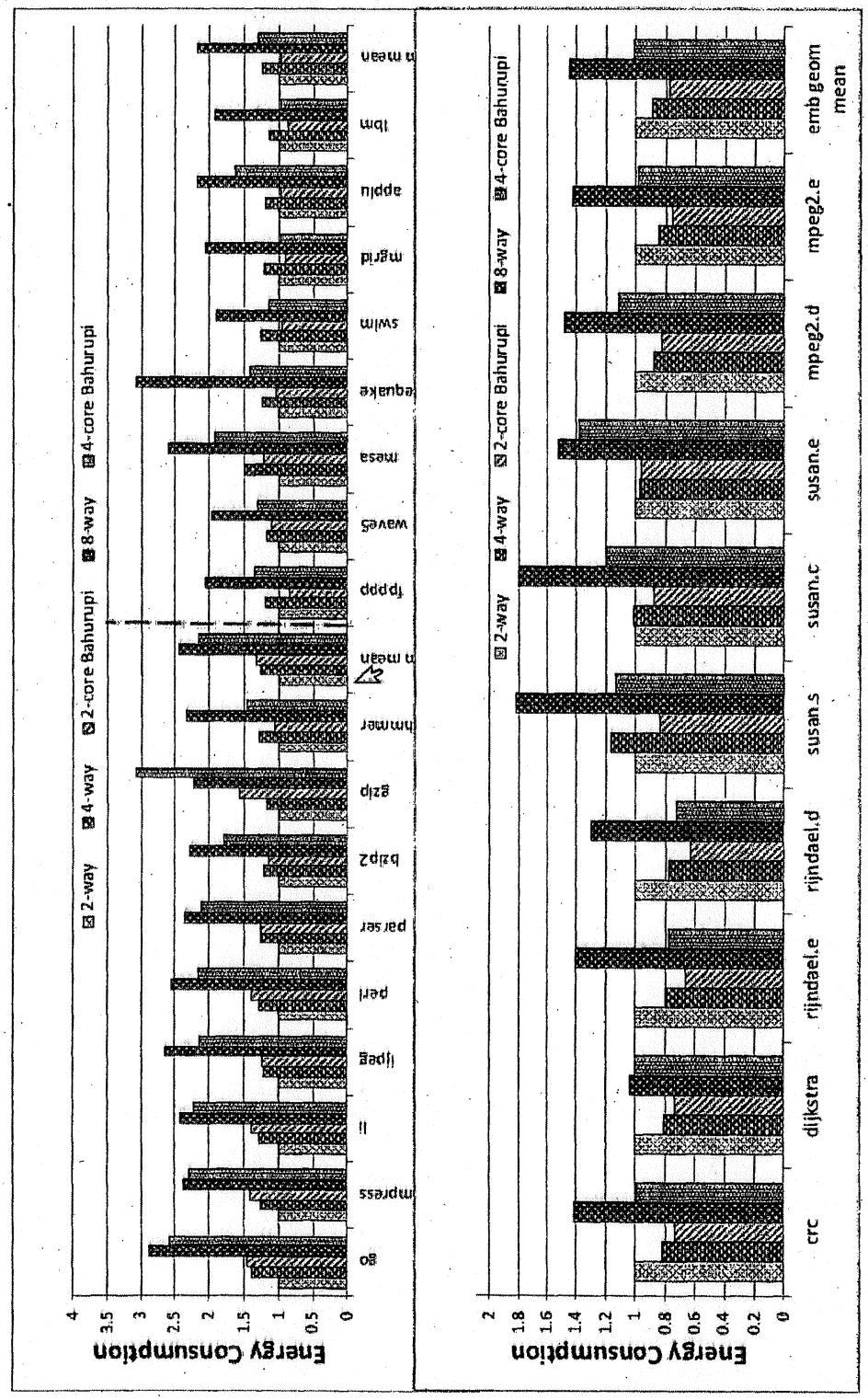
Energy Consumption
2-way
4-way
2-core Bahurupi
8-way
4-core Bahurupi
go
mpress
li
ijpeg
perl
parser
bzip2
gzip
hmmer
n mean
fpppp
wave5
mesa
equake
swim
mgrid
applu
lbm
n mean
crc
dijkstra
rijndael.e
rijndael.d
susan.s
susan.c
susan.e
mpeg2.d
mpeg2.e
emb geom mean

FIG. 13B