

JITTER REDUCTION MODULE

This invention relates generally to automatic test equipment, and more particularly to reducing jitter in a test system clock.

5 Automatic test equipment, generally known as testers, are commonly used in the electronics industry for determining whether electronic components, semiconductor devices, or printed circuit board assemblies contain manufacturing defects. Further, testers generally consist
10 of computerized control circuitry, driver and receiver channels, and tester pins, which connect nodes of a device under test (DUT) to the driver and receiver channels.

During a typical test session, the driver channels apply test signals to the DUT, and the receiver channels
15 detect output signals produced by the DUT in response to the test signals. The output signals are then generally evaluated by comparing them with expected response signals, which would be produced by a properly functioning device.

An important feature of testers is the ability to
20 apply the test signals and to detect the output signals at precisely specified times. Accordingly, testers typically include timing generators, which generate timing signals known as "edges." For example, a first specified edge may cause a driver channel to start applying a test signal,
25 while a second specified edge may cause the driver channel to stop applying the test signal. Similarly, a third specified edge may cause a receiver channel to start detecting output signals, while a fourth specified edge may cause the receiver channel to stop detecting the output
30 signals.

Another important feature of testers is the ability to test the DUT at fast data rates. This is because, in many cases, faults or errors in the DUT can only be detected when the DUT is exercised at data rates that either meet or
35 exceed the operating speed of the DUT.

However, we have recognized that as the data rates of testers increase, it becomes more difficult to specify precisely the times when the edges occur. One reason for this is that jitter, which generally causes the phase of signals to vary over time, usually becomes more prominent with increasing data rates. Such jitter is inherent in test system clocks used by most timing generators.

One way of reducing jitter in the test system clocks is through filtering. In particular, a band-pass filter, centered at the fundamental frequency of a clock, has been used to attenuate jitter components of the clock. However, the band-pass filter also generally attenuates higher-order harmonics of the clock. This means that although the jitter components might be sufficiently reduced, the overall characteristics of the clock may be changed. For example, the attenuation of higher-order harmonics typically reduces the slope of a clock signal at transition regions between high and low voltage levels.

Another way of reducing jitter is to regenerate the clock using a phase-locked loop, which typically includes a voltage-controlled oscillator, a low-pass filter, and a feedback circuit. However, jitter in the regenerated clock is normally dependent upon the quality of the voltage-controlled oscillator. This tends to complicate the design of the phase-locked loop, thereby increasing the cost of testers.

It would therefore be desirable to have a method of reducing jitter in a test system clock that does not alter characteristics of the clock such as voltage level, duty cycle, and overall shape of the clock. It would also be desirable to have a method of reducing jitter that is inexpensive and easy to implement.

SUMMARY OF THE INVENTION

With the foregoing background in mind, it is an object of the invention to reduce jitter components of a test system clock in a tester.

- 5 Another object of the invention is to provide an apparatus for reducing test system clock jitter in a tester that is inexpensive and easy to implement.

The foregoing and other objects are achieved in a jitter reduction module including a clock input, and a
10 first port for providing a clock output with reduced jitter. A first open-circuited tuning stub is connected between the clock input and the first output, and is tuned for providing maximum gain at all integer multiples of the fundamental frequency of a test system clock.

- 15 In a preferred embodiment, the first open-circuited tuning stub has an electrical length that is equal to one-half of the wavelength of the test system clock.

In another embodiment, the jitter reduction module includes a second port for providing a jitter output, and a
20 radio frequency (RF) transformer connected between the clock input and the second output. The RF transformer is preferably a balun having a transforming ratio of 1:1, and a ferrite rod core.

- In still another embodiment, a short-circuited tuning
25 stub is connected between the RF transformer and the second output. The short circuited tuning stub preferably has an electrical length that is equal to one-half of the wavelength of the test system clock.

In yet another embodiment, a second open-circuited
30 tuning stub is connected between the RF transformer and the second output. The second open-circuited tuning stub preferably has an electrical length that is equal to one-quarter of the wavelength of the test system clock.

- Still further objects and advantages will become
35 apparent from a consideration of the ensuing description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

- 5 FIG. 1 is a partial block diagram of a tester
 incorporating a jitter reduction module in
 accordance with the present invention,
 FIG. 2 is a block diagram of the jitter reduction
 module used with FIG. 1, and
10 FIG. 3 is a block diagram of another embodiment of the
 jitter reduction module.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 depicts a partial block diagram of tester 100, which incorporates jitter reduction module 104 in accordance with the present invention.

5 In a typical test configuration, a test engineer develops test programs on computer work station 103. The test programs generally include a series of test vectors. The test engineer also typically enters commands on computer work station 103, including commands for starting
10 a test or specifying operating parameters. In particular, the test engineer might specify a frequency of a test system clock, which is subsequently produced by frequency generator 102, thereby specifying a test cycle. The frequency of the test system clock is typically in the RF
15 band; i.e., from 20 MHz to 800 MHz.

Further, frequency generator 102 is coupled to both frequency reference 101, which provides a reference for the test system clock, and jitter reduction module 104, which is coupled to vector sequencer 105. Jitter reduction
20 module 104 will be discussed in greater detail below.

The test engineer then typically enters a command on computer work station 103 for loading the test programs into memory 110 included in vector sequencer 105. For example, during a specified test cycle, processor 109,
25 which is also included in vector sequencer 105, sequentially reads the test vectors from memory 110, and then sends data values, timing information, and format information to channel 106. As shown, channel 106 is but one of a plurality of channels included in tester 100.
30 Further, tester pin 107, which is also one of a plurality of tester pins, connects channel 106 to one of the nodes of device under test (DUT) 108. The number of tester pins is generally equal to the number of channels in tester 100.

The data values are typically logical values of binary
35 digits 0 and 1, and the format information generally indicates whether the data values are applied to or

captured at certain nodes of DUT 108. Also, the timing information generally indicates when the data values are applied or captured, relative to the beginning of the specified test cycle. Accordingly, channel 106 includes
5 circuitry (not shown) for either applying test data to DUT 108 or capturing output data produced by DUT 108 in response to the test data.

Tester 100 then compares the captured output data with expected data, which is also typically stored in memory
10 110. The comparing is usually implemented in software using processor 109, which generally responds to a series of programmed steps. If the captured output data matches the expected data, then tester 100 would normally indicate that DUT 108 is functioning properly.

15 Frequency reference 101, frequency generator 102, computer work station 103, vector sequencer 105, channel 106, and tester pin 107 represent components that are included in a conventional tester. The construction of each of these components are therefore known to those
20 skilled in this art. It follows that specific implementations of these components are not critical to the present invention.

FIG. 2 shows a block diagram of one embodiment of jitter reduction module 104. Frequency generator 102
25 provides jitter reduction module 104 with the test system clock on line 113, which is the electrical equivalent of a transmission line. In the preferred embodiment, line 113 is a coaxial cable having a center signal conductor for carrying the test system clock, and a grounded outer
30 conductor.

Open-circuited tuning stub 114 is also preferably a coaxial cable having a grounded outer conductor and a center signal conductor, which is coupled to the center signal conductor of line 113. Open-circuited tuning stub
35 114 preferably has an electrical length that is equal to one-half of the wavelength, λ_c , of the test system clock.

For the preferred embodiment shown, both line 113 and open-circuited tuning stub 114 have a characteristic impedance, Z_0 . This simplifies the impedance and gain calculations shown below. However, it should be noted
5 that, in practice, the respective characteristic impedances of line 113 and tuning stub 114 need not be the same.

An important advantage of jitter reduction module 104 is that it reduces jitter in the test system clock without substantially altering characteristics of the clock such as
10 voltage level and overall shape. This is because the gain of jitter reduction module 104 is approximately unity for the fundamental frequency and higher-harmonics of the test system clock.

In particular, it is known that the impedance of open-circuited tuning stub 114 as a function of frequency may be
15 expressed as

$$Z_{114}(f) = -j(Z_0) \cot[(2\pi f / f_c \lambda_c) l_{114}],$$

where f_c is the fundamental frequency of the test system clock, and l_{114} is the electrical length of open-circuited
20 tuning stub 114, which is equal to $\lambda_c/2$ for the preferred embodiment. Accordingly,

$$Z_{114}(f) = -j(Z_0) \cot[(f/f_c)\pi].$$

Further, the gain from the input to the output of jitter reduction module 104 may be expressed as

25
$$A = Z_{114}(f) / [2Z_{114}(f) + Z_0].$$

This quantity will be referred to as the gain at the test system clock output of jitter reduction module 104.

It follows that $Z_{114}(f)$, and therefore A , approach successive maxima as the frequency, f , approaches
30 respective frequencies f_c , $2f_c$, $3f_c$, and so on. Also, $Z_{114}(f)$, and therefore A , approach zero (0) when the frequency, f , approaches respective frequencies $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and so on. This means that maximum gain is achieved for the fundamental frequency and higher-
35 harmonics of the test system clock. Also, because noise with frequencies approaching $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and

so on, normally constitute jitter, jitter components in the test system clock are reduced.

FIG. 3 shows a block diagram of another embodiment of jitter reduction module 104. Frequency generator 102 once again provides jitter reduction module 104 with the test system clock on line 115. In the preferred embodiment, line 115 is a coaxial cable having a center signal conductor for carrying the test system clock, and a grounded outer conductor.

The test system clock on line 115 is introduced at one end of a primary coil of RF transformer 119, which is also commonly known as a transmission line transformer. In the preferred embodiment, RF transformer 119 is a balun having a transforming ratio of 1:1, and a ferrite rod core, thereby making the balun linear. The transforming ratio of 1:1 is chosen for maximizing the bandwidth of RF transformer 119.

Lines 116 and 117, which are also coaxial cables having grounded outer conductors in the preferred embodiment, are coupled to RF transformer 119 at the other end of the primary coil. Line 116 is preferably an open-circuited tuning stub having an electrical length that is equal to one-half of the wavelength, λ_c , of the test system clock. Further, line 117 provides a test system clock with reduced jitter to vector sequencer 105.

The test system clock is induced in a secondary coil of RF transformer 119. One end of the secondary coil is grounded, while the other end of the secondary coil provides jitter output 120 and is coupled to line 118, which is also preferably a coaxial cable with a grounded outer conductor. RF transformer 119 electrically isolates jitter output 120 from line 116, and lines 115 and 117, which are part of the signal path for the test system clock.

Further, lines 115, 116, 117, and 118 each have a characteristic impedance, Z_0 , for the preferred embodiment

shown. This simplifies the impedance and gain calculations that follow. However, the invention described herein is meant to include those embodiments in which lines corresponding to lines 115, 116, 117, and 118 have any appropriate characteristic impedance.

Jitter reduction module 104 uses both lines 116 and 118 as tuning stubs for transmission lines 115 and 117. In particular, it was described above that the impedance of an open-circuited tuning stub, more specifically line 116, as a function of frequency, may be expressed as

$$Z_{116,OPEN}(f) = -j(Z_0)\cot[(2\pi f/f_c\lambda_c)l_{116}],$$

where f_c is the fundamental frequency of the test system clock, and l_{116} is the electrical length of line 116, which is preferably equal to one-half of the wavelength, λ_c , of the test system clock. It follows that

$$Z_{116,OPEN}(f) = -j(Z_0)\cot[(f/f_c)\pi].$$

In the preferred embodiment, line 118 is a short-circuited tuning stub. It is known that the impedance of a short-circuited stub, more specifically line 118, may be expressed as

$$Z_{118,SHORT}(f) = j(Z_0)\tan[2\pi f/f_c\lambda_c)l_{118}].$$

Further, line 118 preferably has an electrical length, l_{118} , that is equal to $\lambda_c/2$. Accordingly,

$$Z_{118,SHORT}(f) = j(Z_0)\tan[(f/f_c)\pi].$$

The gain at the test system clock output of jitter reduction module 104 may be expressed as

$$A_c = (Z_0Z_{116}+Z_{116}Z_{118})/(Z_0Z_{116}+Z_0Z_{118}+2Z_{116}Z_{118}).$$

Also, the gain at jitter output 120 may be expressed as

$$A_J = (Z_0Z_{118}+Z_{116}Z_{118})/(Z_0Z_{116}+Z_0Z_{118}+2Z_{116}Z_{118}).$$

Consequently, $Z_{116,OPEN}(f)$ approaches successive maxima, and $Z_{118,SHORT}(f)$ approaches null, as the frequency, f , approaches respective frequencies f_c , $2f_c$, $3f_c$, and so on. Further, $Z_{116,OPEN}(f)$ approaches null, and $Z_{118,SHORT}(f)$ approaches successive maxima, as f approaches respective frequencies $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and so on.

This means that the gain at the test system clock output, A_c , is approximately unity at respective frequencies f_c , $2f_c$, $3f_c$, and so on, which are the fundamental frequency and higher-harmonics of the test system clock. Also, A_c is approximately null at respective frequencies $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and so on, which normally constitute jitter. Accordingly, line 117 passes a test system clock with reduced jitter to sequencer 105 (FIG. 1).

This also means that the gain at jitter output 120, A_J , is approximately unity at respective frequencies $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and so on. Additionally, A_J is approximately null at respective frequencies f_c , $2f_c$, $3f_c$, and so on. Accordingly, jitter output 120 provides substantially all of the jitter derived from the test system clock.

In still another embodiment, line 118 is an open-circuited tuning stub having an electrical length that is equal to $\lambda_c/4$. Accordingly,

$$Z_{118, OPEN}(f) = -j(Z_0) \cot[(f/2f_c)\pi].$$

Consequently, $Z_{118, OPEN}(f)$ is non-zero as f approaches respective frequencies $(1/2)f_c$, $(3/2)f_c$, $(5/2)f_c$, and so on. Further, $Z_{118, OPEN}(f)$ approaches null as the frequency, f , approaches f_c , $3f_c$, $5f_c$, $7f_c$, and so on, which are the fundamental frequency and odd harmonics of the test system clock.

As a result, line 117 passes a test system clock with more jitter than the preferred embodiment described above, which included line 118 having an electrical length, $\lambda_c/2$, and an impedance, $Z_{118, SHORT}(f)$. However, this embodiment may have advantages of less weight and smaller signal loss for some lower frequency applications.

Another advantage of jitter reduction module 104 is that the jitter provided by jitter output 120 can be measured and analyzed by the test engineer. This is

sometimes useful in evaluating the quality of the test system clock provided by line 117.

Having described one embodiment, alternative embodiments or variations might be made. For example, lines 114, 116, and 118 may be configured with different electrical lengths for achieving optimal weight, signal loss, and jitter reduction for various applications.

Also, alternative embodiments of RF transformer 119 may be used for achieving optimal isolation between line 117, which is the test system clock output, and jitter output 120.

Also, the embodiment of jitter reduction module 104 shown in either FIG. 2 or FIG. 3 may be combined with the prior art apparatus for reducing jitter, which regenerated the test system clock using a phase-locked loop. In particular, jitter reduction module 104 may be coupled to the output of the phase-locked loop for further reducing any jitter that might remain in the regenerated clock.

Therefore, the invention should be limited only by the spirit and scope of the appended claims.



What is claimed is

- 1 1. Automatic test equipment including a jitter reduction
2 module, the jitter reduction module comprising:
3 (a) a transmission line for carrying a test system
4 clock; and
5 (b) a tuning stub coupled to the transmission line.
- 1 2. The automatic test equipment as recited in claim 1,
2 wherein the tuning stub is a coaxial cable with an
3 open-circuited termination.
- 1 3. The automatic test equipment as recited in claim 2,
2 wherein the tuning stub has an electrical length equal
3 to one-half of the wavelength of the test system
4 clock.
- 1 4. Automatic test equipment including a jitter reduction
2 module, the jitter reduction module comprising:
3 (a) a first transmission line for inputting a test
4 system clock;
5 (b) an RF transformer having a primary coil and a
6 secondary coil, the first transmission line being
7 coupled to one end of the primary coil;
8 (c) a second transmission line for outputting a test
9 system clock with reduced jitter, coupled to an
10 opposite end of the primary coil;
11 (d) a first tuning stub coupled to the opposite end
12 of the primary coil; and
13 (e) a second tuning stub coupled to the secondary
14 coil.
- 1 5. The automatic test equipment as recited in claim 4,
2 wherein the RF transformer is a 1:1 balun.
- 1 6. The automatic test equipment as recited in claim 4,





- 2 wherein the first tuning stub is a coaxial cable with
3 an open-circuited termination.
- 1 7. The automatic test equipment as recited in claim 6,
2 wherein the first tuning stub has an electrical length
3 equal to one-half of the wavelength of the test system
4 clock.
- 1 8. The automatic test equipment as recited in claim 4,
2 wherein the second tuning stub is a coaxial cable with
3 a short-circuited termination.
- 1 9. The automatic test equipment as recited in claim 8,
2 wherein the second tuning stub has an electrical
3 length equal to one-half of the wavelength of the test
4 system clock.
- 1 10. The automatic test equipment as recited in claim 4,
2 wherein the second tuning stub is a coaxial cable with
3 an open-circuited termination.
- 1 11. The automatic test equipment as recited in claim 10,
2 wherein the second tuning stub has an electrical
3 length equal to one-quarter of the wavelength of the
4 test system clock.
- 1 12. A clock jitter reduction module, comprising:
2 (a) a first cable for providing a clock signal
3 delivery path; and
4 (b) a second cable, coupled to the first cable, for
5 tuning the clock signal delivery path using
6 microwave techniques.
- 1 13. The clock jitter reduction module as recited in claim
2 12,





3 wherein the second cable is a coaxial cable with an
4 open-circuited termination.

1 14. The clock jitter reduction module as recited in claim
2 13,
3 wherein the second cable has an electrical length
4 equal to one-half of the wavelength of the clock
5 signal.

1 15. A clock jitter reduction module, comprising:
2 (a) a first cable for inputting a clock signal;
3 (b) an RF transformer having a primary and a
4 secondary coil, one end of the primary coil being
5 coupled to the first cable;
6 (c) a second cable coupled to an opposite end of the
7 primary coil, for outputting a clock signal with
8 reduced jitter;
9 (d) a third cable having an open-circuited
10 termination coupled to the opposite end of the
11 primary coil; and
12 (e) a fourth cable having a short-circuited
13 termination coupled to the secondary coil.

1 16. The clock jitter reduction module as recited in claim
2 15,
3 wherein the RF transformer is a 1:1 balun.

1 17. The clock jitter reduction module as recited in claim
2 15,
3 wherein the third cable has an electrical length equal
4 to one-half of the wavelength of the clock signal.

1 18. The clock jitter reduction module as recited in claim
2 15,





3 wherein the fourth cable has an electrical length
4 equal to one-half of the wavelength of the clock
5 signal.

1 19. The clock jitter reduction module as recited in claim
2 15,
3 wherein the fourth cable has an open-circuited
4 termination.

1 20. The clock jitter reduction module as recited in claim
2 19,
3 wherein the fourth cable has an electrical length
4 equal to one-quarter of the wavelength of the clock
5 signal.

This Sheet Has Been Replaced

