

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
20 January 2005 (20.01.2005)

PCT

(10) International Publication Number
WO 2005/006340 A3

(51) International Patent Classification⁷: **G11C 11/413**

(21) International Application Number:

PCT/US2004/021162

(22) International Filing Date: 30 June 2004 (30.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/484,565 1 July 2003 (01.07.2003) US

(71) Applicant (for all designated States except US): **ZMOS TECHNOLOGY, INC.** [US/US]; 1290 Oakmead Parkway, Suite 318, Sunnyvale, CA 94085 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **SOHN, Jeong-Duk** [KR/US]; 1841 Paseo Del Cajon, Pleasanton, CA 94566 (US).

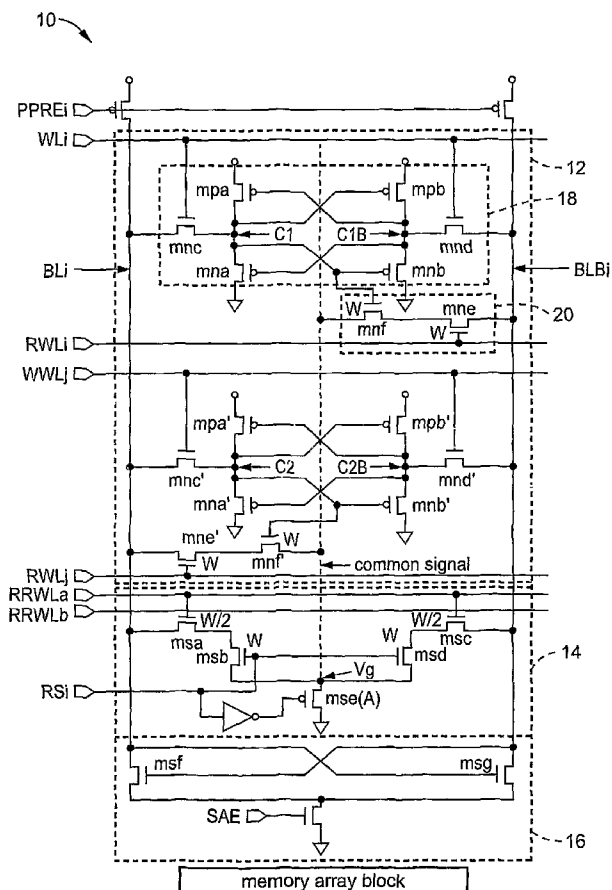
(74) Agent: **O'BANION, John, P.**; O'Banion & Ritchey LLP, Suite 1550, 400 Capitol Mall, Sacramento, CA 95814 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,

[Continued on next page]

(54) Title: SRAM CELL STRUCTURE AND CIRCUITS



(57) Abstract: An SRAM circuit structure and method for reducing leakage currents and/or increasing the speed of the devices. Various forms of SRAM devices may be fabricated utilizing the techniques, such as single port and dual port RAM devices. By way of example the SRAM structure utilizes separate write and read lines, splits the circuit into portions which can benefit from having differing threshold levels, and can allow splitting read path transistors for connection to a first terminal and a virtual node connected to a source transistor. The structure is particularly well suited for forming transistors in a combination of NMOS and PMOS, or solely in NMOS. Memory arrays may be organized according to the invention in a number of different distributed or lumped arrangements with the reference read paths and sense blocks being either shared or dedicated.

WO 2005/006340 A3



SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:

30 June 2005