CLAIMS

What is claimed is:

1. A tunnel field effect transistor comprising:
a source structure;
a transition layer adjacent the source structure;
an intrinsic channel layer adjacent the transition layer; and
a drain structure adjacent the intrinsic channel

2. The tunnel field effect transistor of claim 1, wherein the source structure is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

3. The tunnel field effect transistor of claim 2, wherein the source structure is a gallium/arsenic/antimony alloy.

4. The tunnel field effect transistor of claim 2, wherein the source structure is a indium/gallium/arsenic alloy

5. The tunnel field effect transistor of claim 1, wherein the transition layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

6. The tunnel field effect transistor of claim 2, wherein the transition layer is indium arsenide.

7. The tunnel field effect transistor of claim 2, wherein the transition layer is indium/gallium/arsenide alloy.

8. The tunnel field effect transistor of claim 1, wherein the intrinsic layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

9. The tunnel field effect transistor of claim 2, wherein the intrinsic layer is indium phosphide.

10. The tunnel field effect transistor of claim 2, wherein the intrinsic layer is formed of multiple layers.

11. An electronic system, comprising:

a processor; and

a memory device in data communication with the processor;

wherein at least one of the processor and the memory device includes at least one tunnel field effect transistor comprising:

a source structure;

a transition layer adjacent the source structure;

an intrinsic channel layer adjacent the transition layer; and

a drain structure adjacent the intrinsic channel

12. The electronic system of claim 11, wherein the source structure is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

13. The electronic system of claim 12, wherein the source structure is a gallium/arsenic/antimony alloy.

14. The electronic system of claim 12, wherein the source structure is a indium/gallium/arsenic alloy

15. The electronic system of claim 11, wherein the transition layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

16. The electronic system of claim 12, wherein the transition layer is indium arsenide.

17. The electronic system of claim 12, wherein the transition layer is indium/gallium/arsenide alloy.

18. The electronic system of claim 11, wherein the intrinsic layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

19. The electronic system of claim 12, wherein the intrinsic layer is indium phosphide.

20. The electronic system of claim 12, wherein the intrinsic layer is formed of multiple layers.

CLAIMS

What is claimed is:

1. A tunnel field effect transistor comprising:
a source structure;

a transition layer, formed of multiple layers, adjacent the source structure;

an intrinsic channel layer adjacent the transition layer; and

a drain structure adjacent the intrinsic channel;

wherein a first layer of the multiple layers of the transition layer abuts the source structure forming a heterojunction; wherein a second layer of the multiple layers of the transition layer abuts the intrinsic channel layer forming a heterojunction; wherein the first layer of the multiple layers of the transition layer separates the second layer of the multiple layers of the transition layer from the source structure; wherein the second layer of the multiple layers of the transition layer separates the first layer of the multiple layers of the transition layer from the intrinsic channel layer; and a heterojunction between the first layer and the second layer of the multiple layers of the transition layer.

2. The tunnel field effect transistor of claim 1, wherein the source structure is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

3. The tunnel field effect transistor of claim 2, wherein the source structure is a gallium/arsenic/antimony alloy.

4. The tunnel field effect transistor of claim 2, wherein the source structure is a indium/gallium/arsenic alloy.

5. The tunnel field effect transistor of claim 2, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is indium arsenide.

6. The tunnel field effect transistor of claim 2, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is indium/gallium/arsenide alloy.

7. The tunnel field effect transistor of claim 2, wherein the intrinsic layer is indium phosphide.

8. The tunnel field effect transistor of claim 1, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

9. The tunnel field effect transistor of claim 1, wherein the intrinsic layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

10. An electronic system, comprising:
a processor; and

a memory device in data communication with the processor;

wherein at least one of the processor and the memory device includes at least one tunnel field effect transistor comprising:
a source structure;

a transition layer, formed of multilayers, adjacent the source structure;

an intrinsic channel layer adjacent the transition layer; and

a drain structure adjacent the intrinsic channel;

wherein a first layer of the multiple layers of the transition layer abuts the source structure forming a heterojunction; wherein a second layer of the multiple layers of the transition layer abuts the intrinsic channel layer forming a heterojunction; wherein the first layer of the multiple layers of the transition layer separates the second layer of the multiple layers of the transition layer from the source structure; wherein the second layer of the multiple layers of the transition layer separates the first layer of the multiple layers of the transition layer from the intrinsic channel layer; and a heterojunction between the first layer and the second layer of the multiple layers of the transition layer.

11. The electronic system of claim 10, wherein the source structure is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

12. The electronic system of claim 11, wherein the source structure is a gallium/arsenic/antimony alloy.

13. The electronic system of claim 11, wherein the source structure is a indium/gallium/arsenic alloy.

14. The electronic system of claim 11, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is indium arsenide.

15. The electronic system of claim 11, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is indium/gallium/arsenide alloy.

16. The electronic system of claim 11, wherein the intrinsic layer is indium phosphide.

17. The electronic system of claim 10, wherein at least one of the first layer and the second layer of the multiple layers of the transition layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.

18. The electronic system of claim 10, wherein the intrinsic layer is an alloy of aluminum, antimony, arsenide, gallium, indium, nitrogen, or phosphorous.