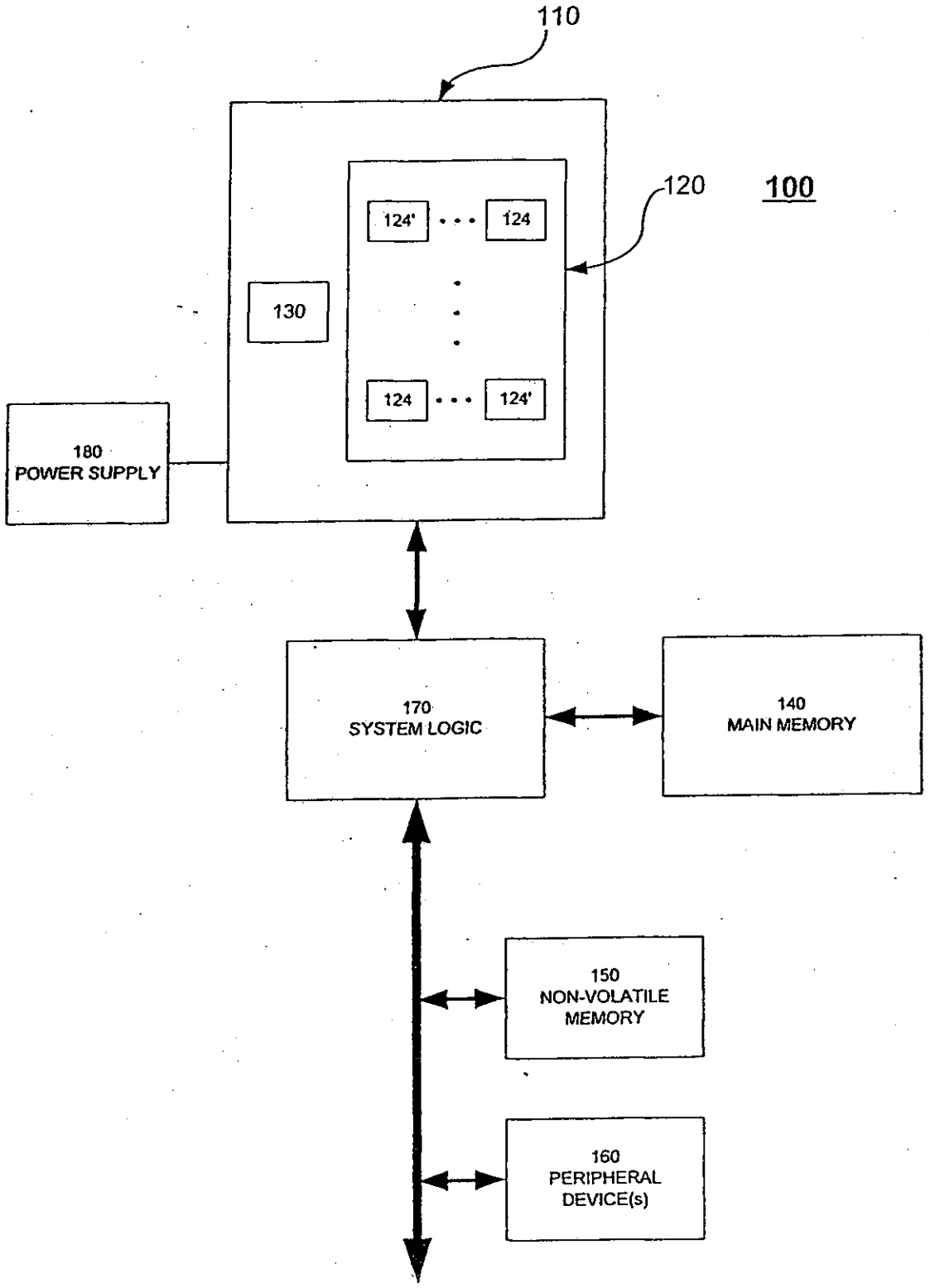

110
120
100
124'
124
130
124
124'
180
POWER SUPPLY
170
SYSTEM LOGIC
140
MAIN MEMORY
150
NON-VOLATILE
MEMORY
160
PERIPHERAL
DEVICE(s)

Fig. 1

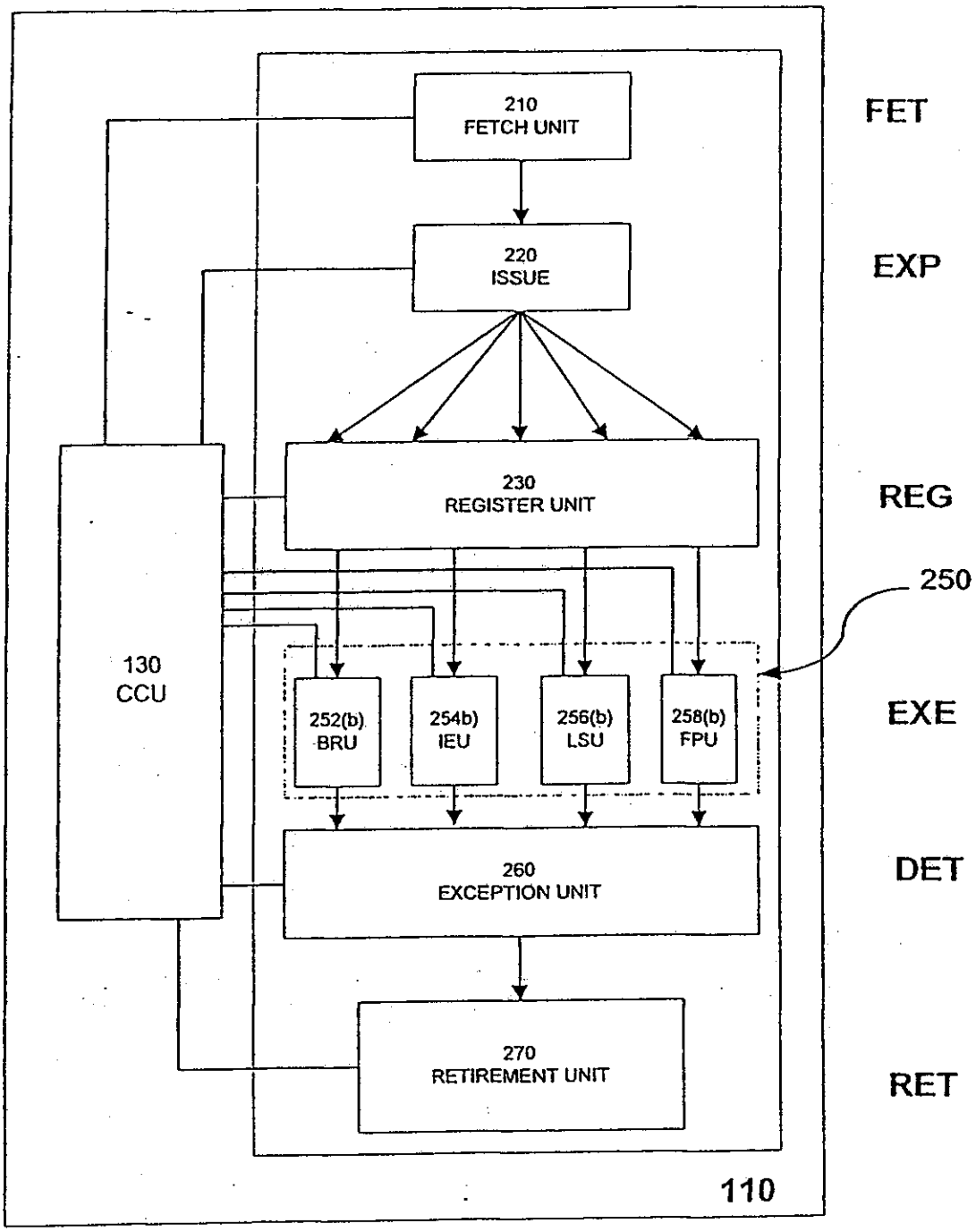

210
FETCH UNIT
220
ISSUE
230
REGISTER UNIT
130
CCU
252(b)
BRU
254b)
IEU
256(b)
LSU
258(b)
FPU
260
EXCEPTION UNIT
270
RETIREMENT UNIT
110
FET
EXP
REG
250
EXE
DET
RET

Fig. 2

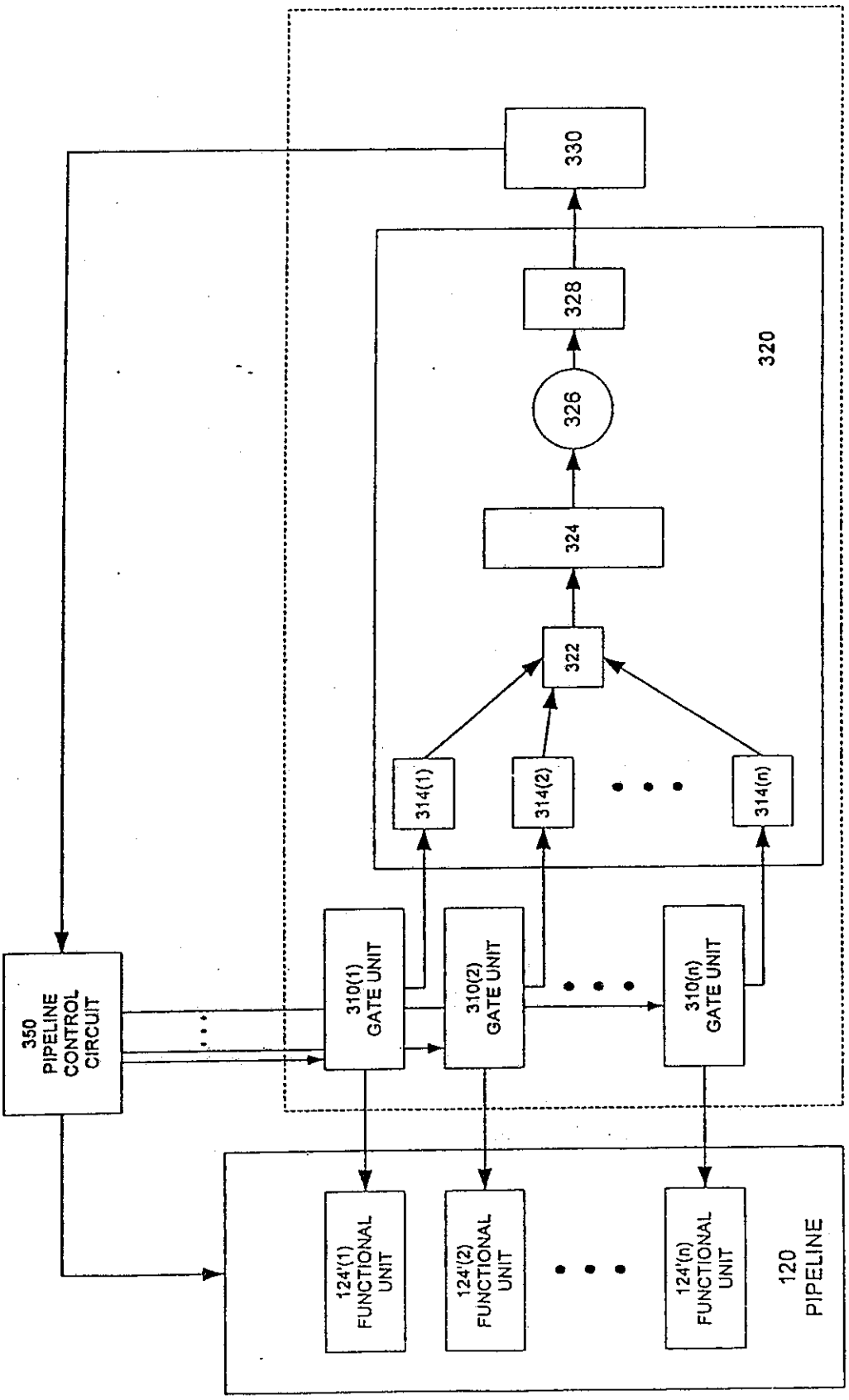

330
328
320
326
324
322
314(1)
314(2)
314(n)
350
PIPELINE
CONTROL
CIRCUIT
310(1)
GATE UNIT
310(2)
GATE UNIT
310(n)
GATE UNIT
124'(1)
FUNCTIONAL
UNIT
124'(2)
FUNCTIONAL
UNIT
124'(n)
FUNCTIONAL
UNIT
120
PIPELINE

Fig. 3

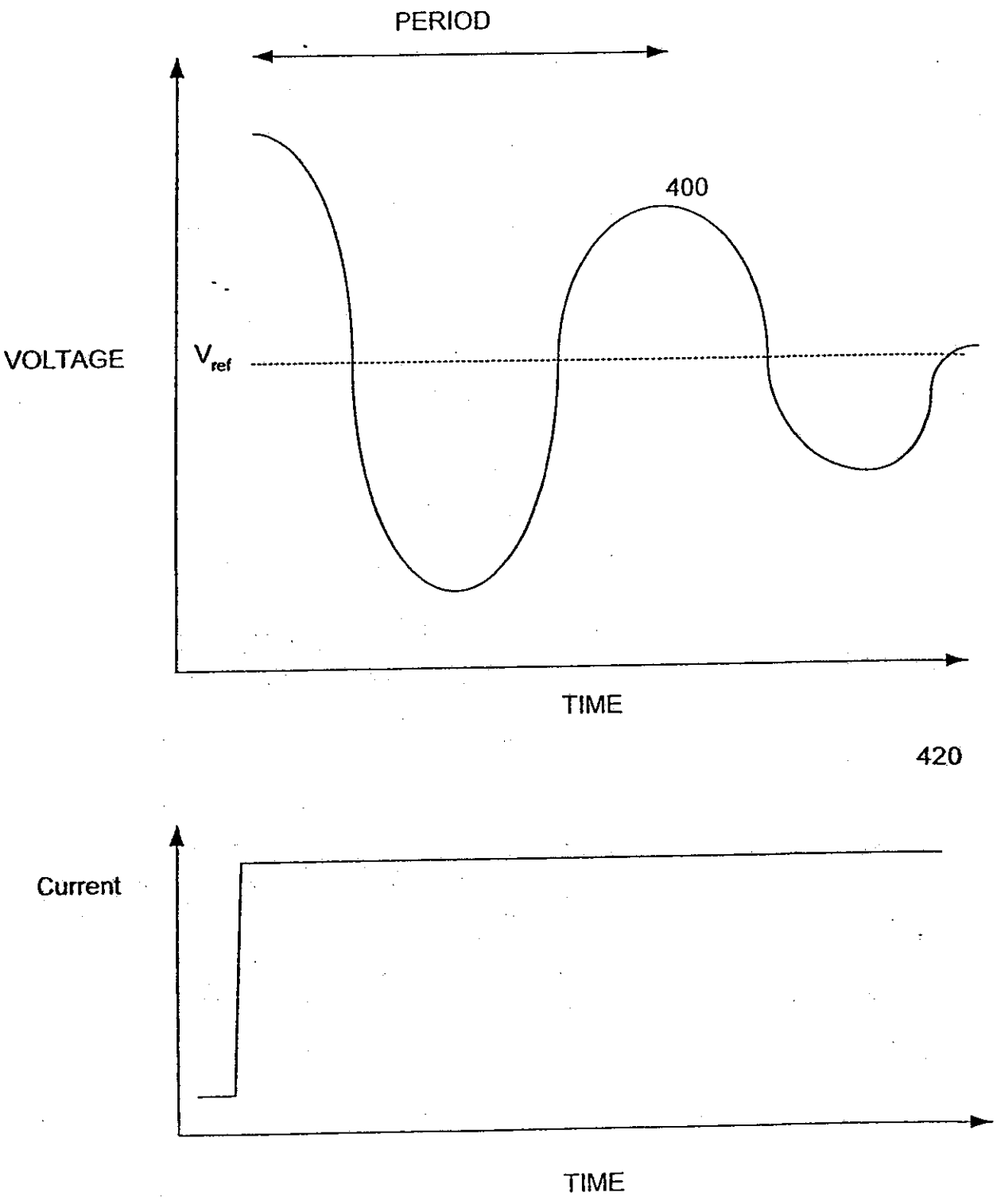


Fig. 4

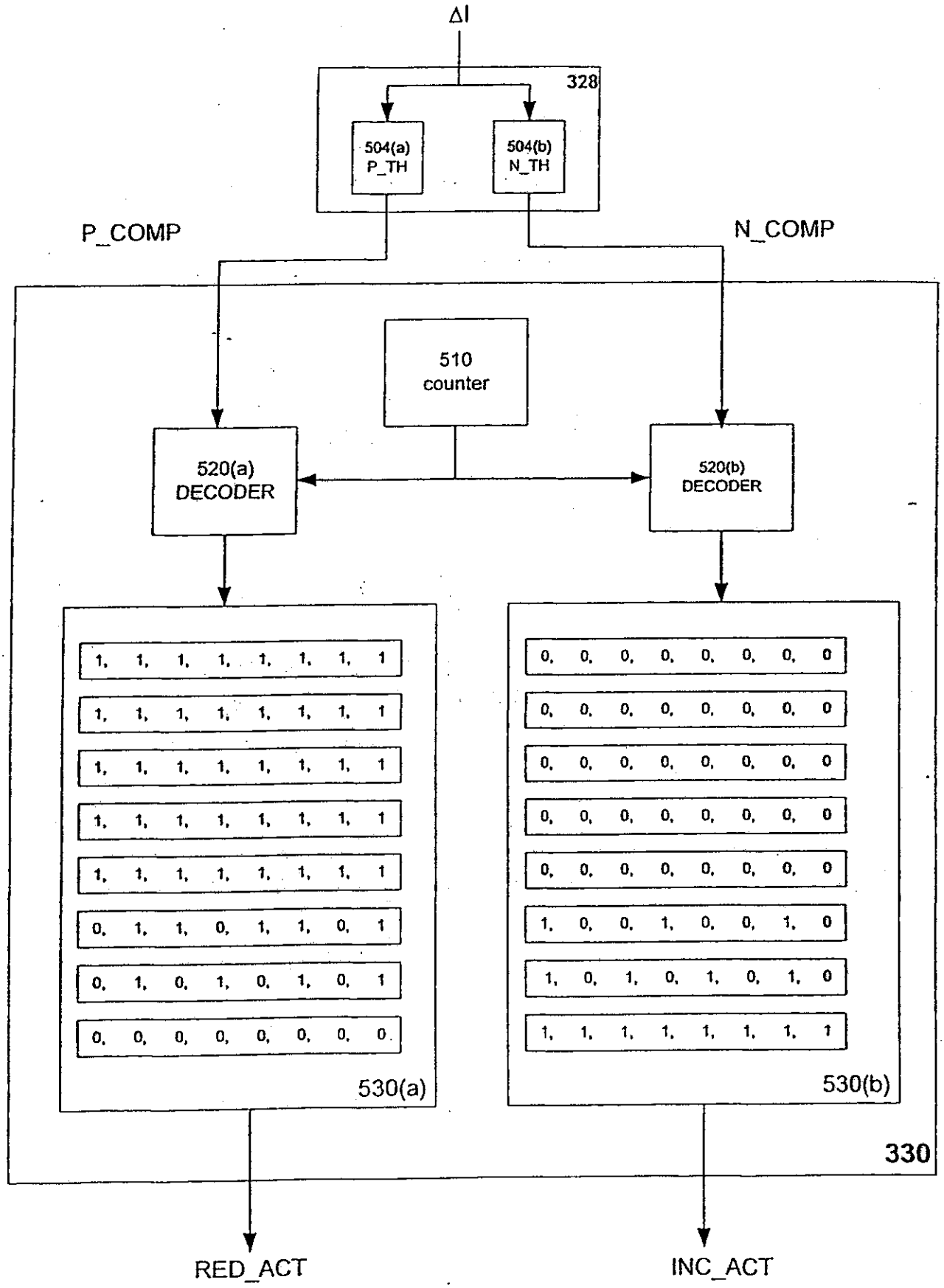

ΔI
328
504(a)
P_TH
504(b)
N_TH
P_COMP
N_COMP
510
counter
520(a)
DECODER
520(b)
DECODER
1, 1, 1, 1, 1, 1, 1, 1
1, 1, 1, 1, 1, 1, 1, 1
1, 1, 1, 1, 1, 1, 1, 1
1, 1, 1, 1, 1, 1, 1, 1
1, 1, 1, 1, 1, 1, 1, 1
0, 1, 1, 0, 1, 1, 0, 1
0, 1, 0, 1, 0, 1, 0, 1
0, 0, 0, 0, 0, 0, 0, 0
530(a)
0, 0, 0, 0, 0, 0, 0, 0
0, 0, 0, 0, 0, 0, 0, 0
0, 0, 0, 0, 0, 0, 0, 0
0, 0, 0, 0, 0, 0, 0, 0
0, 0, 0, 0, 0, 0, 0, 0
1, 0, 0, 1, 0, 0, 1, 0
1, 0, 1, 0, 1, 0, 1, 0
1, 1, 1, 1, 1, 1, 1, 1
530(b)
330
RED_ACT
INC_ACT

Fig. 5

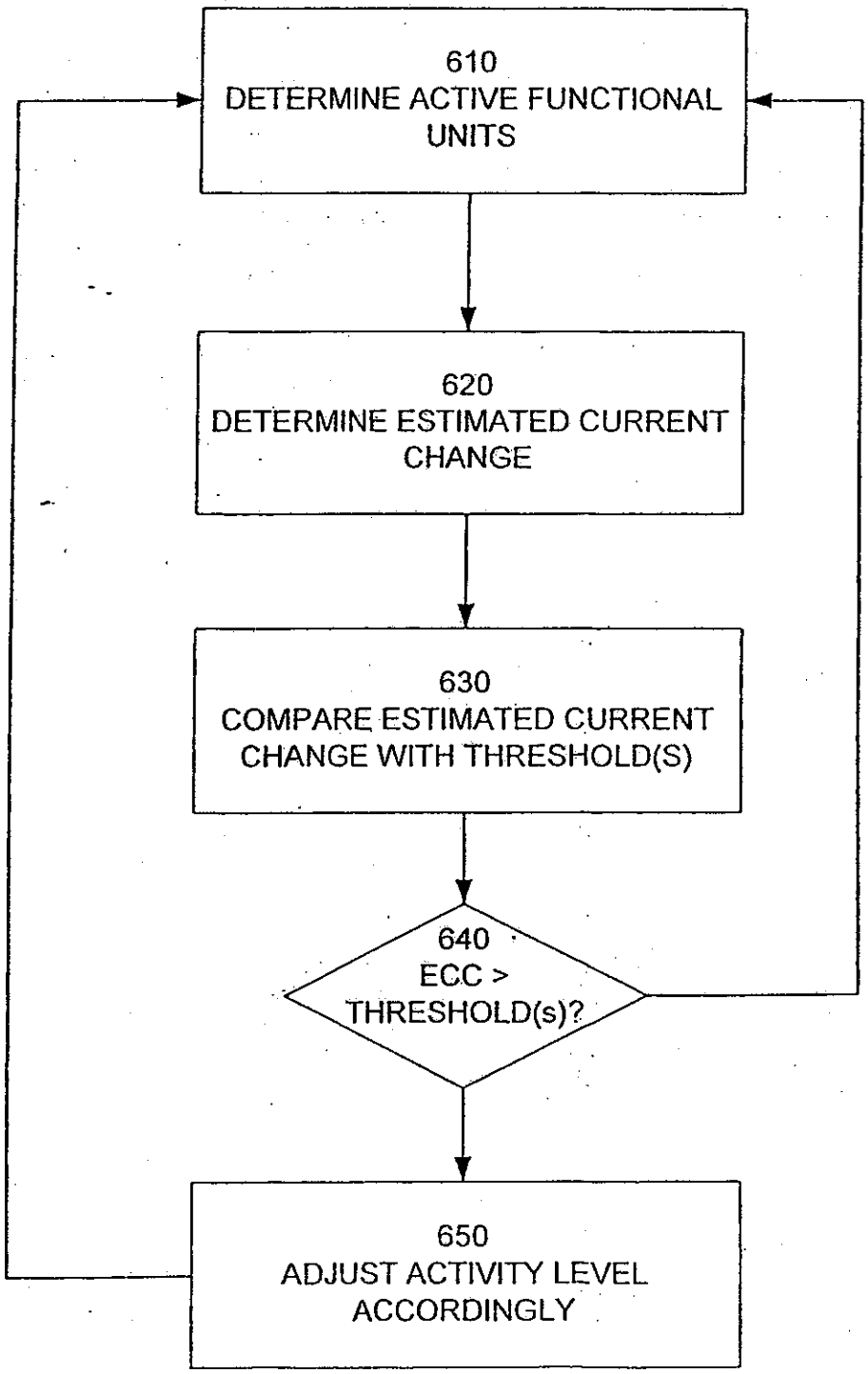

610
DETERMINE ACTIVE FUNCTIONAL UNITS
620
DETERMINE ESTIMATED CURRENT CHANGE
630
COMPARE ESTIMATED CURRENT CHANGE WITH THRESHOLD(S)
640
ECC > THRESHOLD(s)?
650
ADJUST ACTIVITY LEVEL ACCORDINGLY

Fig. 6