WHAT IS CLAIMED IS:

1. A pixel array substrate, comprising:

a plurality of scanning line pads and a plurality of data line pads located on a substrate;

a plurality of scanning lines extending along a first direction;

a plurality of data lines and a plurality of gate transmission lines extending along a second direction, wherein the data lines are electrically connected to the data line pads, and the scanning lines are electrically connected to the scanning line pads through the gate transmission lines;

a plurality of pixels located on the substrate, wherein a ratio of a number of rows of pixels arranged in the first direction to a number of rows of pixels arranged in the second direction is X:Y, wherein each of the pixels comprises m sub-pixels electrically connected to the scanning lines and the data lines, wherein each of the sub-pixels overlaps two corresponding data lines and one corresponding scanning line, and each of the scanning line pads is electrically connected to two corresponding scanning lines;

at least one data line signal chip and at least one scanning line signal chip, the at least one data line signal chip being electrically connected to the data line pads, and the at least one scanning line signal chip being electrically connected to the scanning line pads, wherein

the scanning line pads and the data line pads are arranged into a plurality of repeated units in an arrangement direction, a sum of a number of the scanning line pads and a number of the data line pads in each of the repeated units being U, wherein $U = a \times (k \times m \times X + h \times n \times Y)$, where n is a number of the at least one scanning line signal chip, and a, k, and h are positive integers.

2. The pixel array substrate according to claim 1, wherein a part of the scanning line pads and a part of the data line pads belong to a first metal layer, and the other part of the scanning line pads and the other part of the data line pads belong to a second metal layer, wherein a is 1, k is 4, and h is 1.

3. The pixel array substrate according to claim 2, wherein there are R data line pads between two adjacent scanning line pads in the arrangement direction, and $R = 2 \times m \times N$, where N is an integer between 1 and k + 1.

4. The pixel array substrate according to claim 1, wherein the scanning line pads all belong to a same metal layer, where a is 2, k is 4, and h is 1.

5. The pixel array substrate according to claim 4, wherein there are R data line pads between two adjacent scanning line pads in the arrangement direction, and $R = 2 \times m \times N + 1$, where N is an integer between 1 and k + 1.

6. The pixel array substrate according to claim 4, wherein the scanning line pads are aligned with each other in the arrangement direction.

7. A pixel array substrate, comprising:

a plurality of scanning line pads and a plurality of data line pads located on a substrate;

a plurality of scanning lines extending along a first direction;

a plurality of data lines and a plurality of gate transmission lines extending along a second direction, wherein the data lines are electrically connected to the data line pads, and the scanning lines are electrically connected to the scanning line pads through the gate transmission lines;

a plurality of pixels located on the substrate, wherein a ratio of a number of rows of pixels arranged in the first direction to a number of rows of pixels arranged in the second direction is X:Y, wherein each of the pixels comprises m sub-pixels

electrically connected to the scanning lines and the data lines, wherein each of the sub-pixels overlaps two corresponding data lines and one corresponding scanning line, and different scanning lines are not electrically connected directly through the scanning line pads or the gate transmission lines;

at least one data line signal chip and at least one scanning line signal chip, the at least one data line signal chip being electrically connected to the data line pads, and the at least one scanning line signal chip being electrically connected to the scanning line pads, wherein

the scanning line pads and the data line pads are arranged into a plurality of repeated units in an arrangement direction, a sum of a number of the scanning line pads and a number of the data line pads in each of the repeated units being U, wherein $U = a \times (k \times m \times X + h \times n \times Y)$, where n is a number of the at least one scanning line signal chip, and a is 1, k is 2, and h is 1.

8. The pixel array substrate according to claim 7, wherein there are R data line pads between two adjacent scanning line pads in the arrangement direction, and $R = 2 \times m \times N$, where N is an integer between 1 and k+1.

9. A pixel array substrate, comprising:

a plurality of scanning line pads and a plurality of data line pads located on a substrate;

a plurality of scanning lines extending along a first direction;

a plurality of data lines and a plurality of gate transmission lines extending along a second direction, wherein the data lines are electrically connected to the data line pads, and the scanning lines are electrically connected to the scanning line pads through the gate transmission lines;

a plurality of pixels located on the substrate, wherein a ratio of a number of rows of pixels arranged in the first direction to a number of rows of pixels arranged in the second direction is X:Y, wherein each of the pixels comprises m sub-pixels electrically connected to the scanning lines and the data lines, wherein each of the sub-pixels overlaps one corresponding data line and one corresponding scanning line;

at least one data line signal chip and at least one scanning line signal chip, the at least one data line signal chip being electrically connected to the data line pads, and the at least one scanning line signal chip being electrically connected to the scanning line pads, wherein

the scanning line pads and the data line pads are arranged into a plurality of repeated units in an arrangement direction, a sum of a number of the scanning line pads and a number of the data line pads in each of the repeated units being U, wherein $U = a \times (k \times m \times X + h \times n \times Y)$, where n is a number of the at least one scanning line signal chip, and a is 1, k is 1, and h is 1; and

there are R data line pads between two adjacent scanning line pads in the arrangement direction, and $R = 2 \times m \times N$, where N is an integer between 1 and $k + 1$.

10. The pixel array substrate according to any one of claims 1, 7, or 9, further comprising:

a plurality of first fan-out lines electrically connecting the scanning line pads to the gate transmission lines; and

a plurality of second fan-out lines electrically connecting the data line pads to the data lines, wherein the first fan-out lines and the second fan-out lines do not overlap each other.

11. A pixel array substrate, comprising:

a plurality of scanning line pads, a plurality of first data line pads, a plurality of second data line pads, and a plurality of third data line pads located on a substrate, wherein the scanning line pads, the first data line pads, the second data line pads, and the third data line pads are arranged in an arrangement direction;

a plurality of scanning lines extending along a first direction;

a plurality of data lines and a plurality of gate transmission lines extending along a second direction, wherein the scanning lines are electrically connected to the scanning line pads through the gate transmission lines, and the data lines are electrically connected to the first data line pads, the second data line pads, and the third data line pads;

a plurality of red sub-pixels, a plurality of green sub-pixels, and a plurality of blue sub-pixels electrically connected to the scanning lines and the data lines, wherein the red sub-pixels are electrically connected to the first data lines pads, the green sub-pixels are electrically connected to the second data line pads, and the blue sub-pixels are electrically connected to the third data line pads, wherein a number of the scanning line pads located between the first data line pads and the second data line pads or between the third data line pads and the second data line pads in the arrangement direction is less than a number of the scanning line pads located between the first data line pads and the third data line pads; and

at least one chip on film circuit comprising at least one data line signal chip, at least one scanning line signal chip, a first insulating layer, a second insulating layer, a third insulating layer, a first conductor layer, a second conductor layer, a plurality of first connection structures, a plurality of second connection structures, a plurality of third connection structures, and a plurality of fourth connection structures, wherein the at least one data line signal chip is electrically connected to the first data

line pads, the second data line pads, and the third data line pads, the at least one scanning line signal chip is electrically connected to the scanning line pads, the first insulating layer, the second insulating layer, and the third insulating layer are sequentially overlapping, the at least one data line signal chip and the at least one scanning line signal chip are located on the first insulating layer, the first conductor layer is located between the second insulating layer and the first insulating layer, the second conductor layer is located between the second insulating layer and the third insulating layer, the plurality of first connection structures penetrates through the first insulating layer and is electrically connected to the first conductor layer, the plurality of second connection structures penetrates through the first insulating layer and the second insulating layer and is electrically connected to the second conductor layer, the plurality of third connection structures penetrates through the second insulating layer and the third insulating layer and is electrically connected to the first conductor layer, the plurality of fourth connection structures penetrates through the third insulating layer and is electrically connected to the second conductor layer, the at least one data line signal chip is electrically connected to one of the first conductor layer and the second conductor layer, and the at least one scanning line signal chip is electrically connected to the other one of the first conductor layer and the second conductor layer.