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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Inverter Circuit

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a semiconductor electronic circuit. More particularly, this invention relates to an integrated inverter circuit which is fabricated from semiconductor material.

Many methods and techniques for miniaturizing electronic circuits have been proposed in the past. At first, most of the effort was spend upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on, but has nearly reached a limit. Other efforts have been made to reduce the size of electronic circuits, such as by eliminating the protective coverings from components, by using more or less conventional techniques to form the components of a complete circuit on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging therefor.

All of these methods and techniques require a very large number and variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturization by conventional techniques, fabrication requires at least the following steps:

a. Formation of the substrate
b. Preparation of the substrate
c. Application of terminations
d. Preparation of resistor material
e. Application of the resistor material
f. Heat treatment of the resistor material
g. Protection or stabilization of the resistor

Capacitors, transistors, and diodes when adapted for miniaturization each require at least as many steps in the fabrication thereof. Unfortunately, many of the steps required are not compatible. A treatment that is desirable for the protection of a resistor may damage another element formed on the same substrate, such as a capacitor or transistor, and as the size of the complete circuit is reduced, such conflicting treatments, or interactions, become of increasing importance. Interactions may be minimized by forming the components separately and then assembling them into a complete package, but the very act of assembly may cause damage to the more sensitive components.

Because of the large number of operations required, control over miniaturized circuit fabrication becomes very difficult. To illustrate, many raw materials must be evaluated and controlled, even though they may not be well understood. Further, many testing operations are required and, even though a high yield may be obtained for each operation, so many operations are required that the over-all yield is often quite low. In service, the reliability of a circuit produced by methods of such complexity may also be quite low due to the tremendous number of controls required. Additionally, the separate formation of individual components requires individual terminations for each component. These terminations may eventually becomes as

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small as a dot of conductive paint. However, they still account for a large fraction of the usable area or volume of the circuit, and may become an additional cause of circuit failure or rejection due to misalignment.

In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from a new and totally different concept for miniaturization. Semiconductor circuits or devices made in accordance therewith are the subject matter of our co-pending patent application No. 3633/60, Serial No. 945,734.

In the specification of our co-pending patent application aforesaid, a single crystal of semiconductor material exhibits one type of conductivity, either N-type or P-type, and certain regions thereof are processed so as to form certain kinds of circuit components such as diodes and transistors. Other regions of the basic semiconductor crystal may inherently perform functions of certain other circuit components such as resistors. In the present invention all components of a transistor inverter circuit may be fabricated in and/or on a body of semiconductor material by utilizing the techniques described in the specification of said co-pending patent application, together with certain other techniques. All components of this inverter circuit may be integrated with the main body of semiconductor material and actually constitute portions thereof.

An object of the present invention is to provide a novel semiconductor network which functions as a transistor inverter circuit.

The present invention is a semiconductor inverter circuit comprising a substrate, semiconductor portions in or on one face of said substrate, said portions including first, second, third, fourth and fifth portions, said first portion defining a transistor having a base region, an emitter region and a collector region, said second portion defining a load resistor, one end of said load resistor being ohmically connected to said collector region, said third portion defining a diode comprised of a region of P-type conductivity and a region of N-type conductivity, said fourth and fifth portions defining resistors, each of said resistors having one end thereof ohmically connected to one of the regions of said diode, and means completing the electrical interconnection of said portions as an inverter circuit including an electrical lead secured to a surface of one of said portions, which surface is remote from said substrate.

The concept of shaping described in detail in said co-pending patent application makes it possible in a circuit to obtain the necessary isolation between components and to define the components or, stated differently, to limit the area which is utilized in a given component. Shaping may be accomplished in a given circuit in one or more of several different ways. These various ways include actual removal of portions of the semiconductor material, specialized configuration of the semiconductor material such as rectangles, "L" shapes, "U" shapes, etc., selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow, and selective conversion of semiconductor material of one conductivity type to conductivity of the opposite type wherein the P-N junction thereby formed acts as a barrier to current flow. In any event, the effect of shaping is to direct and/or confine paths for current flow, thus permitting the fabrication of circuits which could not otherwise be obtained in a single wafer of semiconductor material. As a result, the final circuit is arranged in essentially planar form. It is possible to shape the wafer during processing and to produce by diffusion the various circuit elements in a desired and proper relationship.

Other and further objects of the present invention will become more readily apparent from the following detailed description of a preferred embodiment of the present invention when taken in conjunction with the accompanying drawings in which:

Fig. 1 is a conventional schematic diagram of the inverter circuit which is to be fabricated within a body of semiconductor material in accordance with the present invention;

Fig. 2 illustrates the inverter circuit of the present invention; and

Figs. 3 and 4 are exaggerated cross sectional views of portions of the inverter circuit shown in Fig. 2.

Referring now to Fig. 1, there is shown a conventional schematic diagram of the electrical inverter circuit which is fabricated from semiconductor material. The active elemnt T_1 is a N-P-N transistor having its collector 12 connected to a load resistor R_1 which, in turn, is connected to a source of positive potential. Emitter 14 is connected to another source of positive potential, as shown. Base 16 of transistor T_1 is connected to one terminal of resistor R_4, the other terminal of which is connected to a low negative potential. Base 16 is also connected to the cathode 17 of diode D_1 and to one terminal of resistor R_2. The other terminal of R_2 is connected to one terminal of R_3 which, in turn, may be further selectively connected to a positive potential, depending upon which of the two input leads I_1 or I_2 is to receive a signal. If input lead I_2 is to receive a positive signal, the

resistor R_3 is not connected to a positive potential. This results in base 16 of transistor T_1 being normally biased negatively with respect to emitter 14. In the absence of a positive signal at I_2 no current flows in the collector 12 circuit and, thus, the OUT lead from collector 12 is at a relatively high potential. When a positive signal is applied at I_2 to the anode 15 of diode D_1, the potential of base 16 becomes positive with respect to emitter 14 so that the voltage at the OUT lead drops and, thus, inverts the applied signal. No signals are applied to I_1 when I_2 is being used as the input. However, when it is desired to use input lead I_1, lead I_2 is not used and resistor R_3 is connected to a positive potential. The values of R_3, R_2 and R_4 are such that this normally results in potential of base 16 being higher than potential of emitter 14 so that the collector voltage is low until an appropriate negative signal is applied at input I_1. Upon the receipt of such a signal, transistor T_1 is turned off and the collector voltage rises, thus inverting the input signal.

Both the passive and active components of the circuit, as defined in our co-pending application, shown in Fig. 1 are embodied or integrated within portions of a body of semiconductor material, as shown in Fig. 2. A glass or ceramic substrate 18 is provided to support the semiconductor material used in fabricating the circuit of Fig. 1. The manner in which the semiconductor material may be supported or attached to the substrate is disclosed in the application for patent No. 16070/60 (Serial No. 958,241) filed 6th May, 1960.

Two associated portions of an N-type semiconductor material in the form of wafer strips 20 and 22 are formed on substrate 18. Each wafer strip 20 and 22 is shaped and regions of its surface processed so as to include therein several of the circuit components found in Fig. 1. The regions of each wafer 20 and 22 have been marked with symbols representative of the circuit element functions that are performed therein which correspond to the components found in Fig. 1. Metal contact strips 26, 28, 30, 32, 34, 36, and 38 are also attached to the substrate material 18 so as to provide input and output connectors for the bias voltages and signals shown in Fig. 1. For example, contact strip 26 corresponds to input lead I_2 in Fig. 1 so as to apply a signal thereon to diode D_1 which is formed within a region of wafer 20, as will subsequently be described. It will be noted that the end portions of contact strips 30, 32, 34, 36, and 38 are positioned in physical contact beneath various regions of wafers 20, and 22 and so make ohmic connections thereto. However, contact strips 26 and 28 do not extend beneath the wafer strips, but rather are connected to specific components which are fabricated within certain regions of these two wafers. Contact strip 24 is similar in nature to the other above described contact strips 30-38, except that it is not used to introduce or remove signals from the circuit formed on substrate 18. It corresponds to the junction of base 16, resistor R_4, cathode 17 of D_1, and resistor R_3 which is shown in Fig. 1. However, it makes ohmic contact with a region of wafer 20, and is utilized as a terminal post and test point within the circuits, as will later be explained.

The construction and function of wafer 22 in Fig. 2 will now be explained with particular reference to Fig. 3. Wafer 22 may be formed in the shape of "L", as shown, and is processed so as to include therein regions providing the functions of resistor R_1 and transistor T_1 shown in Fig. 1. Wafer 22 is so designed that the sum of the effective bulk resistances of its horizontal and vertical legs is equal to the desired value of resistance R_1. The resistance may be calculated from the following equation:

$$P = \rho L/A,$$

where L is the sum of the active leg lengths in centimeters. A is the cross-sectional area of the wafer strip, and ρ is the resistivity in ohm-centimeters of the N-type semiconductor material in the wafer strip. Transistor T_1 is formed or fabricated at the left-hand end of the horizontal leg of wafer 22. The construction of transistor T_1 is more readily discerned from Fig. 3, which is a cross sectional view taken of this left-hand region of wafer 22. As shown, a small amount 48 of P-type semiconductor material is formed on top of the N-type semiconductor material of this region of wafer 22 in any well known manner so as to form a rectifying P-N junction therebetween. Another amount 46 of N-type semiconductor material is formed on top of P-region 48 so as to create a rectifying P-N junction therebetween. Regions 46, 48, and the left-hand region of wafer 22 thus form an N-P-N transistor at this region of wafer 22. Furthermore, in the particular embodiment as shown, N-region 46 is taken to be the emitter region, while the left-hand region of wafer 22 is considered to be the collector region of the above-identified transistor. A metal emitter electrode 14 is attached to region 46 in a well known manner so as to form an ohmic contact thereto. Furthermore, a metal base electrode 16 is alloyed through region 46 so as to make an ohmic contact with the base region 48. The junction between contact 16 and region 46 may be etched away if desired so as effectively to insulate 16 from 46. Contact strip 38 makes ohmic

connections with the N-wafer 22 at the regions shown in Figs. 2 and 3, whereas strip 32 makes ohmic contact as is shown in Figure 2 only.

The different regions of wafer strip 20 and the circuit components fabricated therein will now be described with particular reference to Fig. 4. Wafer 20 is composed of N-type semiconductor material similar to that of wafer 22. The upper horizontal leg of wafer 20 is of such a length and cross sectional area as to provide the desired resistance for resistor R_4 shown in Fig. 1. The lower horizontal leg of wafer 20 in like manner corresponds to resistor R_3, while the single vertical leg corresponds to resistor R_2. The diode D_1 is fabricated in the region found at the intersection of the upper horizontal and vertical legs. Fig. 4 is a cross sectional view taken of this diode region. As shown in Fig. 4, an amount 50 of P-type semiconductor material is formed at the above-described region of wafer 20 in such a manner as to form a rectifying P-N junction therebetween. A metal contact 15 is ohmically connected to P-region 50. The processing of the original wafer 20 thus results in a diode D_1 being formed whose anode is region 50 and whose cathode is a region of the wafer 20. Contact strips 24, 30, 34, and 36 make ohmic connections with wafer 20 at the regions shown in Fig. 2.

It has thus been described how wafer strip 22 has regions contained therein which perform the functions of resistance R_1 and transistor T_1, while wafer strip 20 has regions therein which perform the functions of resistors R_2, R_3, R_4, and diode D_1. It now remains to effectively connect the two wafer strips 20 and 22 together so as to form the complete inverter circuit. These final connections are made by ohmic leads 40, 42, and 44. Emitter contact 14 of transistor T_1 is connected to contact strip 28 by lead 44. Base contact 16 of T_1 is connected by lead 42 to contact strip 24 which, in turn, makes ohmic contact with the upper left-hand region of wafer 20. Anode contact 15 of diode D_1 is connected to contact strip 26 by lead 40.

The functioning of the inverter circuit which is fabricated within the semiconductor wafers 20 and 22 will now be described in order to aid in the understanding of its construction. Assuming that input lead I_2 is being utilized, the proper bias voltages corresponding to those shown in Fig. 1 will be connected to contact strips 28, 30, and 32. A positive potential on contact strip 32 is applied to the lower left-hand region of wafer 22, which corresponds to the collector electrode 12 of transistor T_1, through the vertical and horizontal legs of wafer 22 which correspond to resistance R_1. Contact strip 38 is also connected to this region of wafer 22 so as to indicate the potential at the collector. A negative bias on contact strip 30 is applied to the upper left-hand region of wafer 20 through the upper horizontal leg of wafer 20 which corresponds to resistance R_4. Since contact strip 24 is ohmically connected to this upper left-hand region of wafer 20, it is seen that the base electrode 16 of transistor T_1 in wafer 22 is therefore connected by lead 42 to one terminal of resistor R_4, such as indicated in Fig. 1. Furthermore, this upper left-hand region of wafer 20 is also utilized as the cathode 17 of diode D_1, and it is further seen that strip 26 provides an ohmic connection to the anode 15 of diode D_1 to which is applied a signal at input I_2. As before explained, since input I_2 is being utilized, no bias is applied to contact strip 36 so that the lower horizontal leg and vertical leg of wafer 20 are not made effective and can be disregarded. Therefore, a positive signal which is introduced at I_2 will cause the potential on contact strip 38 to fall in accordance with the previously described operation of Fig. 1. However, if input I_1 is to be used, then a positive potential is applied to contact strip 36 and, thence, to the upper left-hand region of wafer 20 through its lower horizontal leg and vertical leg, which correspond to resistors R_3 and R_2 respectively. Contact strip 34 is connected to the region of wafer 20 which is formed at the junction of the lower horizontal and vertical legs. Thus, a signal at I_1 enters the inverter circuit between resistors R_3 and R_2.

Techniques suitable for processing the wafers 20 and 22 so as to fabricate circuit components therein have been fully described in the afore-mentioned co-pending patent application No. 3633/60 (Serial No. 945734). For example, in order to fabricate the transistor T_1 in wafer 22, diffusion or other processes may be used in forming the P-N junctions between regions 48 and 22 and 46 and 48, after which the desired area of these regions may be shaped by means of an etching process. Furthermore, the formation of the wafer strips 20 and 22 may be accomplished by initially placing a single body of N-type semiconductor material onto the substrate 18 and thereafter etching away portions thereof so as to form the desired shape of the wafers. This etching also divides the original single body of N-type semicondutcor material into several bodies, or wafers, which are thus effectively insulated from each other so as to prevent short circuits between components. However it is conceivable that the inverter circuit could be fabricated within a single body if the resistance of certain current paths were made so great as to effectively create open

circuits. The "L" and "U" shapes of the wafers in Fig. 2 provide compactness.

Although the invention has been shown and described in terms of an inverter circuit utilizing an N-P-N transistor, it will be evident that such a circuit could be fabricated within semiconductor material which employed a P-N-P transistor or other transistors. It will, thus, be evident that such changes and modifications are deemed to fall within the scope of the invention, as defined in the appended claims.

Thus, for example, since it is known that intrinsic semiconductor material is characterized by a relatively high order of resistivity, the substrate could be formed thereof; or, the entire unit could be formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the regions occupied by the cut wafers in the drawing.

According to this arrangement, member 18 of Fig. 2 would be either a separate block of intrinsic material on which wafers 20 and 22 were mounted, or it would be part of the same physical piece of semiconductor material as areas 20 and 22, the latter differing therefrom only in electrical characteristics due to impurity doping.

Among the advantages of the present invention are that it provides semiconductor transistor inverter circuit which may be fabricated from a body of semiconductor material which contains at least two P-N junctions and wherein all components of the inverter may be fabricated completely within the body of semiconductor material, a transistor inverter circuit structure which is substantially smaller and more compact than are circuit packages heretofore developed using known techniques, a transistor inverter circuit structure in which a transistor and its output load may be formed within one portion of a body of semiconductor material while the input circuit to said transistor may be formed within another portion of the body of semiconductor material.

WHAT WE CLAIM IS:—

1. A semiconductor inverter circuit comprising a substrate, semiconductor portions in or on one face of said substrate, said portions including first, second, third, fourth and fifth portions, said first portion defining a transistor having a base region, an emitter region and a collector region, said second portion defining a load resistor, one end of said load resistor being ohmically connected to said collector region, said third portion defining a diode comprised of a region of P-type conductivity and a region of N-type conductivity, said fourth and fifth portions defining resistors, each of said resistors having one end thereof ohmically connected to one of the regions of said diode, and means completing the electrical interconnections of said portions as an inverter circuit including an electrical lead secured to a surface of one of said portions, which surface is remote from said substrate.

2. An inverter circuit according to claim 1, in which said substrate is semiconductor material.

3. An inverter circuit according to claim 1, wherein said semiconductor portions include a sixth portion defining a resistor, and one end of said last mentioned resistor being ohmically connected to the other end of one of said resistors.

4. An inverter circuit according to any preceding claim, wherein said one end of said resistors is ohmically connected to said base region.

5. A semiconductor inverter circuit substantially as described herein with reference to Figs. 2 to 4 of the accompanying drawings.

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