ABSTRACT

Provided are a semiconductor chip with a reduced thickness and improved reliability, and a semiconductor package including the semiconductor chip. The semiconductor chip includes a semiconductor substrate, an integrated device layer on the semiconductor substrate, a multi-wiring layer on the integrated device layer, and a pad metal layer of a plurality of pad metal layers on the multi-wiring layer, and having test pads defined therein. The pad metal layers extend in a first direction parallel to a top surface of the semiconductor substrate or in a second direction perpendicular to the first direction. A test pad is a central portion of the pad metal layer and, and an outer portion of the pad metal layer excluding the test pad overlaps the wires in a third direction perpendicular to the top surface of the semiconductor substrate.

FIG. 1C