ABSTRACT OF THE DISCLOSURE

A SELF ALIGNED CHANNEL DOPING METHOD FOR HIGH SPEED MOS TRANSISTORS

A method of self aligned lightly doped drain/halo doping for suppressing leakage current while avoiding increased junction capacitance in metal oxide semiconductor field effect transistors having sub micron channel lengths. A gate window is formed in a dielectric layer and spacers are formed on the sidewalls of the gate window. After formation of the gate electrode the spacers are etched away and lightly doped drain regions are formed using ion implantation through the openings formed by etching away the spacers. This provides relatively heavy doping concentrations only in the lightly doped drain regions and avoids the increase of junction capacitance.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)