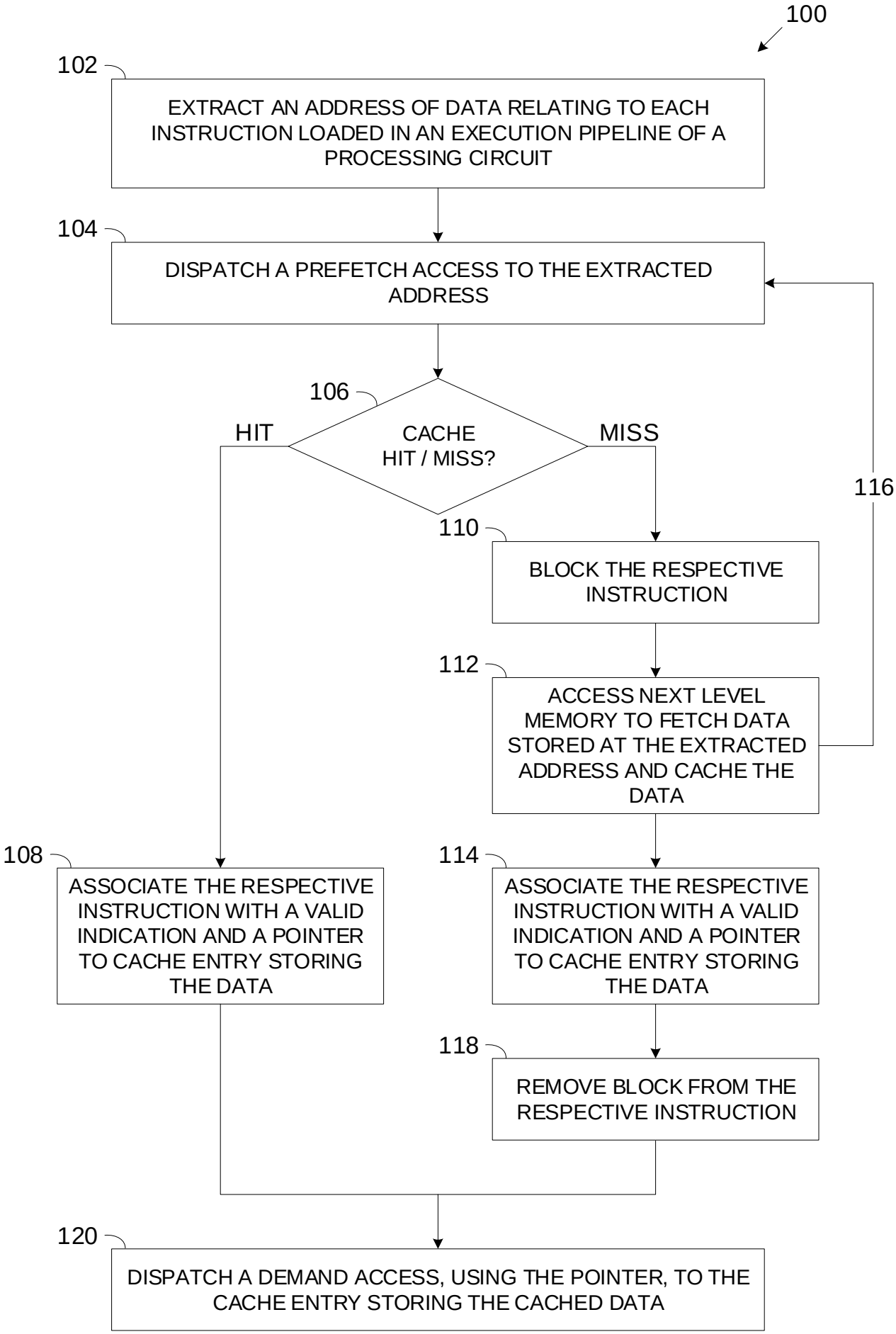

100
102
EXTRACT AN ADDRESS OF DATA RELATING TO EACH INSTRUCTION LOADED IN AN EXECUTION PIPELINE OF A PROCESSING CIRCUIT
104
DISPATCH A PREFETCH ACCESS TO THE EXTRACTED ADDRESS
106
CACHE HIT / MISS?
HIT
MISS
116
110
BLOCK THE RESPECTIVE INSTRUCTION
112
ACCESS NEXT LEVEL MEMORY TO FETCH DATA STORED AT THE EXTRACTED ADDRESS AND CACHE THE DATA
108
ASSOCIATE THE RESPECTIVE INSTRUCTION WITH A VALID INDICATION AND A POINTER TO CACHE ENTRY STORING THE DATA
114
ASSOCIATE THE RESPECTIVE INSTRUCTION WITH A VALID INDICATION AND A POINTER TO CACHE ENTRY STORING THE DATA
118
REMOVE BLOCK FROM THE RESPECTIVE INSTRUCTION
120
DISPATCH A DEMAND ACCESS, USING THE POINTER, TO THE CACHE ENTRY STORING THE CACHED DATA

FIG. 1

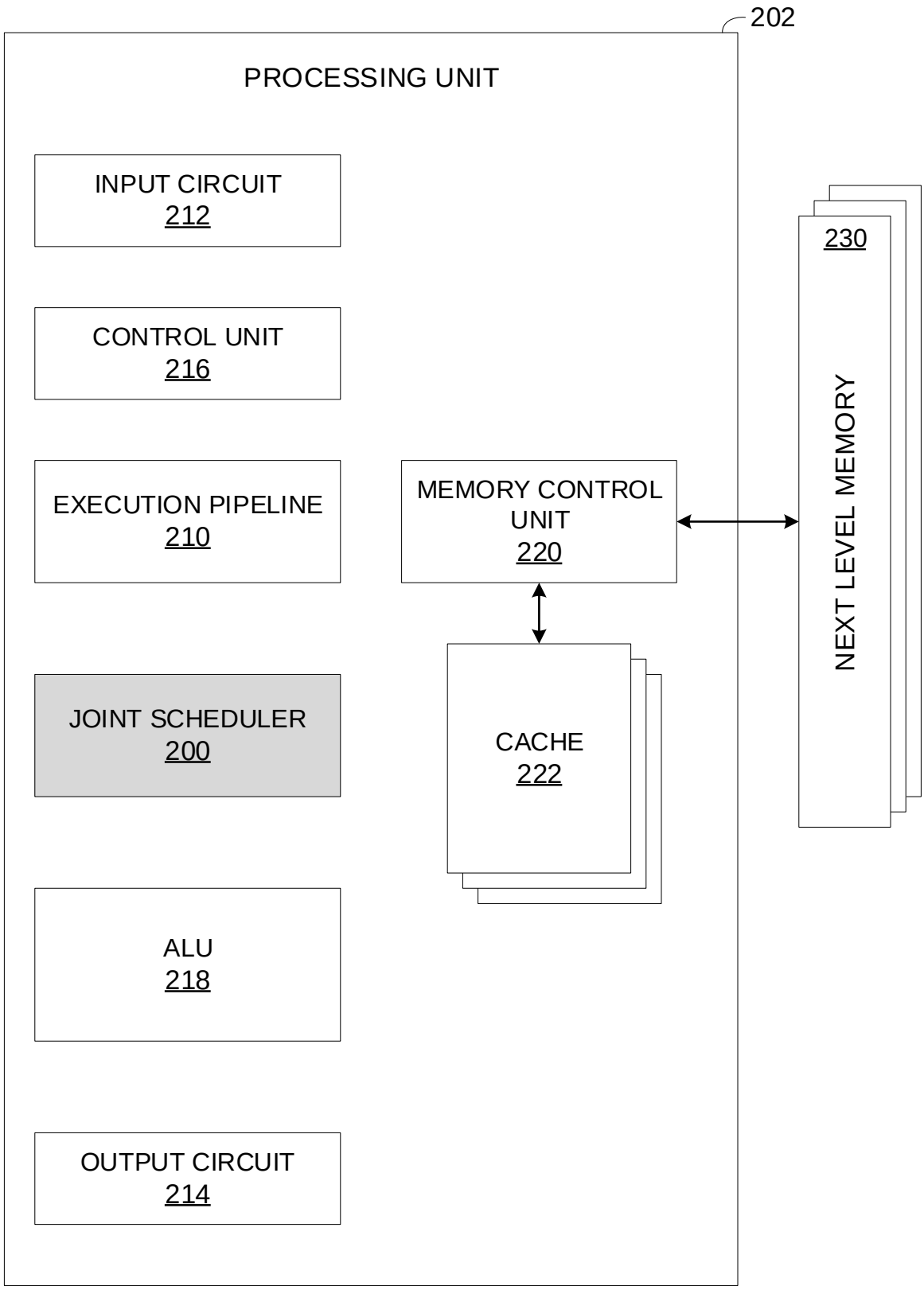

202
PROCESSING UNIT
INPUT CIRCUIT
212
CONTROL UNIT
216
EXECUTION PIPELINE
210
JOINT SCHEDULER
200
ALU
218
OUTPUT CIRCUIT
214
MEMORY CONTROL UNIT
220
CACHE
222
230
NEXT LEVEL MEMORY

FIG. 2A

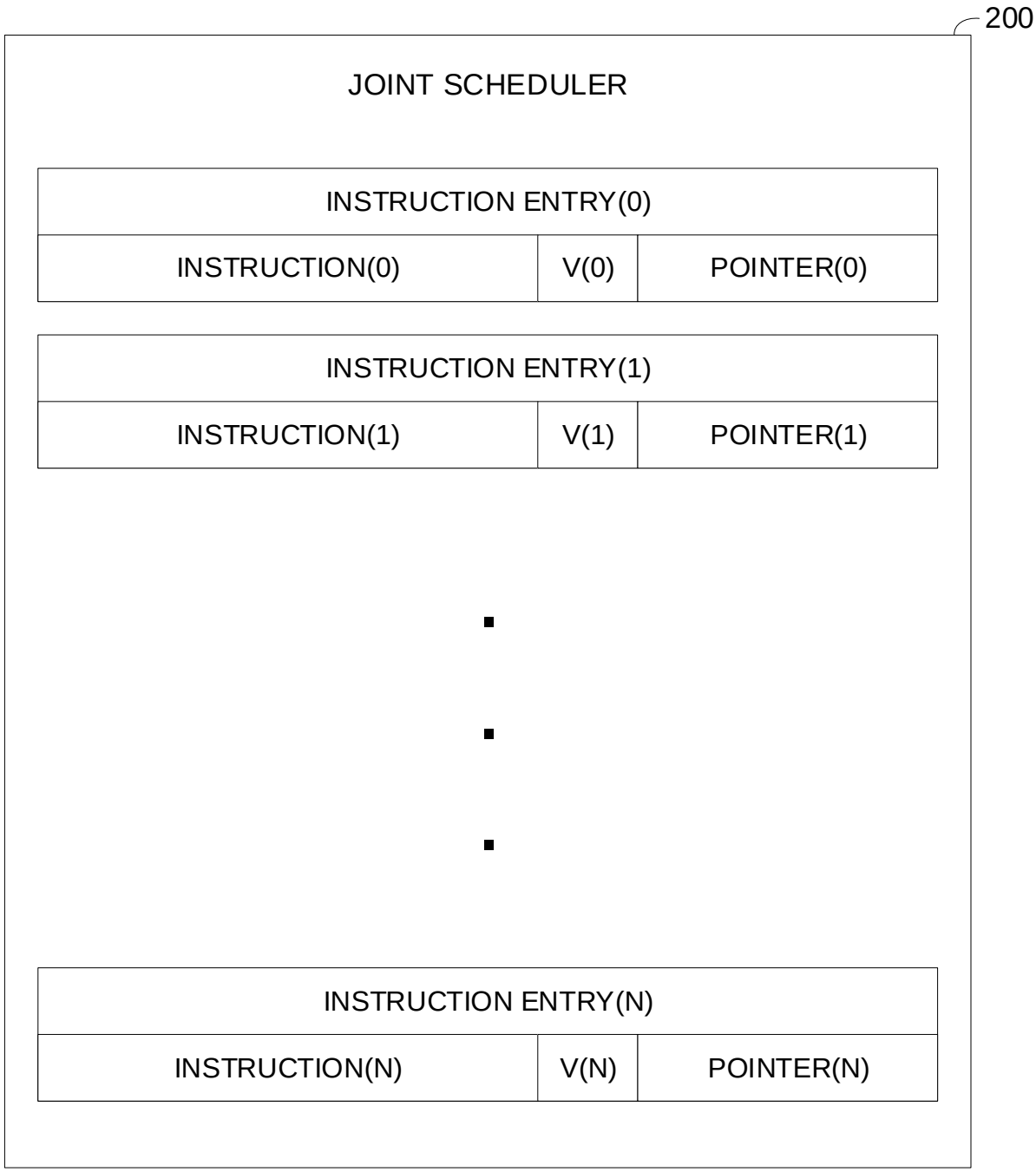

200
JOINT SCHEDULER
INSTRUCTION ENTRY(0)
INSTRUCTION(0)
V(0)
POINTER(0)
INSTRUCTION ENTRY(1)
INSTRUCTION(1)
V(1)
POINTER(1)
INSTRUCTION ENTRY(N)
INSTRUCTION(N)
V(N)
POINTER(N)

FIG. 2B

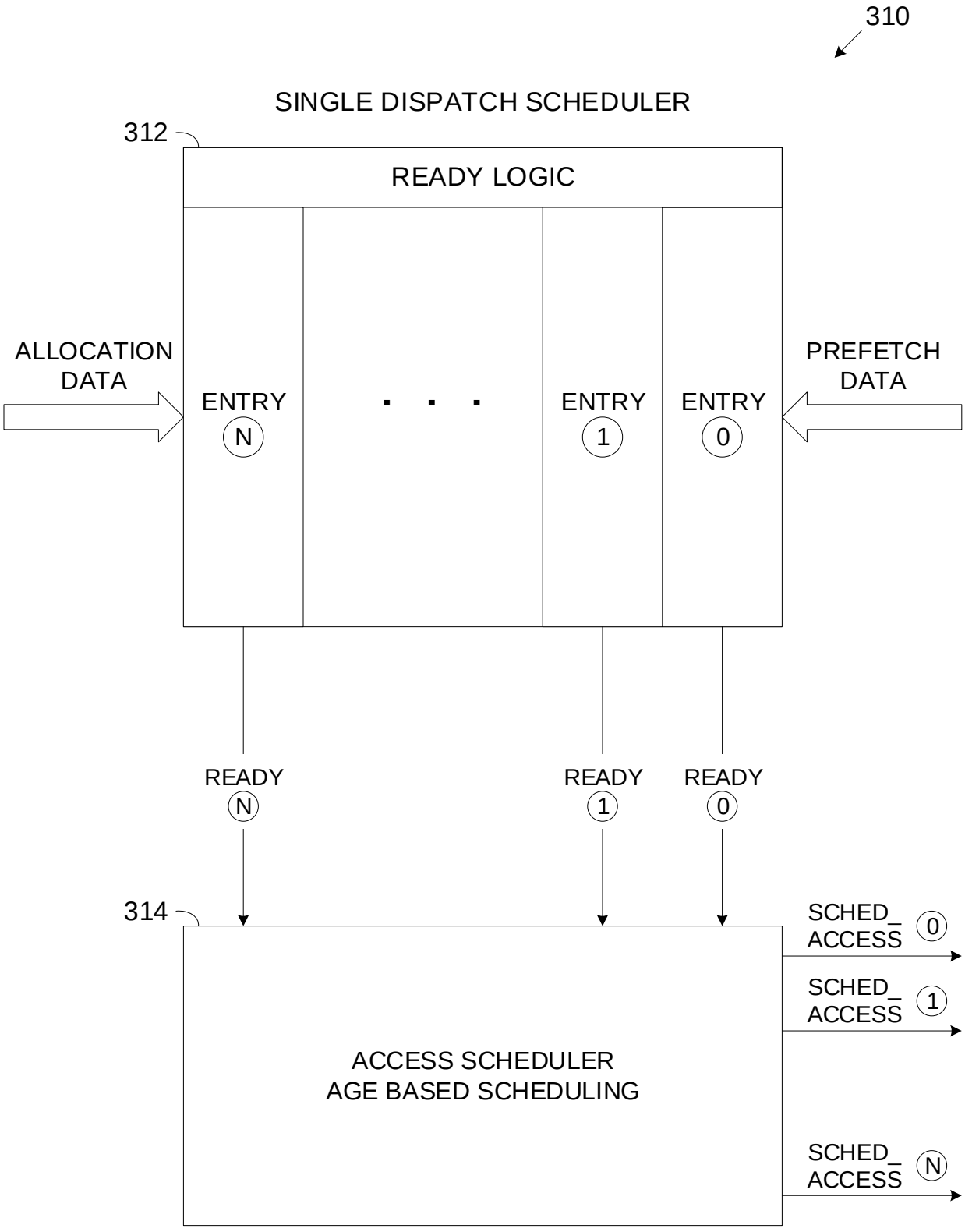

310
SINGLE DISPATCH SCHEDULER
312
READY LOGIC
ALLOCATION DATA
PREFETCH DATA
ENTRY N
ENTRY 1
ENTRY 0
READY N
READY 1
READY 0
314
ACCESS SCHEDULER
AGE BASED SCHEDULING
SCHED_ ACCESS 0
SCHED_ ACCESS 1
SCHED_ ACCESS N

FIG. 3A

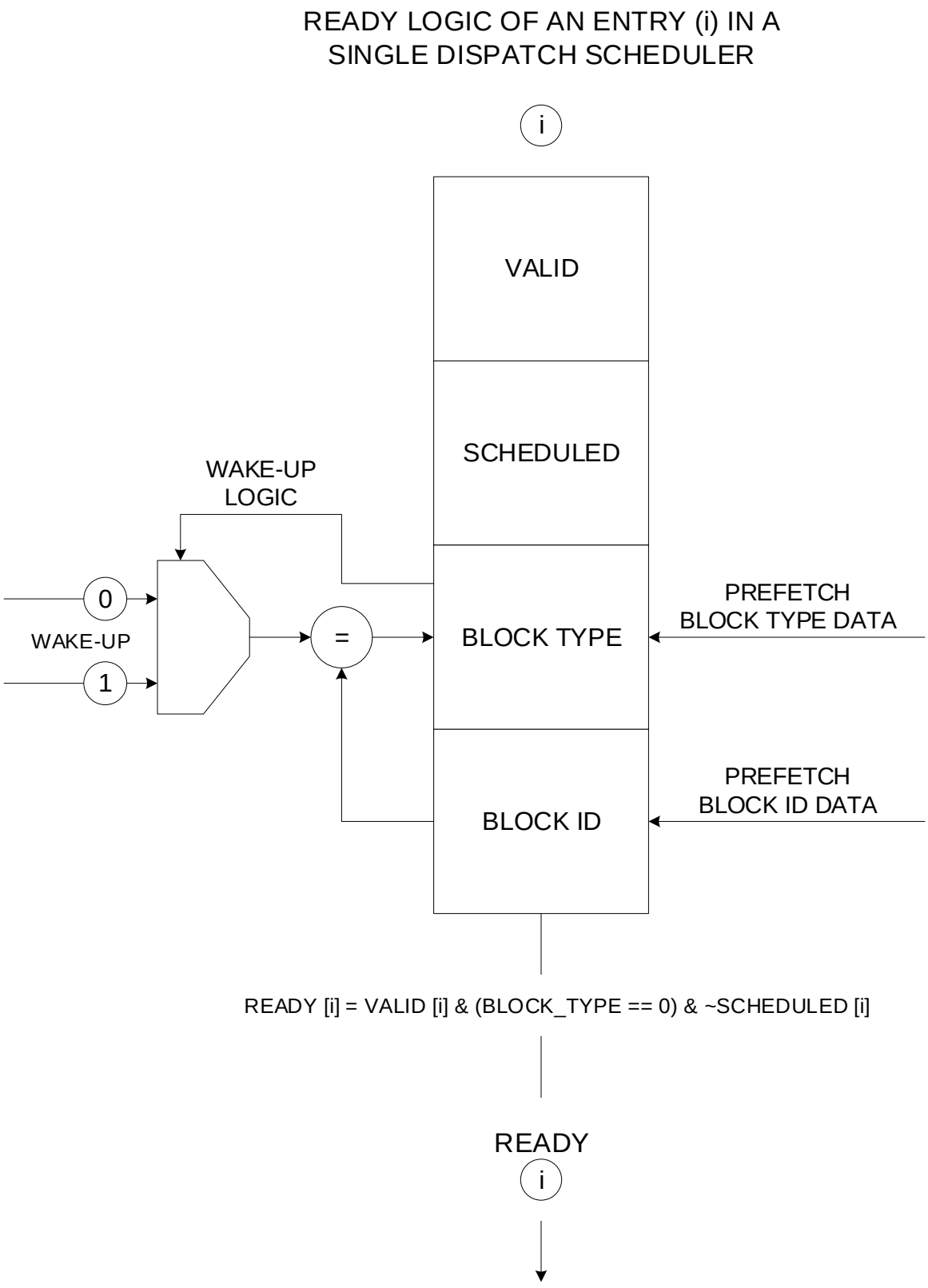

READY LOGIC OF AN ENTRY (i) IN A
SINGLE DISPATCH SCHEDULER
i
VALID
SCHEDULED
WAKE-UP
LOGIC
0
WAKE-UP
1
=
BLOCK TYPE
PREFETCH
BLOCK TYPE DATA
BLOCK ID
PREFETCH
BLOCK ID DATA
READY [i] = VALID [i] & (BLOCK_TYPE == 0) & ~SCHEDULED [i]
READY
i

FIG. 3B

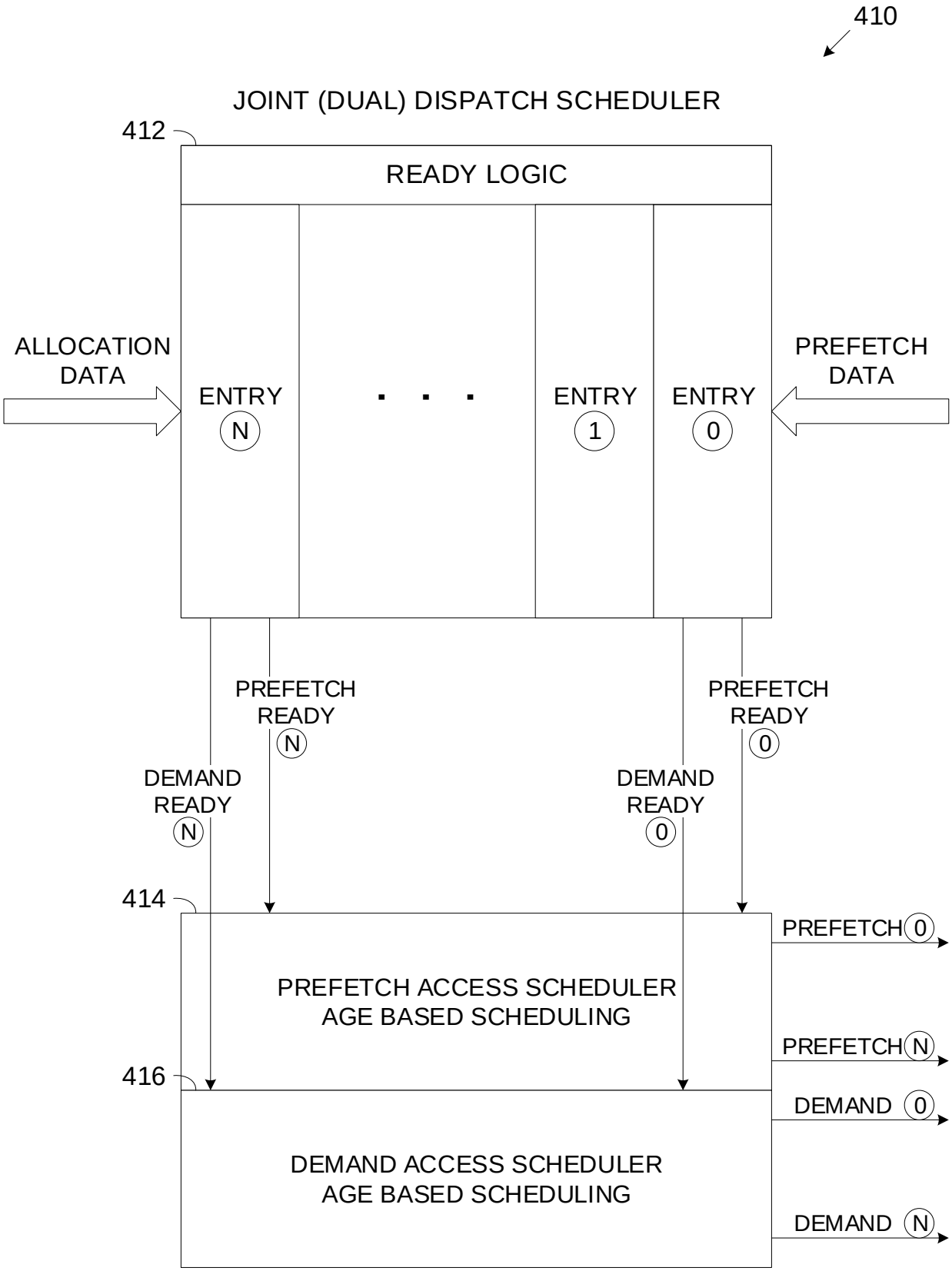

410
JOINT (DUAL) DISPATCH SCHEDULER
412
READY LOGIC
ALLOCATION DATA
PREFETCH DATA
ENTRY N
ENTRY 1
ENTRY 0
PREFETCH READY N
PREFETCH READY 0
DEMAND READY N
DEMAND READY 0
414
PREFETCH ACCESS SCHEDULER
AGE BASED SCHEDULING
416
DEMAND ACCESS SCHEDULER
AGE BASED SCHEDULING
PREFETCH 0
PREFETCH N
DEMAND 0
DEMAND N

FIG. 4A

DUAL READY LOGIC OF AN ENTRY (i) IN
A DUAL DISPATCH SCHEDULER

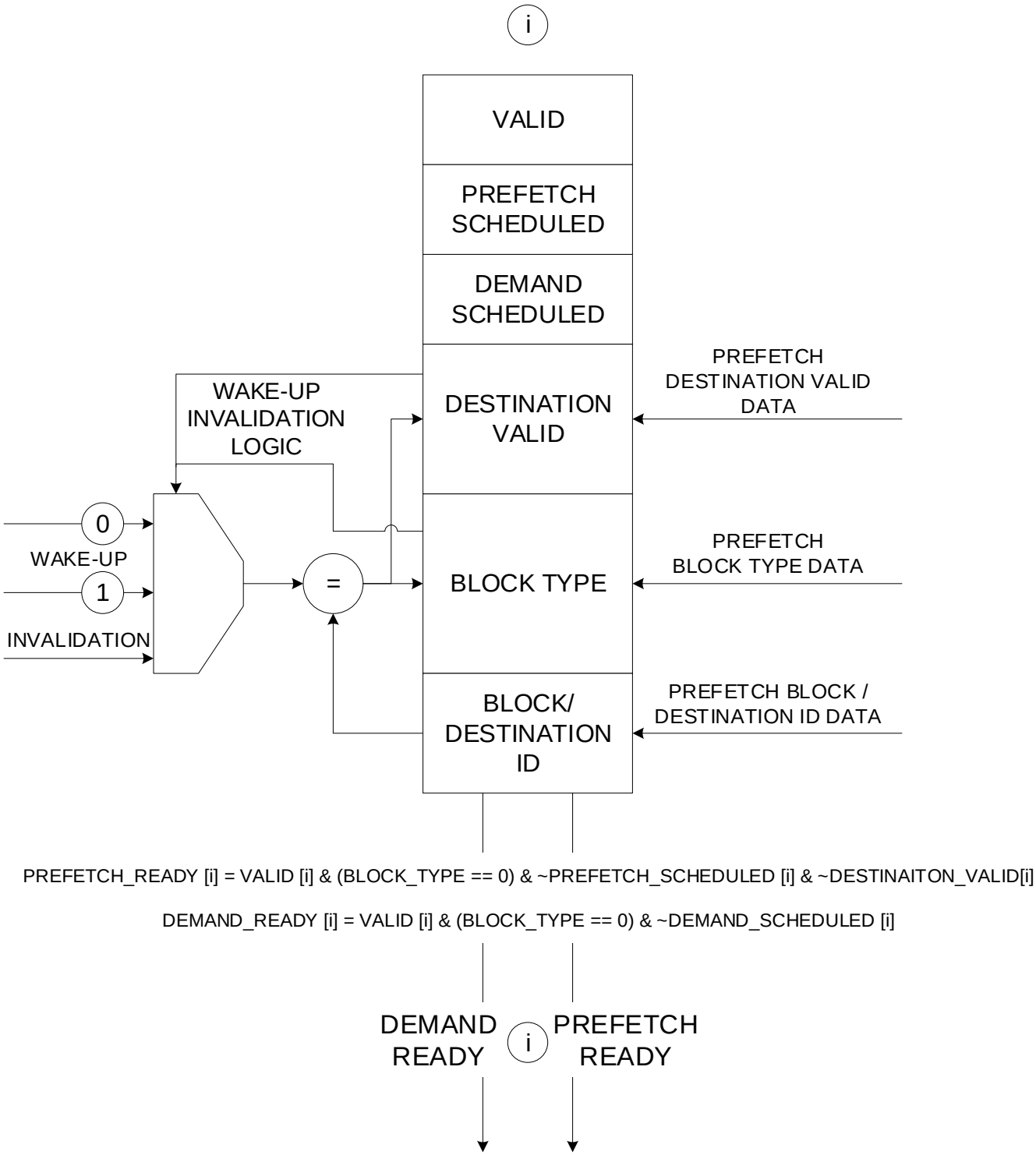


FIG. 4B