What is claimed is:

1. A layered structure comprising:

a starting material layer that comprises a material having resistivity in a range of 0.1 to 10 ohm-cm; and

a fully depleted porous layer directly on the starting material layer,

wherein a first band gap of the fully depleted porous layer is greater than a second band gap of the starting material and the fully depleted porous layer is elementally identical to the starting material.

2. The layered structure of claim 1, wherein the fully depleted porous layer is between 10-20μm thick with resistivity greater than 10000 ohm-cm.

3. The layered structure of claim 1, wherein the starting material comprises silicon.

4. The layered structure of claim 1, the starting material comprises a plurality of layers stacked vertically, wherein a resistivity of the plurality of layers of the starting material varies.

5. The layered structure of claim 1, wherein the starting material layer is a silicon substrate with a <111> or <100> crystal orientation.

6. The layered structure of claim 1, wherein the fully depleted porous layer comprises a first porosity in a first region and a second porosity in a second region.

7. The layered structure of claim 1, wherein the fully depleted porous layer is lattice matched to the starting material.

8. The layered structure of claim 6, wherein the fully depleted porous layer comprises a plurality of sublayers stacked vertically, wherein

a porosity of the plurality of sublayers is graded with a sublayer with a low porosity at a surface of the fully depleted porous layer, and a sublayer with a high porosity at an interface of the fully depleted porous layer and the starting material.

9. The layered structure of claim 6, wherein the fully depleted porous layer comprises periodically alternating sublayers of the first porosity and the second porosity, the first porosity and the second porosity being different from each other.

10. The layered structure of claim 9, wherein the first porosity is a high porosity, and the second porosity is a low porosity.

11. The layered structure of claim 9, wherein the periodically alternating sublayers of the first porosity and the second porosity form an acoustic reflector, or a coherent phonon structure.

12. The layered structure of claim 1, wherein a thermal conductivity is at least equal to 3 W/mK.

13. The layered structure of claim 1, wherein the permittivity is in a range of approximately 2 to 4 farads per meter.

14. A layered structure of any preceding claim further comprising:
an epitaxial layer grown over the fully depleted porous layer.

15. The layered structure of claim 14, wherein the epitaxial layer is a silicon semiconductor layer.

16. The layered structure of claim 14, wherein the epitaxial layer is selected from the group consisting of a InP layer, a cREO layer, a Mo layer, a AlGaInN layer, a RE-III-N layer and a metal layer.

17. The layered structure of claim 14, wherein the layered structure is a layer of an RF switch structure; a layer of an integrated passive device; or a layer in an RF filter.

18. The layered structure of claim 14, wherein the starting material comprises a first region having a first resistivity and a second region having a second resistivity.

19. The layered structure of claim 18, wherein:

the fully depleted porous layer is formed over the first region; and

the layered structure further comprises a non-fully depleted porous layer formed over the second region.

20. A method of forming a layered structure, the method comprising:

forming a fully depleted porous layer converted from a starting material,

wherein the starting material is a p-type, boron doped substrate having a resistivity in the range of 0.1 to 10 ohm-cm,

wherein a first band gap of the fully depleted porous layer is greater than a second band gap of the starting material and the fully depleted porous layer is elementally identical to the starting material.

21. The method of claim 20, further comprising:

growing an epitaxial layer over the fully depleted porous layer.

22. The method of claim 20, wherein the starting material is a silicon substrate with a <111> or <100> crystal orientation.