

CLOCK EXTRACTION DEVICE WITH DIGITAL PHASE LOCK,
REQUIRING NO EXTERNAL CONTROL

The invention relates to a clock-extraction device, and more particularly a device for clock extraction and for extraction of digital data from a baseband serial signal, known as the received signal, that is representative of digital data and coded with a clock signal exhibiting a clock-bit frequency f_{sr} corresponding at least substantially to a nominal frequency f_n .

In numerous applications, and in particular in the field of very high frequencies (nominal frequencies f_n higher than 500 MHz, capable of being higher than 10 GHz, currently capable of going up to 40 GHz and even of very largely exceeding these values in future) corresponding to very high throughputs (higher than 500 Mbits/s, capable of being higher than 10 Gbits/s, and capable of going up to 40 Gbits/s for SONET OC-768 and SDH STM-256 standards and capable of very largely exceeding these values in future) on a transmission channel (the implementation technology of which may be of any type: electrical, optical, radiofrequency etc.) of a baseband serial link a signal is transmitted incorporating digital data mixed with a clock signal in such a manner as to avoid having to transmit these two types of information on two different channels. This makes it possible to avoid any tricky pairing of the path-lengths of the signals. With such signals, at the receiver level it is necessary to extract from the received signal, which is of analogue nature, on the one hand the values of the digital data and, on the other hand, the clock signal corresponding to these data. In order to obtain the values of the data, the received signal is

sampled from the clock signal previously extracted from the data.

The most common solution in order to implement such a device for clock extraction and for extraction of data consists in using circuits including at least one phase-locked loop, known as PLL, which principally includes, at the output of a circuit generating pulses corresponding to the rising and falling edges of the received signal, a phase comparator supplying a set-point signal to a voltage-controlled oscillator, known as VCO, via a loop filter. The VCO provides an internal clock signal to a decision flip-flop constituting a sampling circuit which extracts the data from the received signal. These traditional PLL circuits, which use relaxation oscillators or LC mains oscillators, phase/frequency comparators and high-frequency digital dividers, exhibit various drawbacks. They are incompatible with connections having very high throughput; they require an external frequency reference; they require a synchronisation on start-up by a data preamble necessarily having to be present in the received signal, which is not admissible in certain applications; they exhibit great complexity for optimisation of operation and of implementation, numerous interdependent and contradictory parameters having to be taken into account, particularly so far as the phase/frequency comparator circuit is concerned; they have a very significant energy consumption; their analogue implementation is highly dependent on the technology for manufacture of the semiconductor components that is put into effect etc. Consequently, the implementation of a PLL circuit in order to implement a clock-extraction functionality requires the intervention of specialists in analogue circuits having considerable experience and considerable know-how, and, on

the other hand, requires significant periods of development, to be repeated regularly with each evolution of technology, something which is not admissible from the point of view of the current constraints of utilisation on an industrial scale.

Another known solution in order to implement the clock extraction is based on the use of a delay-locked loop, known as DLL. These circuits, however, require a specific code so far as the received signal is concerned, in particular with a start-bit and a stop-bit in order to form a reference transition in each word (which reduces the maximal transmission frequency accessible for the data, typically 33 % with useful data on 8 bits and a code such as 8B/12B). In addition, the recovered data exhibit a relatively significant phase drift (jitter), capable of resulting in a non-negligible bit-error rate. Also, such a DLL circuit is highly sensitive to noise in the received signal. Lastly, this technique which is put into effect by digital components is not easily compatible with extremely high transmission speeds.

FR 2 838 265 has proposed a solution consisting in using an injection oscillator - that is to say, an oscillator that is injection-locked onto the frequency of edges of the received signal in an open-loop circuit. In order to do this, the injection oscillator is an oscillator with negative resistances using a coupled pair of MOS transistors, and receives a synchronisation-pulse signal that is clocked at the clock-bit frequency f_{sr} of the received signal, this pulse signal being emitted by a generator of synchronisation pulses. This injection-locked oscillator exhibiting a frequency of free oscillations f_{os} has the property of being locked onto the signal of pulses

if the frequency of said signal is within its operating range, known as the lock-in range. It then provides a clock signal, the frequency of which corresponds exactly to the clock-bit frequency f_{sr} .

Nevertheless, the problem which is then posed is to ensure also the phase synchronisation of the clock signal provided by the oscillator in relation to the received signal. In this connection it is known that the phase shift introduced by the oscillator is proportional to the difference between the frequency of the signal at the input of the oscillator and the natural frequency f_{os} of said oscillator.

Consequently, it is possible to consider adjusting the value of the natural frequency of the oscillator as a function of the clock-bit frequency f_{sr} of the received signal when designing the circuit. But this solution remains imperfect, insofar as the value of this clock-bit frequency f_{sr} is simply not known with precision (which constitutes the principal initial technical problem requiring the presence of a clock-extraction circuit in the receiver). In addition, it would in any case require an adjustment of the circuit for each application. If such an adjustment is admissible within the context of a laboratory prototype, it is not acceptable in the majority of industrial applications of such a circuit.

FR 2 838 265 has proposed solving this problem of phase shift by providing a decision logic in order to select one value from various values provided by a plurality of sampling flip-flops shifted in accordance with distinct shift durations in relation to the pulses of the reception clock signal. It turns out that, in practice, this solution is not really effective in all situations.

Likewise, US 6,924,705 describes a PLL circuit including a digital phase detector, a charge pump and a loop filter controlling a voltage-controlled oscillator, this latter receiving the input data signal via a frequency doubler. Apart from the practical implementation of the digital phase detector not being indicated, this circuit exhibits the drawback of not being able to be implemented entirely in digital form, since the charge pump and the loop filter are components of analogue type. Consequently, the implementation of a circuit according to this document is strictly dependent in practice on the semiconductor technology that is put into effect and cannot be simply and rapidly adapted to another semiconductor technology without requiring a new design of the circuit beforehand. In addition, this circuit which exhibits a low range of admissible input frequencies and which is not automatically adapted to the received signal requires external manual adjustments of the free frequency of the oscillator and of the difference in propagation delays between the various lines, in particular that enabling the data to be extracted and that enabling the clock to be extracted. Consequently, the circuit described in this document cannot be the object of utilisation on an industrial scale in applications where the period of development has to be minimised and/or in those where it is necessary to be able to migrate frequently from one semiconductor technology to another and/or in those where the frequency of the received signal may vary within a wide range of values.

US 5,671,259 describes a clock-recovery circuit including a resonant circuit that is implemented with discrete components mounted on a printed circuit and a digital phase-locked loop including a counting circuit making it possible to format a control signal for adjustment of the

frequency of the resonant circuit. The operation of such a resonant circuit is not compatible with an implementation in integrated circuit(s) (the quality factor of the components in this technology being very inadequate) and only enables operating frequencies to be obtained that are not very high (of the order of 2 MHz for the clocking of incoming data). In addition, with such a resonant circuit in the absence of a transition in the data signal the oscillation disappears after a few cycles, so that this type of circuit is not compatible with data signals exhibiting few or no transitions over certain periods. Furthermore, in this document the phase of the input signal may vary over more or less a quarter of a bit - that is to say, an absolute variation of a half bit - without the phase-locked loop reacting, so that the accidental phase shifts between 0 % and 50 % are not detected. In addition, the counting circuit is a counter over 20 bits, only the 8 most significant bits being used for the control of the resonant circuit. Such an extremely high filtering (a difference of 4096 successive phase shifts being necessary before bringing about an adjustment) is totally ineffective in practice. Above all, contrary to what this document indicates, it does not enable in any manner the possible accidental phase shifts that are present in the input signal to be resolved.

In this way, despite intensive research that has been carried out on these clock-extraction circuits for a long time, the need persists to be able to propose a simple solution that is compatible with utilisation in large numbers on an industrial scale in the majority of the current practical applications of these circuits, including those with connections having very high output - in particular higher than 500 Mbits/s - and/or having very

high frequency - in particular higher than 500 MHz - the energy consumption of which is acceptable, and which requires neither external adjustments nor specific design, each manufactured circuit being necessarily regulated on account of its design independently of the production technology that is put into effect, and which remains perfectly in phase with the input data signals while being compatible with a very great variety of such input data signals, including when these latter exhibit periods exhibiting few transitions or without transitions, or numerous accidental phase shifts.

The invention therefore aims to propose such a solution. The inventors have indeed established that it was possible, by means of a specific architecture, to propose for the first time a clock-extraction device, and more particularly a device for clock extraction and for data extraction, that exhibits these qualities, and in particular that is very simple in implementation, 'self-regulated' (that is to say, not requiring any external manual regulation) while exhibiting a wide locking range and a very low bit-error rate while being compatible with a very great variety of input data signals.

The invention also aims to propose such a device that is quite insensitive to variation in quality of the received signals, and in particular that is compatible with signals that are capable of exhibiting a variable density of transitions, and noise.

The invention also aims to propose such a device that can be implemented almost entirely in the form of digital components, and in particular having a phase-locked loop that is integrally implemented in the form of digital

components. Indeed, the inventors have ascertained that this results, on the one hand, in a wider range of admissible frequencies for the received signal, and, on the other hand, in a simplicity of implementation of the device, and in particular a possibility of migration from one semiconductor technology to another in simple and rapid manner. The design of each circuit may be effected on the basis of libraries of standard functions without requiring the perfecting of specific components, unlike the former devices (for example, the voltage-controlled gates in a DLL circuit or the analogue components of a PLL circuit).

Throughout the text, the term 'digital component' designates any electronic component exhibiting at least one input terminal and/or output terminal, each terminal conveying a signal, the state of which may vary among a discrete plurality of states, in particular 1 and 0, without the real analogue value of the corresponding signal having an influence on the operation of the component or of the circuit within which it is integrated. Furthermore, throughout the text the terms 'input' and 'output' of a component designate a connecting terminal or a set of connecting terminals receiving or, respectively, supplying a unique signal. The signal applied to an input or supplied by an output may therefore be, apart from complementary precision, just as easily a serial signal as a parallel signal and may be constituted by a single channel or by several channels (particularly in the case of an architecture of differential type).

The invention therefore relates to a device for clock extraction from a baseband serial signal, known as the received signal, that is representative of digital data and

coded with a clock signal exhibiting a clock-bit frequency f_{sr} , including:

- a circuit receiving a signal resulting from the received signal and clocked at the clock-bit frequency f_{sr} , and supplying, to at least one clock output, a clock signal, known as the reception clock signal, at least substantially synchronised and in phase with the clock-bit frequency f_{sr} of the received signal,
- a phase-locked loop including:
 - a first input connected to a clock output of the circuit supplying a reception clock signal,
 - a second input which is fed by a signal resulting from the received signal,
 - a digital phase detector including a lead/lag detector connected to the first and second inputs and supplying to at least one output a digital signal, known as the phase-state signal, that is representative of a phase shift between the reception clock signal and the received signal, and of the direction of this shift,
 - an output supplying a signal, known as the control signal, which is connected to an input, known as the command input, of the circuit supplying a reception clock signal which is adapted so that the value of the frequency of the reception clock signal depends on the value of the control signal received at this control input,
 - a circuit, known as the counting circuit, exhibiting an input connected to said output of the digital phase detector, said counting circuit being adapted to implement at least one filtering by digital counting/down-counting in respect of the variations of the relative values of the digital signal which are supplied in time by the phase detector, and in order to supply a control signal in digital form, the value of which is a function of the result of this/these filtering(s), this value of the

control signal being adapted to set a value of the frequency of the reception clock signal equal to a value, filtered in this way, of the clock-bit frequency f_{sr} of the reception clock signal, characterised in that

- the circuit supplying a reception clock signal is an injection-locked oscillator with digital control, including a digital control input which is adapted to be able to receive the control signal supplied by the phase-locked loop in digital form, and so that the value of the natural frequency f_{os} of the oscillator depends on the value of the received control signal at this control input,
 - the phase-locked loop includes a circuit exhibiting at least one input connected respectively to the output(s) of the lead/lag detector, and supplying to at least one output a digital signal, known as the filtered phase-state signal:
 - having a first relative value after reception of a predetermined number N , greater than 1, of successive identical input values, corresponding to N successive data bits of the received signal for which the lead/lag detector has detected a phase shift in the same direction,
 - having a second relative value after reception of N successive identical input values, corresponding to N successive data bits of the received signal for which the lead/lag detector has detected a phase shift in the other direction,
 - having a third relative value in the other cases,
- so that the relative value of the filtered phase-state signal is representative of the presence of a phase shift in the same direction and of the direction of this phase shift, for N successive data bits of the received signal, between the edges of the reception clock signal and the corresponding data bits of the received signal.

The invention also extends to a device for clock extraction and for extraction of digital data including a clock-extraction device according to the invention. A device for clock extraction and for extraction of digital data according to the invention includes, in addition, a circuit for sampling of the received signal with the reception clock signal, this sampling circuit having a first input, known as the signal input, connected to the reception input, and a second input, known as the clock input, connected to a clock output of the injection-locked oscillator, this sampling circuit being adapted to supply digital data transmitted by the received signal to at least one data output, and is characterised in that it includes at least one phase-shifting circuit which is adapted to introduce a constant phase difference between the signal input and the clock input of the sampling circuit, the total phase difference between these two inputs resulting from each phase-shifting circuit being adapted to guarantee a phase alignment of the signal at the signal input and of the signal at the clock input.

Advantageously and according to the invention, the lead/lag detector is adapted to supply to a first output a digital signal that is representative of the presence of a phase lead between the reception clock signal and the received signal, and to a second output a digital signal that is representative of the presence of a phase lag between the reception clock signal and the received signal.

Advantageously and according to the invention, the lead/lag detector is adapted to sample the received signal at the rising and falling edges of the reception clock signal. More particularly, advantageously and according to the invention the lead/lag detector is adapted to implement a

double sampling, one in phase with the edges of the reception clock signal, the other in quadrature with the edges of the reception clock signal, in such a manner as to determine the intermediate state of the received signal.

Furthermore, advantageously and according to the invention a device according to the invention is characterised in that said circuit supplying the filtered phase-state signal is a decision-making converter.

In one embodiment of the invention, $N = 2$. Any other value may nevertheless be chosen, according to the desired level of filtering. Indeed, such a decision-making converter has the effect of implementing a first type of filtering starting from relative values of the phase shifts detected by the digital phase detector. This first filtering makes it possible to liken accidental phase shifts to noise, since only a series of N identical states of the phase shift will have an effect on the output of the decision-making converter. Typically, this first filtering makes it possible to avoid taking account of the phenomena of non-permanent accidental phase drifts such as the phenomena of jitter. In particular, it should be noted that the series of data bits exhibiting a phase shift in the same direction including a number of data bits capable of going as far as $N-1$ do not modify the value of the filtered phase-state signal.

Furthermore, advantageously and according to the invention said counting circuit includes at least one circuit, known as the accumulator circuit, including at least one input receiving a digital signal resulting from each phase-state signal supplied by the lead/lag detector, this accumulator circuit being adapted to supply a digital signal, known as

the counting/down-counting signal, the relative value of which is representative of the reception of a plurality of relative values exhibited at the input(s) of this accumulator circuit.

Advantageously and according to invention, said counting circuit includes successively a decision-making converter and an accumulator circuit that is adapted to aggregate the relative values of the filtered phase-state signal supplied by the decision-making converter.

In a device according to the invention, in combination with the first type of filtering described above, or in a variant, another type of filtering can be implemented by said counting circuit. In this way, advantageously and according to the invention the accumulator circuit exhibits a parallel output and is adapted to supply to this parallel output a parallel digital counting/down-counting signal, and the injection-locked oscillator includes a parallel digital control input comprising a number of bits lower than that of the parallel digital output of the accumulator circuit, only a portion of the high-weight bits of the parallel digital output of the accumulator circuit being linked to the bits of the parallel digital control input of the injection-locked oscillator, so that said control signal supplied by the counting circuit is formed from said portion of high-weight bits of said counting/down-counting signal.

In this way, the value of the control signal is modified only from the moment when the accumulator circuit has counted/down-counted a predetermined threshold number M of data bits having a phase shift in the same direction

between the edges of the reception clock signal and the corresponding data bits of the received signal.

In one embodiment according to the invention, the parallel digital output of the accumulator circuit comprises, for example, 8 or 9 bits, and the parallel digital input of the injection-locked oscillator comprises 5 bits, only the 5 high-weight bits of the parallel digital output of the accumulator circuit being linked to the 5 bits of the parallel digital control input of the injection-locked oscillator. In this way, the control signal is modified only from the moment when the accumulator circuit has detected an unbalance of the total (representative of phase shifts in the same direction) at least equal to 111 (binary value) in the relative values that it receives at the input. In this example, in the absence of a decision-making converter it would therefore be the case that $M = 111$.

Said accumulator circuit can be implemented by one or more adders and/or by one or more counters. It should be noted that by virtue of the counting and down-counting function, the M data bits of a series of data bits of identical phase shifts triggering a modification of the control output are not necessarily all successive. For example, they may be, on the contrary, separated by data bits for which no phase shift is detected, even by data bits exhibiting a phase shift in the opposite direction, subsequently compensated by other subsequent data bits. This second type of filtering therefore detects a general drift of the phase over at least M data bits.

The fact of retaining only a portion of the bits (of high weight) of the parallel digital output of the accumulator

circuit in order to act as control signal of the injection-locked oscillator makes it possible to implement in this way a second type of filtering having rather different characteristics from the first type of filtering. Be that as it may, the filtering implemented on the variations of the phase shifts is adapted in accordance with the dynamic response desired for the feedback loop.

In the embodiment variants of the device according to the invention in which the two types of filtering are used successively in combination, the fact of being able to implement this filtering in two successive stages, one of which is constituted by the decision-making converter, and the other by said accumulator circuit, makes it possible, in particular, to reduce the working frequency of the accumulator, facilitating its use at high frequency. In addition, the first type of filtering makes it possible to minimise the risk of a variation of the high-frequency control signal when the data exhibit an accidental phase drift (jitter), whereas said accumulator circuit has previously down-counted a number of successive data bits of identical phase shifts close to the threshold value which triggers the variation of the control signal. In order to avoid this phenomenon of variations at high frequency, it is also possible to implement the accumulator circuit with the aid of several adders and/or several counters in cascade with a device for reloading of an intermediate value, for example a median value, when said threshold value has been exceeded, so that the accumulator circuit resumes the counting/down-counting from this intermediate value.

This/these digital filtering(s) resulting from the structure of the decision-making converter and/or from the

link between the accumulator circuit and the digital control input of the injection-locked oscillator make(s) it possible to dispense with any specific filtering component in the phase-locked loop.

In an advantageous embodiment and according to the invention, the digital control input of the injection-locked oscillator is connected to a circuit including a plurality of switches, each switch being connected in series to at least one integrated condenser in the circuit of the oscillator in such a way as to modify its natural frequency. Advantageously and according to the invention, each bit of the digital control input is linked to one of the switches.

In addition, advantageously and according to the invention the clock-extraction circuit includes, in addition, a circuit, known as the synchronisation-pulse generator, generating a current-pulse signal at the frequency of edges of the received signal and adapted for operation of the injection-locked oscillator, this synchronisation-pulse generator being adapted to supply the current-pulse signal to a single output connected solely to a current input of the injection-locked oscillator. The current pulses supplied by this synchronisation-pulse generator are adapted at the input of the injection-locked oscillator in such a way as to ensure its operation - that is to say, the locking of the oscillator onto the clock-bit frequency fsr.

Furthermore, any type of injection-locked oscillator may be used within the scope of the invention. It may be a question, in particular, of a relaxation oscillator of RC type or with current-source, of an unstable oscillator with logic gates or coupled transmitters, of a ring oscillator,

of a quasi-sinusoidal oscillator with Wien bridge, phase displacement or LC, of a Colpitts, Hartley, Clapp, Pierce oscillator or with negative resistance with LC resonant circuit, with transmission lines or quartz-type resonator, a resonator with surface waves, with integrated MEMS or piezoelectric element, etc. Nevertheless, advantageously and according to the invention the injection-locked oscillator is of the type constituted by an LC resonant circuit. Such an oscillator exhibits, in particular, the advantage of minimising the intrinsic phase drift (jitter). More particularly, advantageously and according to the invention the injection-locked oscillator includes two branches, each including a field-effect transistor with negative resistance, the two transistors being coupled in accordance with a differential topology. It may be a question of an oscillator as described in FR 2 838 265.

In this way, the invention makes it possible to bring about decisive advantages in the design of clock-extraction devices, and more particularly of devices for clock extraction and extraction of digital data, enabling development on an industrial scale of a circuit, the operation of which is based on an injection-locked oscillator.

In particular, a device according to the invention is free from charging pump and from loop filter, and more generally from analogue component in the phase-locked loop. Consequently, in a device according to the invention the phase-locked loop can be developed with a homogeneous, entirely digital, simple and fast design.

A device according to the invention is also completely autonomous - that is to say, it requires no manual or other

external adjustment, nor any calibration. In this way, advantageously a device according to the invention is free from any means for external manual adjustment. Moreover, this autonomy is obtained with great simplicity of implementation.

A device according to the invention does not require the presence of an external frequency reference either, unlike a traditional PLL. In addition, a few data bits are sufficient to ensure synchronisation at start-up. By virtue of its very great simplicity, the architecture of a device according to the invention enables its implementation with a very small number of elementary components having low energy consumption (therefore a reduced total surface area and a lower total consumption). A device according to the invention can also be designed using digital technology, particularly so far as the phase-locked loop is concerned, without requiring the intervention of a designer possessing considerable know-how (unlike the prior devices based on PLL, in which, in particular, it is very difficult to implement a phase/frequency comparator operating at high frequency). With a device according to the invention of simple design it is also possible to attain transmission speeds close to the limits offered by semiconductor technology. In a particular case it is possible to attain transmission speeds that are substantially higher than with prior circuits based on PLL or DLL. In addition, it is possible to implement a device according to the invention with any semiconductor technology (CMOS, bipolar, SiGe, ...).

Unlike a circuit based on DLL, a device according to the invention is quite insensitive to noises in the received signal, and the coding of the data exhibits a rate of

expansion similar to that of a traditional PLL - that is to say, much lower than that required for a DLL.

Furthermore, in view of the simplicity and effectiveness of the phase-control loop, in a device according to the invention the natural frequency f_{os} of the oscillator is always equal to the clock-bit frequency f_{sr} of the reception clock signal; consequently, the phase deviation between the clock signal supplied by the oscillator and the received signal is fixed. Now, since the totality of the other elements constituting the device are capable of bringing about a constant phase displacement between the two inputs of the sampling circuit, it is possible to determine the constant structural differential phase lag between these two inputs of the sampling circuit. Consequently, it is sufficient to provide one (or more) phase-shifting circuits in order to guarantee a phase alignment between the two inputs of the sampling circuit without requiring any external adjustment, so that the device according to the invention can operate autonomously and stably with a wide lock-in range. In addition, in a device according to the invention the sampling circuit may be simply constituted by a simple flip-flop D.

It should be noted in this respect that this/these phase-shifting circuit(s) is/are provided in supplement to the possible phase-shifting circuit sometimes necessarily provided at the input of a circuit such as a phase comparator, in order to compensate the phase displacements introduced by certain architectures of this type of circuit. Such a phase-shifting circuit which is necessary for the operation of a phase comparator which it feeds is functionally different from the phase-shifting circuit(s) of a device according to the invention, the function of

which is to introduce a supplementary phase displacement in order to compensate the total phase displacement between the two inputs of the sampling circuit.

Advantageously a device according to the invention is implemented in the form of at least one integrated circuit incorporating at least the injection-locked oscillator. A device for clock extraction and for extraction of digital data according to the invention is adapted to be able to operate with a clock-bit frequency f_{sr} higher than 500 MHz.

In this way, the invention makes it possible, for the first time, to obtain a clock-extraction circuit, and more particularly a circuit for clock extraction and for extraction of digital data, that is perfectly autonomous and stable, being capable of being the object of utilisation on an industrial scale in numerous applications.

The invention also relates to a clock-extraction device, and more particularly a device for clock extraction and for extraction of digital data, characterised in combination by all or some of the characteristics mentioned above or below.

Other aims, characteristics and advantages of the invention will become apparent from the following description which is given by way of non-limiting example and which refers to the appended Figures, in which:

- Figure 1 is a general functional block diagram illustrating a device for clock extraction and for extraction of digital data according to a first embodiment of the invention,

- Figure 2 is a functional block diagram of an embodiment of the lead/lag detector of the device shown in Figure 1,
- Figure 3 is a functional block diagram of an embodiment of the decision-making converter of the device shown in Figure 1,
- Figure 4 is a diagram illustrating an embodiment of an injection-locked oscillator that is capable of being used in a device according to the invention,
- Figure 5 is a diagram illustrating an exemplary embodiment of an 8-bit adder that is capable of being used in the device shown in Figure 1,
- Figure 6 is a diagram illustrating an exemplary embodiment of a 2-bit accumulator that is capable of being used in order to implement the adder shown in Figure 5,
- Figure 7 is a diagram illustrating an embodiment of a block of capacitors at the digital control input of the oscillator shown in Figure 4,
- Figure 8 is a diagram illustrating a second embodiment of a counting circuit of a device according to the invention,
- Figure 9 is a diagram illustrating a third embodiment of a counting circuit of a device according to the invention,
- Figure 10 is a diagram illustrating a fourth embodiment of a counting circuit of a device according to the invention.

A device for clock extraction and for extraction of digital data according to the invention which is represented in Figure 1 receives at a principal input, known as the reception input 10, a signal, known as the received signal, which is a baseband serial signal that is representative of digital data D and that is coded with a clock signal exhibiting a clock-bit frequency f_{sr} . In general, this received signal is a coded signal of type NRZ (non-return to zero) received on a transmission channel of a baseband serial link. This transmission channel may be constituted by a single electrically conductive wire or by a single optical fibre or by a single-channel radiofrequency link (non-differential signal). The invention is nevertheless also applicable in the case of a received signal of the type transmitted differentially, the transmission channel then including two lines transmitting two components in phase opposition. The invention is also applicable to other types of coding of the received signal, for example NRZI (non-return to zero inverted).

The reception input 10 is connected to a branching node 11 to which two branches are connected in parallel, namely a first clock-extraction branch 12 according to the invention, generating at a clock output 13 a clock signal, known as the reception clock signal H, synchronised and in phase with the clock-bit frequency f_{sr} of the received signal, and another, second branch 14 including a circuit 15 for sampling the received signal with the reception clock signal H, this sampling circuit 15 being adapted to supply, at a data output 16, digital data transmitted by the received signal.

The clock-extraction circuit 12 includes an injection-locked oscillator 19 which is fed by a synchronisation-

pulse generator 20, this latter exhibiting an input 21 connected to the node 11 of the reception input 10. The synchronisation-pulse generator 20 exhibits a single output 22 (which may be constituted by two lines in the case of a differential topology) connected solely to the current input 23 of the injection-locked oscillator 19. The current-pulse signal provided by the synchronisation-pulse generator 20 is adapted to the operation of the injection-locked oscillator 19 and is clocked at the frequency of edges of the data D of the received signal. The whole can be implemented, for example, as described by FR 2 838 265. In particular, the injection-locked oscillator 19 is then of the type constituted by a symmetrical LC resonant circuit defining the frequency of free oscillations f_{os} of oscillation and endowed with two crossed branches, each including a field-effect transistor with negative resistance, the two transistors being in this way coupled in accordance with a differential topology. The injection-locked oscillator 19 exhibits a clock output 29 supplying a clock signal that is synchronised and in phase with the clock-bit frequency of the received signal.

The sampling circuit 15 includes a first input, known as the signal input 17, connected by the second branch 14 to the reception input 10, and a second input, known as the clock input 18, connected to the clock output of the clock-extraction circuit 12 - that is to say, to the clock output 29 of the oscillator 19. This sampling circuit 15 may be constituted by a simple flip-flop D.

The injection-locked oscillator 19 includes, furthermore, an input, known as the control input, which is adapted so that the value of the natural frequency f_{os} of the oscillator depends on the value of the digital control

signal received at this control input. The control input is a digital parallel input which, in the example represented, comprises 5 bits 24a, 24b, 24c, 24d, 24e.

The oscillator 19 may be constructed from any type of oscillator, since it can be adapted in order to exhibit a digital control input as described below. It may be a question, in particular, of a relaxation oscillator of RC type or with current-source, of an unstable oscillator with logic gates or coupled transmitters, of a ring oscillator, of a quasi-sinusoidal oscillator with Wien bridge, phase displacement or LC, of a Colpitts, Hartley, Clapp, Pierce oscillator or with negative resistance with LC resonant circuit, with transmission lines or quartz-type resonator, a resonator with surface waves, with MEMS or integrated piezoelectric element, etc.

The oscillator 19 is, for example, implemented as described by FR 2 838 265 and represented schematically Figure 4. It is then of the type constituted by a symmetrical LC resonant circuit defining the frequency of free oscillations f_0 and endowed with two crossed branches 40a, 40b, each including a field-effect transistor 41a, respectively 41b, with negative resistance, the two transistors 41a, 41b being in this way coupled in accordance with a differential topology. The pair of transistors 41a, 41b is charged by a symmetrical LC circuit defining the oscillation frequency starting from a reference polarisation voltage V_2 applied between two inductors 42a, respectively 42b, and from a current-source 47, the output of which is at the lowest potential and which may be simply constituted by a series resistor connected to a junction node of the two sources of the transistors 41a, 41b.

Each transistor 41a, 41b is furthermore polarised by an appropriate polarisation voltage V_1 applied to its drain 50a, 50b by means of a series resistor 48a, 48b and a parallel capacitor 49a, 49b.

The parallel capacitors of the LC resonant circuit are constituted by a block 43 of capacitors, each associated respectively with a switch 45a, 45b, 45c, 45d, 45e, each switch receiving one of the bits 24a, 24b, 24c, 24d, 24e of the parallel digital control input of the oscillator 19. The parallel capacitors are associated in such a way that the variation of an increment (a unit) of the digital signal received at input brings about a variation of an identical value Δf of the oscillation frequency f_{os} of the oscillator 19. In the embodiment shown in Figure 8, each switch 45a, 45b, 45c, 45d, 45e is interposed between two condensers 44a', 44b', 44c', 44d', 44e', and, respectively, 44a'', 44b'', 44c'', 44d'', 44e'', of identical value arranged symmetrically in series in relation to this switch, these two condensers constituting said capacitor which is associated with the switch. Each switch 45a, 45b, 45c, 45d, 45e is constituted by a field-effect transistor, and the values of the capacitances are equal to $2^n \times 2C$, n being the rank (0, 1, 2, 3, 4) of the bit b_3 , b_4 , b_5 , b_6 , b_7 being considered of the digital control signal applied at the digital input 24a, 24b, 24c, 24d, 24e, C being a predetermined capacitance value, and the capacitance value of each condenser 44a', 44a'', 44b', 44b'', 44c', 44c'', 44d', 44d'', 44e', 44e'' being respectively equal to C , C , $2C$, $2C$, $4C$, $4C$, $8C$, $8C$, $16C$, $16C$, as represented in Figure 7.

The value of the variation step Δf is chosen to be sufficiently low, preferably lower than 1 % of the mean

value of the oscillation frequency f_{os} , in particular of the order of 0.3 % of this mean value. For example, Δf is of the order of 30 MHz for an oscillation frequency f_{os} of the order of 10 GHz.

The amplitude of oscillation of the oscillator 19 is controlled with the aid of two diodes 46a, respectively 46b, mounted between the drain 50a, 50b and the grid 51a, 51b of each corresponding transistor 41a, 41b by means of a filtering capacitor 52a, 52b.

The clock-extraction circuit 12 of the device according to the invention includes a phase-control loop 25 entirely constituted by digital components. This phase-control loop 25 includes a lead/lag detector 26 exhibiting two inputs 27, 28. The first input 27 of the lead/lag detector 26 is connected to the output 29 of the oscillator 19 in such a manner as to receive the reception clock signal H generated by the oscillator at this output 29. The second input 28 is connected to the branching node 11 and therefore to the reception input 10. In this way, the received signal is supplied to the second input 28 of the lead/lag detector 26.

An embodiment of the lead/lag detector 26 is represented in Figure 2. This lead/lag detector 26 exhibits two parallel digital outputs 33a, 33b, to each of which it supplies a signal, known as the phase-state signal E, respectively L, that is representative of the existence and of the direction of a phase shift between its two inputs 27, 28 - that is to say, between the data D of the received signal and the reception clock signal H provided by the oscillator 19. In particular, the signals E and L supplied respectively to the parallel digital outputs 33a, 33b of

the lead/lag detector 26 are zero when the signals at its two inputs 27, 28 are in phase. The first output 33a of the lead/lag detector 26 is a digital signal E on 1 bit which identifies the presence of a phase lead between the two inputs 27, 28. In the example described, this signal E is equal to 1 when a phase lead is detected and is equal to 0 when the two inputs 27, 28 are in phase. The second output 33b of the lead/lag detector 26 supplies a digital signal L on 1 bit which identifies the presence of a phase lag between the two inputs 27, 28. In the example described, this signal L is equal to 1 when a phase lag is detected, and is equal to 0 when the two inputs 27, 28 are in phase.

Any type of digital lead/lag detector 26 may be used in a device according to the invention. It may be a question, in particular, of an Alexander cell (cf. J.D.H. Alexander "Clock recovery from random binary signals" Electronics Letters 30 October 1975 Vol. 11 No. 22). In this way, in the embodiment represented in Figure 2 the lead/lag detector 26 is constituted by an Alexander cell based on a double sampling of the received signal, a first time in phase with the reception clock signal H, a second time in quadrature with this signal. In this way, this lead/lag detector 26 includes a first stage of two flip-flops D 61, 62 receiving the received signal and the reception clock signal H, a quadrature-shift gate 65 being interposed at the input of the second flip-flop D 62 of the first stage at its terminal receiving the clock signal. The detector 26 includes a second stage of two flip-flops D 63, 64 and two exclusive OR gates 66, 67 in order to form the signals that are representative of the phase shift. The output of the first flip-flop 61 of the first stage provides a signal DI(n) that is representative of the in-phase sampling of a

bit n of the received signal. The output of the first flip-flop 63 of the second stage connected downstream of the first flip-flop 61 of the first stage provides a signal $DI(n-1)$ that is representative of the in-phase sampling of bit $n-1$ immediately preceding said bit n in the received signal. The output of the second flip-flop 62 of the first stage provides a signal $DQ(n+1/2)$ that is representative of in-quadrature sampling between the data bits n and $n+1$. The output of the second flip-flop 64 of the second stage provides a signal $DQ(n-1/2)$ that is representative of the in-quadrature sampling between the data bits n and $n-1$. Two flip-flops D 68, 69 are furthermore provided, in order to form an output register making it possible to synchronise the signals with the reception clock.

The following Table 1 is a truth table of an example of a particular lead/lag detector 26:

TABLE 1:

$DI(n-1)$	$DQ(n-\frac{1}{2})$	$DI(n)$	E	L	Meaning
0	0	0	0	0	in phase
0	0	1	1	0	lead
0	1	0	1	1	impossible
0	1	1	0	1	lag
1	0	0	0	1	lag
1	0	1	1	1	impossible
1	1	0	1	0	lead
1	1	1	0	0	in phase

It should be noted that the digital phase detector constituted by the lead/lag detector 26 makes it possible to detect solely the existence of a phase shift and its direction, but not the amplitude of this phase shift.

The two outputs 33a, 33b of the lead/lag detector 26 are connected respectively to two inputs 32a, 32b of a decision-making converter circuit 30 of the phase-control loop, an exemplary embodiment of which is given Figure 3. This decision-making converter circuit 30 makes it possible to supply to a parallel digital output with two terminals 31a, 31b a digital signal, known as the filtered phase-state signal, having three states according to the values taken by the phase-state signal - that is to say, the lead signals E and lag signals L supplied for each data bit of the received signal by the lead/lag 26 converter.

The decision-making converter 30 modifies the value of the filtered phase-state signal supplied to its parallel digital output only when it receives successively a predefined number of identical values at its inputs 32a, 32b corresponding to a predefined number of successive data bits of the received signal for which the lead/lag detector 26 has detected a phase shift in the same direction.

The filtered phase-state signal is, for example, a signed binary signal coded on two bits a_0 and a_1 , each bit corresponding to one of the two output terminals 31a, 31b. When the phase shifts of the successive data bits detected are in a first direction, for example when the reception clock signal H is leading, the filtered phase-state signal is equal to 1, coded by the values $a_0 = 1$ and $a_1 = 0$. When the phase shifts of the successive data bits detected are in the other direction, for example when the reception clock signal H is lagging, the filtered phase-state signal is equal to -1, coded by the values $a_0 = a_1 = 1$. When the data bits are in phase, the filtered phase-state signal is zero, coded by the values $a_0 = a_1 = 0$.

Consequently, the function of the decision-making converter 30 is to implement a filtering of the variations of the phase shift detected by the detector 26 in order to take into account only the phase shifts that are reproduced in a number n , greater than 1, of successive data bits of the received signal. The function of the decision-making converter 30 is also to convert the phase-state signals E and L into filtered phase-state signals a_0 and a_1 .

This decision-making converter 30 includes, firstly, a stage of two flip-flops D making it possible to store the states $E(n-1)$, $L(n-1)$ of each of the signals E and, respectively, L received at its inputs 32a, 32b for a bit $n-1$ in relation to the state $E(n)$, $L(n)$ of these signals for an immediately successive bit n . The decision-making converter 30 includes, in addition, two stages of AND gates 72, 73 and an OR gate 74 making it possible, in the example represented, to detect the states of each of the signals E and, respectively, L received at its inputs 32a, 32b remaining identical on two successive data bits. It is sufficient to multiply the input flip-flops D and the AND gates in order to increase the number of successive data bits taken into account by the decision-making converter.

Two flip-flops D 75, 76 are furthermore provided, in order to form an output register making it possible to synchronise the signals a_0 , a_1 supplied to the output terminals 31a, 31b of the decision-making converter 30 with the reception clock.

The following Table 2 is a truth table of an example of a decision-making converter 30 for which $n = 2$:

TABLE 2:

$E_{(n)}$	$E_{(n-1)}$	$L_{(n)}$	$L_{(n-1)}$	a_1	a_0	Relative value of counting/ down-counting signal	Remarks
0	0	0	0	0	0	+0	
1	0	0	0	0	0	+0	1 st cycle where E=1
1	1	0	0	0	1	+1	2 nd successive cycle where E=1
1	1	0	0	0	1	+1	3 rd successive cycle where E=1
0	1	0	0	0	0	+0	1 st cycle where E passes through 0
0	0	0	0	0	0	+0	
0	0	1	0	0	0	+0	1 st cycle where L=1
0	0	1	1	1	1	-1	2 nd successive cycle where L=1
0	0	1	1	1	1	-1	3 rd successive cycle where L=1
0	0	0	1	0	0	+0	1 st cycle where L passes through 0
0	0	0	0	0	0	+0	

The two output terminals 31a, 31b of the decision-making converter 30 are connected to two input terminals 34a, 34b of an adder 35 of the phase-control loop. This adder 35 is adapted to aggregate the relative values +1, 0, -1 of the filtered phase-state signal. In the example described, adder 35 exhibits a parallel output 36 on 8 bits to which the result of the aggregate is applied. According to the invention, not all the bits of output 36 are used in order to control the oscillator 19. In fact, only the high-weight bits 36a of the signal supplied to the parallel output 36 are used in order to constitute the parallel digital control signal supplied by adder 35 to the oscillator 19. The low-weight bits 36b, which in reality are representative solely of the relative phase noise

(jitter) are not used. In the example represented, the 5 high-weight bits are used by way of control signal of the oscillator 19. By virtue of this, by using only a portion of the high-weight bits of the signal at the output of adder 35 a filtering is implemented by continuous integration of the signal provided by the digital phase detector 26, 30.

Figure 5 represents an exemplary embodiment of such an adder 35 constituted by a cascade of four 2-bit accumulators 81, 82, 83, 84 in series. Figure 6 represents an exemplary embodiment of a 2-bit accumulator that is capable of being used in the adder shown in Figure 5. Such a 2-bit accumulator is constituted by two AND/OR gates 101, 102 and two exclusive OR gates 103, 104 with three inputs. Three flip-flops D 105, 106, 107 constitute an output register.

In adder 35 the four 2-bit accumulators 81, 82, 83, 84 are assembled in accordance with a pipeline architecture including three synchronisation flip-flops D 85, 86, 87 and an output register constituted by three flip-flops D 88, 89, 90, by the output flip-flops 105, 106 of the first 2-bit accumulator 81, by the output flip-flop 105 of the second 2-bit accumulator 82, and by the output flip-flops 105, 106 of the last 2-bit accumulator 84. The 8-bit adder makes it possible to supply at the output a signal aggregated on 8 bits b0, b1, b2, b3, b4, b5, b6, b7. In the example described, only the high-weight bits b3, b4, b5, b6, b7 are supplied to the injection-locked oscillator 19. It goes without saying that any other known structure of an 8-bit adder exhibiting the same functions may be used within the scope of the invention.

It should be noted that the phase-control loop 25 of a device according to the invention exhibits properties of self-adaptation at the level of the phase noise of the received signal, since the gain of this phase-control loop decreases when the standard deviation of the phase noise increases, which in fact brings about a reduction of the overall pass-band of the filter.

The double digital filtering implemented by the decision-making converter 30, on the one hand, and by the suppression of the low-weight bits at the output of adder 35, on the other hand, makes it possible to dispense with the use of an analogue loop filter.

In a device according to the invention, no manual external adjustment is necessary so far as the natural frequency f_0 of the oscillator 19 is concerned. In addition, whatever the received signal, the phase-control loop 25 makes it possible to ensure that the reception clock signal H provided by the oscillator 19 is always in phase with the received signal.

Under these conditions, in a device according to the invention the phase shifts due to the propagation delays in the various branches of the circuit are all known and constant and may therefore be compensated by a phase-shifting circuit (or several such circuits) 37 placed between the branching node 11 and each of the inputs 17, 18 of the sampling circuit 15. It is, in fact, important that the sampling circuit 15 implements a sampling of the received signal in the central zone of the period of each data bit of the received signal where the value of the corresponding voltage is most stable and where the noise margin is the greatest, in order to avoid implementing the

sampling at the start or at the end of the period of each bit where the voltage of the signal is subjected, in the course of set-up, to a phase drift traditionally designated as jitter). In that the received signal, which is generally noisy, each bit appears in the form of an 'eye', taking into account the phase drift (jitter). The sampling has to take place in the centre of the eye.

Now, since the difference between the clock-bit frequency f_{sr} of the received bits and the oscillation frequency f_{os} of the oscillator 19 is zero in a device according to the invention and the totality of the lags that are capable of being introduced by the other components of the circuit and the totality of the propagation delays in the various branches of the circuit are controlled and known, it is possible to determine the structural and constant differential phase lag between the data contained in the received signal and the reception clock signal H supplied by the oscillator 19. This differential lag is compensated by the phase-shifting circuit(s) 37.

A single phase-shifting circuit 37 may be provided in the device according to the invention at any appropriate place. In a variant, the phase displacement between the two branches 12, 14 can be obtained by means of a plurality of phase-shifting circuits 37 distributed at several places in each branch. In this last case the aggregate of the phase displacements introduced by each phase-shifting circuit 37 is equal to the total phase displacement that has to be implemented between the two branches 12, 14.

In Figure 1 possible locations at which a phase-shifting circuit 37 may be provided are represented by different dotted lines. In this way, a phase-shifting circuit 37a

may be provided between the branching node 11 and the signal input 17 of the sampling circuit 15; a phase-shifting circuit 37b between the output 29 of the oscillator 19 and the clock input 18 of the sampling circuit 15; a phase-shifting circuit 37c between the branching node 11 and the input 21 of the pulse-generator 20 feeding the oscillator 19; a phase-shifting circuit 37d between the output 22 of the pulse-generator 20 and the input 23 of the oscillator 19; a phase-shifting circuit 37e between the branching node 11 and the second input 28 of the lead/lag detector 26; a phase-shifting circuit 37f between the output 29 of the oscillator 19 and the first input 27 of the lead/lag detector 26. Each phase-shifting circuit 37 may be constituted by a simple delay line.

The architecture of a device according to the invention is intrinsically very insensitive to transient events such as the changes of state of a signal that are due to an ionising particle once the oscillator 19 is in locked mode. In fact, the synchronisation of the oscillator with the clocking of the received signal makes it possible to mask the perturbations of external origin.

Figure 8 represents a second embodiment of a counting circuit that is capable of being used in a device according to the invention. This second embodiment differs from the previous one in that the decision-making converter 30 and the adder circuit 35 are replaced by a single counting/down-counting circuit component 55 which exhibits an output 57 on 8 bits and receives directly at its input the phase-state signal supplied by the phase detector 26, namely the phase-lead signal E at its counting input 56a (UP) connected to the first output 33a of the lead/lag detector 26, and the phase-lag signal L at its down-

counting input 56b (DOWN) connected to the second output 33b of the lead/lag detector 26. The counter/down-counter 55 is clocked by the reception clock signal H. It is chosen in such a way that the value of its output 57 remains unmodified when the values exhibited at its inputs 56a and 56b are inactive.

A single level of filtering is obtained by virtue of the fact that, as in the previous first embodiment, only a portion (b3, b4, b5, b6, b7 in the example represented) of the high-weight bits of the output signal supplied by the counter/down-counter 55 is used in order to form the control input of the oscillator 19.

The third embodiment represented Figure 9 differs from the first embodiment by virtue of the fact that the adder circuit 35 is replaced by two adder stages 91, 92, a first, low-level adder stage 91 of which providing at its output low-weight bits, namely 4 low-weight bits b0, b1, b2, b3 in the example represented, of the counting/down-counting signal, and a second, high-level adder stage 92 providing at its output high-weight bits, namely 5 high-weight bits b4, b5, b6, b7, b8 in the example represented, of the counting/down-counting signal.

The first adder stage 91 includes an adder circuit 93 including two parallel digital 4-bit inputs providing the sum of the two inputs at a digital 4-bit output. The first input of this adder circuit 93 is fed from the phase-state signal E, L by the outputs 33a, 33b of the lead/lag detector 26 via the decision-making converter 30. The output 31b of the decision-making converter 30 supplying the filtered phase-state signal a1 is connected to three inputs of adder 93. If $E = 1$, the decision-making

converter 30 supplies the signal 0001 (corresponding to the relative value +1) to the input of adder circuit 93. If $L = 1$, the decision-making converter 30 supplies the signal 1111 (corresponding the relative value -1) to the input of adder circuit 93. The output of adder circuit 93 is connected to the input of a multiplexer 98 which also receives at its input a value recorded in a 4-bit register 97. This value is preferably a median value - that is to say, a value starting from which it is necessary to count an identical number of variations (not necessarily immediately successive) in one direction or the other in order to trigger a modification of the value of the control input of the oscillator 19 - that is to say, of the signal at the output of the second adder stage 92. In the example represented, register 97 contains the value 0111, so that the control signal will be modified only starting from the detection of an unbalance of 7 or 8 states in the same direction (or another number, according to the value contained in register 97).

The output of the multiplexer 98 is an output on 4 parallel bits supplied to a register 95 clocked by the reception clock signal H. This register 95 provides the low-weight output bits b_0 , b_1 , b_2 , b_3 which are supplied to the second input of adder circuit 93 by means of a loop-back.

The second adder stage 92 includes an adder circuit 94 on 5 bits which is fed by a carry-over calculation circuit 100 detecting the extreme values (lower than zero and greater) of the low-weight output b_0 , b_1 , b_2 , b_3 . This carry-over calculation circuit 100 makes it possible to feed a 5-bit input of adder circuit 94 with a parallel digital signal constituting 5 high-weight bits in relation to the low-weight output b_0 , b_1 , b_2 , b_3 of the first adder stage 91.

In order to do this, the low-weight output signal b_0, b_1, b_2, b_3 is supplied to the input of two gates 105, 106 of the carry-over calculation circuit 100. The output of the AND gate 105 is equal to 1 when all the bits b_0, b_1, b_2, b_3 are equal to 0; it is equal to 0 when at least one of bits b_0, b_1, b_2, b_3 is equal to 1. The output of gate 105 is connected to the input of an AND gate 110, the output of which is applied to four high-weight bits c_2, c_3, c_4, c_5 of one of the two inputs of adder circuit 94 of the second stage 92. The output of gate 106 is equal to 1 when all the bits b_0, b_1, b_2, b_3 are equal to 1; it is equal to 0 when at least one of bits b_0, b_1, b_2, b_3 is equal to 0. The output of gate 106 is connected to the input of an AND gate 113, the output of which is connected to the input of an OR gate 112, the output of said OR gate forming the low-weight bit c_1 of the same input of adder circuit 94 of the second stage 92. Furthermore, the output of gate 110 is connected to the second input of the OR gate 112.

When bits b_0, b_1, b_2, b_3 are all equal to 0, the output of gate 105 is equal to 1, and, if gate 110 allows, the same applies to the high-weight bits c_2, c_3, c_4, c_5 of the input of adder circuit 94, as well as one of the inputs of gate 112. Therefore the output of gate 112 is equal to 1, and the same applies to the low-weight bit c_1 of the input of adder circuit 94. Consequently, in this situation the input c_1, c_2, c_3, c_4, c_5 of adder circuit 94 of the second stage is equal to 11111, corresponding to the relative value -1 controlling a decrementation of a unit of register 96.

Likewise, when bits b_0, b_1, b_2, b_3 are all equal to 1 the output of gate 106 is equal to 1, and, if gate 113 allows, the same applies to the low-weight bit c_1 of the input of

adder circuit 94. Simultaneously, the output of gate 105 is equal to 0, and the same applies to the high-weight bits c2, c3, c4, c5 of the input of adder circuit 94.

Consequently, in this situation the input c1, c2, c3, c4, c5 of adder circuit 94 of the second stage is equal to 00001, corresponding to the relative value +1 controlling an incrementation of a unit of register 96.

So long as one of the bits b0, b1, b2, b3 is equal to 0 and one of bits b0, b1, b2, b3 is equal to 1 - that is to say, when the low-weight output of the first adder stage 91 has a value that does not correspond to one of the extreme values, the outputs of the two gates 105, 106 are both equal to zero, so that the input c1, c2, c3, c4, c5 of adder circuit 94 of the second stage is equal to 00000, so that the value of register 96 is not modified.

In this way, as soon as an extreme value of the low-weight output signal b0, b1, b2, b3 is attained, on the one hand the content of register 96 is incremented or decremented, because gates 105 or 106 permit the relative value +1 or -1 upstream of the input c1, c2, c3, c4, c5 of adder 94 to be propagated, and, on the other hand, the low-weight bit c1 of the input of adder circuit 94 being equal to 1, this value +1 or -1 activates the control signal of the multiplexer 98 which forces the reloading of register 95 with the value contained in register 97.

In this way, it is guaranteed that it is necessary for a phase shift of 7 or 8 states to occur in the same direction starting from the median value recorded in register 97 so that the control signal supplied to output 36a is effectively modified.

Adder circuit 94 exhibits an output on 5 bits b4, b5, b6, b7, b8 stored in a register 96 clocked with the reception clock signal H, the output of this register constituting the output 36aa feeding the control input of the digital oscillator 19.

The output of register 96 is likewise provided at the second input of adder circuit 94 by means of a loop-back. Furthermore, the carry-over calculation circuit 100 also makes it possible, if the dynamics of the system require it, to avoid the untimely variations of the signal at the high-weight output 36a when the value of this signal attains an extreme value. In order to do this, the carry-over calculation circuit 100 includes two gates 107, 108 receiving the values of the high-weight bits b4, b5, b6, b7, b8 of output 36a, and the carry-over calculation circuit 100 is adapted to prohibit the incrementation of a unit when the signal on bits b4, b5, b6, b7, b8 is equal to 11111, and the decrementation of a unit when the signal on bits b4, b5, b6, b7, b8 is equal to 00000. This function is obtained by the gates 110, 113, which receive at their input the outputs of gates 107, 108, respectively. When bits b4, b5, b6, b7, b8 take the maximum value 11111, the output of gate 108 is equal to 0, so that the output of gate 113 is forced to zero; the output of 105 being furthermore equal to 0, the input c1, c2, c3, c4, c5 of adder circuit 94 remains equal to 0, prohibiting the incrementation of a unit of register 96. Likewise, when bits b4, b5, b6, b7, b8 take the minimum value 00000 the output of gate 107 is equal to 0, so that the output of gate 110 is forced to 0, as are the high-weight bits c2, c3, c4, c5 of the input of adder circuit 94, the input c1 of the adder circuit being furthermore equal to 0, prohibiting the decrementation of a unit of register 96.

Figure 10 represents a fourth embodiment which is functionally similar to that shown in Figure 9 but which is implemented by replacing the adders 93, 94 with counters/down-counters 116, 117. The first counter 116 receives the phase-state signals E and L at its counting and down-counting inputs, respectively. It exhibits a 4-bit input IN receiving the median value recorded in register 97. Its output OUT provides the low-weight output signal b0, b1, b2, b3. It also exhibits upper and lower carry-over outputs 113a and 113b, respectively, as well as a control input 114 for reloading of its input IN. The upper carry-over output 113a is active when the counting input is incremented by a unit and the output OUT is at its maximum value 1111. Likewise, the lower carry-over output 113b is active when the down-counting input is incremented by a unit and the output OUT is at its minimum value 0000.

The upper and lower carry-over outputs 113a and 113b feed the counting and down-counting inputs, respectively, of the second counter/down-counter 117. Moreover, a gate 115 detects an active state of these two, upper and lower, carry-over outputs 113a and 113b and imposes a reloading of the input IN of the first counter 116 when one of these upper and lower carry-over outputs 113a and 113b is active. In this way, the first counter 116 is re-initialised to the median value contained in register 97 as soon as the low-weight output b0, b1, b2, b3 has exceeded one of its extreme values. Here too, it is therefore ensured that it is necessary to ascertain a phase shift for at least 8 or 9 (or another number, according to the value contained in register 97) successive states starting from one of the extreme values of the low-weight output b0, b1, b2, b3 in order to modify the value of the high-weight output 36a.

The second counter/down-counter 117 exhibits an output on 5 parallel bits constituting the high-weight output 36a feeding the control input of the oscillator 19. As in the previous embodiment, gates 107, 108 are provided receiving the values of the high-weight bits b4, b5, b6, b7, b8 of output 36a and adapted to prohibit the incrementation of a unit when the signal on bits b4, b5, b6, b7, b8 is equal to 11111, and the decrementation of a unit when the signal on bits b4, b5, b6, b7, b8 is equal to 00000.

In a device according to the invention the injection-locked oscillator is adapted so that an increment of the digital control signal brings about a modification of the natural frequency of the oscillator in accordance with a predetermined value step Δf . The choice of the number of bits retained in order to form the bus of the control signal from the parallel output of the accumulator circuit, and the choice of the adjustment step Δf , depend on the dynamics required for the phase-locked loop 25. For example, for a natural frequency of the injection-locked oscillator 19 of the order of 10 GHz, with a step Δf smaller than 1 %, and in particular of the order of 0.3 %, each increment of a unit of the digital control signal brings about a variation of this natural frequency of the order of 30 MHz. Furthermore, in the same example, if the control signal of the oscillator 19 comprises, as in the examples described, 5 bits, this signal makes it possible to implement thirty-two increments and therefore provides a range of adjustment of the natural frequency f_0 of the injection-locked oscillator 19 of the order of 10 % - that is to say, of the order of 1 GHz.

EXAMPLE

A prototype of a device according to the first embodiment of the invention was produced in the form of an ASIC circuit using 0.13 μm CMOS technology from STMicroelectronics. This prototype, encapsulated in a housing, was transferred to a glass-Teflon printed circuit, which made it possible to validate the entire operation of this architecture which successfully passed a complete electrical characterisation.

The invention may be the object of very numerous embodiment variants in relation to the exemplary embodiments represented in the Figures and described above. In particular, the various components of the device (lead/lag detector, decision-making converter, counting circuit, oscillator, pulse-generator etc.) may be implemented by other circuit structures known as such and providing the same functions. For example, circuits 100, 107, 108 may be the object of implementations (with other types of logic gates or other combinations of logic gates) other than those given by way of example and having the same technical functions.

CLAIMS

1. Device for clock extraction from a baseband serial signal, known as the received signal, that is representative of digital data and coded with a clock signal exhibiting a clock-bit frequency *fsr*, including:
 - a circuit (19) receiving a signal resulting from the received signal and clocked at the clock-bit frequency *fsr* and supplying, to at least one clock output (29), a clock signal, known as the reception clock signal, at least substantially synchronised and in phase with the clock-bit frequency *fsr* of the received signal,
 - a phase-control loop (25) including:
 - a first input (27) connected to a clock output (29) of the circuit (19) supplying a reception clock signal,
 - a second input (28) which is fed by a signal resulting from the received signal,
 - a digital phase detector (26) including a lead/lag detector connected to the first and second inputs (27, 28) and adapted to supply to at least one output (33a, 33b) at least one digital signal, known as the phase-state signal, that is representative of a phase shift between the reception clock signal and the received signal, and of the direction of this shift,
 - an output (36a) supplying a signal, known as the control signal, connected to an input, known as the command input, of the circuit (19) supplying a reception clock signal, which is adapted so that the value of the frequency of the reception clock signal depends on the value of the control signal received at this control input,
 - a circuit, known as the counting circuit (30, 35, 55, 91, 92, 116, 117), exhibiting an input connected to said output (33a, 33b) of the digital phase detector (26), said counting circuit being adapted to implement at least one

filtering by digital counting/down-counting in respect of the variations of the relative values of the digital signal which are supplied in time by the phase detector (26), and to supply a control signal in digital form, the value of which is a function of the result of this/these filtering(s), this value of the control signal being adapted to set a value of the frequency of the reception clock signal equal to a value, filtered in this way, of the clock-bit frequency f_{sr} of the reception clock signal, wherein:

- the circuit (19) supplying a reception clock signal is an injection-locked oscillator (19) with digital control, including a digital control input which is adapted to be able to receive the control signal supplied by the phase-control loop (25) in digital form, and so that the value of the natural frequency f_{os} of the oscillator (19) depends on the value of the control signal received at this control input,
- the phase-control loop (25) includes a circuit (30) exhibiting at least one input (32a, 32b) connected respectively to the output(s) of the lead/lag detector (26) and supplying to at least one output (31a, 31b) a digital signal, known as the filtered phase-state signal:

- having a first relative value after reception of a predetermined number N greater than 1 of successive identical values at the input, corresponding to N successive data bits of the received signal for which the lead/lag detector (26) has detected a phase shift in the same direction,

- having a second relative value after reception of N successive identical values at the input, corresponding to N successive data bits of the received signal for which the lead/lag detector (26) has detected a phase shift in the other direction,

- having a third relative value in the other cases, so that the relative value of the filtered phase-state signal is representative of the presence of a phase shift in the same direction and of the direction of this phase shift, for N successive data bits of the received signal, between the edges of the reception clock signal and the corresponding data bits of the received signal.

2. Device as claimed in Claim 1, wherein the lead/lag detector (26) is adapted to supply to a first output (33a) a digital signal (E) that is representative of the presence of a phase lead between the reception clock signal and the received signal, and to a second output (33b) a digital signal (L) that is representative of the presence of a phase lag between the reception clock signal and the received signal.

3. Device as claimed in one of Claims 1 or 2, wherein the lead/lag detector (26) is adapted to sample the received signal at the rising and falling edges of the reception clock signal.

4. Device as claimed in one of Claims 1 to 3, wherein the lead/lag detector (26) is adapted to implement a double sampling, one in phase with the edges of the reception clock signal, the other in quadrature with the edges of the reception clock signal, in such a manner as to determine the intermediate state of the received signal.

5. Device as claimed in one of Claims 1 to 4, wherein said circuit (30) supplying the filtered phase-state signal is a decision-making converter (30).

6. Device as claimed in one of Claims 1 to 5, wherein said counting circuit includes at least one circuit, known as the accumulator circuit (35, 55, 91, 92, 116, 117), including at least one input (32a, 32b) receiving a digital signal resulting from each phase-state signal supplied by the lead/lag detector (26), this accumulator circuit being adapted to supply a digital signal, known as the counting/down-counting signal, the relative value of which is representative of the reception of a plurality of relative values exhibited at the input(s) (32a, 32b) of this accumulator circuit.

7. Device as claimed in Claim 6, wherein said counting circuit includes successively a decision-making converter (30) and an accumulator circuit (35, 91, 92) which is adapted to aggregate the relative values of the filtered phase-state signal supplied by the decision-making converter (30).

8. Device as claimed in Claim 7, wherein the accumulator circuit exhibits a parallel output (36) and is adapted to supply to this parallel output (36) a parallel digital counting/down-counting signal, and wherein the injection-locked oscillator (19) includes a parallel digital control input including a number of bits lower than that of the parallel digital output (36) of the accumulator circuit, only a portion (36a) of the high-weight bits (36) of the parallel digital output of the accumulator circuit being linked to the bits of the parallel digital control input of the injection-locked oscillator (19), so that said control signal supplied by the counting circuit is formed from said portion (36a) of the high-weight bits of said counting/down-counting signal.

9. Device as claimed in Claim 8, wherein the parallel digital input of the injection-locked oscillator (19) comprises 5 bits, only the 5 high-weight bits of the parallel digital output (36) of the accumulator circuit being linked to the 5 bits of the parallel digital control input of the injection-locked oscillator.

10. Device as claimed in one of Claims 1 to 9, wherein the digital control input of the injection-locked oscillator (19) is connected to a circuit including a plurality of switches (45a, 45b, 45c, 45d, 45e), each switch being connected in series to at least one condenser integrated into the circuit of the oscillator (19) in such a manner as to modify its natural frequency.

11. Device as claimed in Claims 7 and 10, wherein each bit of the digital control input is linked to one of the switches.

12. Device as claimed in one of Claims 1 to 11, wherein the clock-extraction circuit includes, in addition, a circuit, known as the synchronisation-pulse generator (20), generating a signal of current pulses at the frequency of edges of the received signal and adapted for the operation of the injection-locked oscillator (19), this synchronisation-pulse generator (20) being adapted to supply the current-pulse signal to a single output (22) connected solely to a current input (23) of the injection-locked oscillator (19).

13. Device as claimed in one of Claims 1 to 12, for clock extraction and for extraction of digital data, including, in addition, a circuit (15) for sampling of the received signal with the reception clock signal, this sampling

circuit (15) having a first input, known as the signal input (17), connected to the reception input, and a second input, known as the clock input (18), connected to the clock output (29) of the injection-locked oscillator, this sampling circuit (15) being adapted to supply to at least one data output (16) digital data transmitted by received signal,

said device including at least one phase-shifting circuit (37a, 37b, 37c, 37d, 37e, 37f) which is adapted to introduce a constant phase difference between the signal input (17) and the clock input (18) of the sampling circuit (15), the total phase difference between these two inputs (17, 18) resulting from each phase-shifting circuit being adapted to guarantee a phase alignment of the signal at the signal input (17) and of the signal at the clock input (18).

14. Device as claimed in Claim 13, wherein the sampling circuit (15) is constituted by a simple flip-flop D.

15. Device as claimed in one of Claims 1 to 14, said device being free from any means of external adjustment.

16. Device as claimed in one of Claims 1 to 15, said device being implemented in accordance with a differential architecture.

17. Device as claimed in one of Claims 1 to 16, said device being implemented in the form of at least one integrated circuit incorporating at least the injection-locked oscillator (19).

18. Device as claimed in one of Claims 1 to 17, said device being adapted to be able to function with a clock-bit frequency f_{sr} higher than 500 MHz.